Pulsed Power Performance of β-Ga_2O_3 MOSFETs at L-Band

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***Abstract*— DC, small, and large signal results are shown under continuous wave and pulsed conditions for a β-Ga_2O_3 metal-oxide-semiconductor field-effect transistor operating at 1 and 2 GHz. The device has a maximum transducer gain, maximum output power, and peak power added efficiency of 13 dB (15 dB), 715 mW/mm (487 mW/mm), and 23.4% (21.2%), respectively at 1 GHz (2 GHz). We observe the continuous wave output power is limited to 213 mW/mm by drain dispersion likely from surface or interface traps in the gate-drain region as indicated by pulsed IV measurements. High parasitic resistances, as indicated by high knee voltages, also limit the power performance under continuous and pulsed large signal conditions.**

***Index Terms*— β-Ga2O3, MOSFET, small signal, large signal, radio frequency, pulsed radio frequency.**

I. Introduction

BETA-PHASE gallium oxide (β-Ga_2O_3) metal-oxide-semiconductor field-effect transistors (MOSFETs) are promising power devices due to high projected critical field strength, E_{crit}, of ~8MV/cm [1], [2] and experimental E_{crit} of >3.8 MV/cm [3]. Most β-Ga_2O_3 devices have been reported so far with excellent power switch figures of merit (FoM) [4]–[6], but it has also been noted that high E_{crit} allows for aggressive scaling of devices which can lead to a high RF FoM for β-Ga_2O_3 [7]. Early β-Ga_2O_3 RF devices have been reported with RF power gain up to nearly 20 GHz using small signal measurements [8], [9] and with limited gain in large-signal results up to 1 GHz [10], [11]. Due to the low thermal conductivity of β-Ga_2O_3, pulsed-power measurements provide an important means to evaluate the RF power performance potential of β-Ga_2O_3 devices. β-Ga_2O_3 devices with high RF FoM can lead to new opportunities for integrating RF and power conversion on available β-Ga_2O_3 native, large-area substrates.

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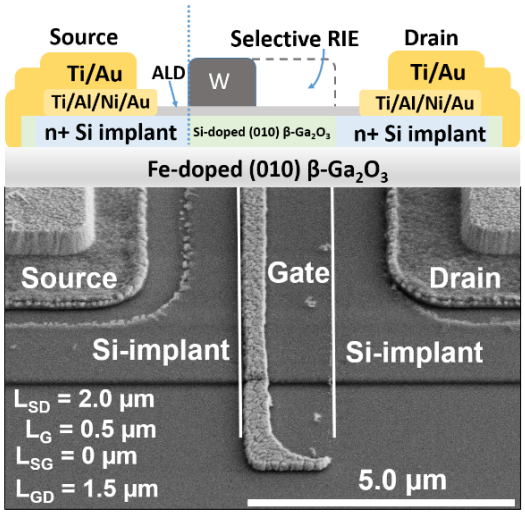

Fig. 1. Schematic of the fabricated device with corresponding scanning electron microscope image of the source-drain region. Device dimensions are included.

Here, we present small and large signal RF power performance at L-band for a β-Ga_2O_3 MOSFET. Higher gain and dc performance than previously measured RF power devices yield RF performance at 1 GHz with output power, P_{OUT} of 715 mW/mm and power added efficiency, *PAE*, of 23.4%. We further evaluate the small and large signal data under continuous wave (CW) and pulsed conditions up to 2 GHz demonstrating the validity and repeatability of the results for both our measurement technique and the device itself. We also provide insight into the limitations of our device, including drain dispersion, self-heating, and parasitic resistances, toward increasing performance.

II. Methods

β-Ga_2O_3 lateral MOSFETs were fabricated on a 65-nm-thick- β-Ga_2O_3 channel grown by molecular beam epitaxy with target Si doping of 2×10^{18} cm^{-3} on an Fe-doped (010)-oriented native substrate acquired commercially. Devices were fabricated based on a subtractive self-aligned gate (SAG) process. First, mesa isolation was performed by a BCl_3 dry etch followed by 30 nm of Al_2O_3 deposited by plasma enhanced atomic layer deposition to serve as a gate oxide and implant ionization cap. Tungsten (W) was

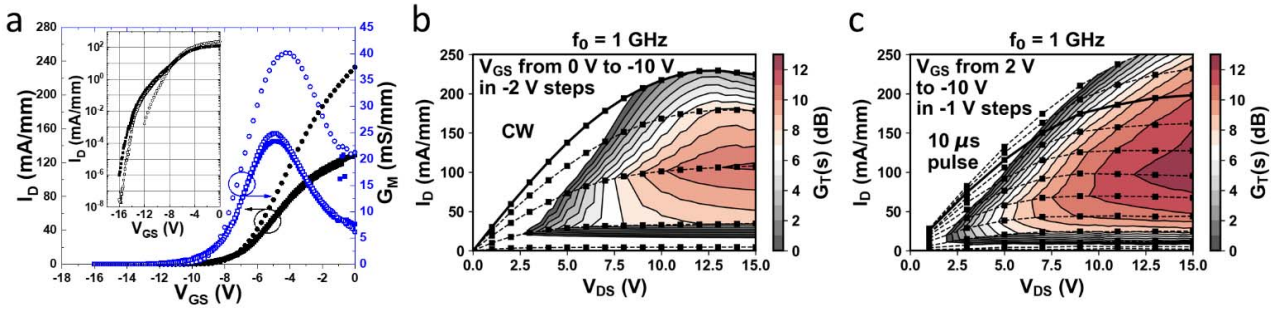

Fig. 2. DC transfer curve, ID vs. VGS, with inset log scale (a) and family of curves, ID vs. VDS, with contours showing the small signal gain, GT(s) for CW S parameters at 1 GHz (b) and 10 μs pulsed S parameters at 1 GHz (c). In (a), forward (closed symbols) and reverse (open symbols) are shown for VD = 15 V (circles) and VD = 5 V (squares). In (b) and (c), the VG = 0 V curve has a solid line for comparison.

sputtered 200 nm thick and an implant mask was defined by a subtractive dry etch process to form a scaled 2 μm channel which is an improvement over our previously reported SAG device [12]. The sample was implanted with Si targeting a box profile of 2.5×10^{20} cm^{-3} and a depth of 85 nm. A second dry-etch of the W implant mask was implemented to remove W to form the drift region while the remaining W formed the SAG electrode. The Al_2O_3 layer is designed to protect the Ga_2O_3 channel layer since it has high etch selectively to the W dry etch process. The Si implant was activated with a 2 minute 900 °C rapid thermal anneal (RTA) in N_2 overpressure. Next, the Al_2O_3 was selectively removed to deposit ohmic metal by electron beam evaporation and the sample was subject to RTA at 470 °C for 1 minute in N_2 overpressure. Interconnect metal (Ti/Au) was added to characterize the dc and RF performance. A final 3 μm of additional pad metal was deposited which was found to be critical for thermal dissipation during high power testing. Fig. 1 shows a schematic cross section and scanning electron microscopy image of the device prior to additional pad metal.

The resulting devices have a 2×50 μm gate periphery. The gate length, L_G, and gate-drain spacing, L_{GD}, were 0.5 μm and 1.5 μm, respectively, as measured with a scanning electron microscope. The free carrier concentration and mobility were measured to be 5.5×10^{17} cm^{-3} and 74 cm^2/(V·s), respectively, after fabrication using van Der Pauw structures on a sister sample. Transfer length method (TLM) was used to determine a contact resistance of ~16 Ω·mm, although variation across the wafer was significant due to an unoptimized implant step and ranged from 5 to 25 Ω·mm for sites with good TLM line fits.

Load-pull testing was performed at L-band using passive source and load tuners. All tuning was performed at 0 dBm available input power with a goal of maximizing transducer gain, G_T. Diode-based power sensors were used during load-pull to measure pulsed power where the gate bias, drain supply, and RF source were pulsed in order with a 2 μs pulse delay between turn on and turn off of each. The quiescent values were $V_{GQ} = 0$ V and $V_{DQ} = 0$ V for all pulsed load pull measurements with a period of 10 ms for the various pulse widths. The measurement window was positioned in the third quarter of each different pulse width and the pulsed power output waveform was observed to verify power did not fluctuate significantly over the pulse width measurement window. Power calibration values were also verified to remain unchanged as the pulse width was changed. Similar

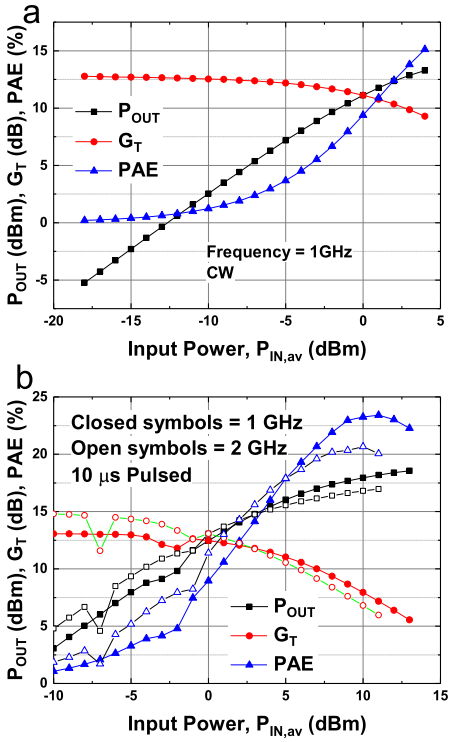

Fig. 3. Load-pull power sweeps for CW at 1 GHz (a) and for 10 μs pulse at 1 GHz and 2 GHz (b).

pulse conditions were used for pulsed scattering parameter (S-parameter) measurements.

III. Results

Fig. 2a shows a DC transfer curve demonstrating transconductance of 40 mS/mm and I_{ON}/I_{OFF} ratio greater than 10^8. Fig. 2 also shows the family of curves (J_D vs. V_{DS}) with overlapping contours of small signal gain, $G_{T(s)}$, for the CW (Fig. 2b) and 10 μs pulse width (Fig. 2c) measurements. The small signal gain was calculated from S-parameters (CW and 10 μs pulse width) at the tuning point for maximum gain found in the load-pull measurement. Fig. 3 shows power sweep data for CW (Fig. 3a) load-pull and 10 μs pulse width (Fig. 3b) load-pull at 1 and 2 GHz. The load-pull results were obtained at a supply voltage, $V_D = 20$ V, and bias, $V_G = -4.5$ V which is near the peak transconductance and expected maximum gain (see Fig. 2a) from the $V_D = 15$ V transfer curve.

To analyze the effects of dispersion and self-heating, Fig. 4 depicts the normalized output power of several different pulse widths. The maximum output power is reduced as

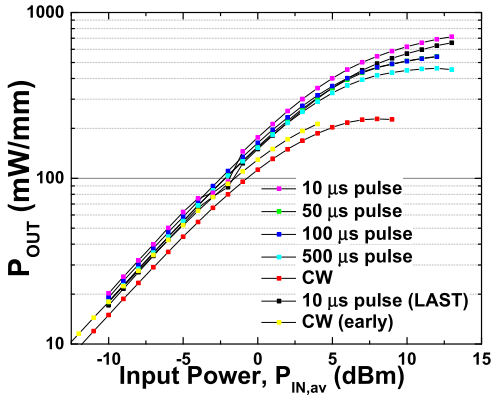

Fig. 4. A comparison of output power for pulsed and CW load pull with varying pulse widths (pulse period remains 10 ms throughout). The measurements include an early CW measurement and a short pulse (10 μs) measurement taken at the beginning and end (labeled "LAST") of testing for analysis of degradation.

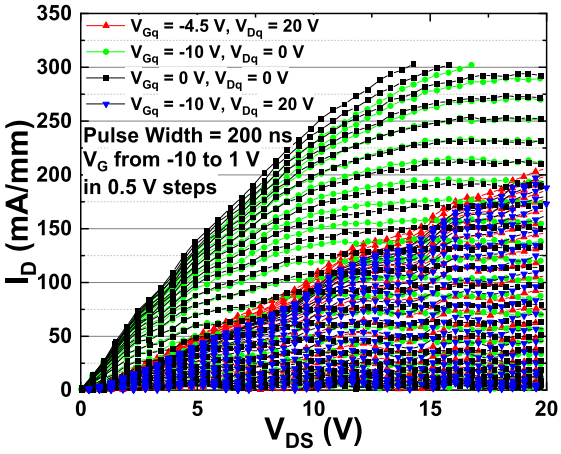

Fig. 5. Pulsed IV measurements for four different quiescent bias points demonstrating the drain dispersion effects at the same bias point used in load pull measurements (red triangles).

the pulse width (and therefore duty cycle) increases. Degradation also has an effect as the first and last short pulse (10 μs) measurements do not match exactly; however, after many measurements deep into gain compression, the device generally maintained the behavior shown in Fig. 2. Fig. 5 shows a pulsed-IV measurement analyzing the drain dispersion characteristics including a quiescent voltage at the bias used in the load pull measurements of Figs. 3 and 4, $V_D = 20$ V and $V_G = -4.5$ V.

IV. Discussion

The 2×50 μm device has a maximum G_T, maximum P_{OUT}, and PAE of 13 dB (15 dB), 715 mW/mm (487 mW/mm), and 23.4% (21.2%), respectively at 1 GHz (2 GHz) as seen in Fig. 3 for a 10 μs pulsed input power. These values agree well with the small signal results of Fig. 2. The 2 GHz G_T is slightly higher because of a larger tuning range for the passive tuner at 2 GHz. For CW input, the device achieved $G_T = 12.8$ dB, $P_{OUT} = 213$ mW/mm, and $PAE = 15.1\%$. In Fig. 4, it is clear that shorter pulse widths (reduced duty cycle) are effective in increasing the linear gain region to higher input powers and do not greatly affect the device gain. The reduced output power for increased pulse widths, thus, is likely a result of current collapse resulting from self-heating or drain dispersion. It is clear that with wider pulse widths the device is held under RF power longer causing potential self-heating effects.

The drain dispersion effect is not as well understood and may occur due to slow negative states near the device surface in the gate drain region causing a virtual gating and increased on-resistance. These slow states have enough time to clear for short pulse widths where the drain voltage is held at $V_D = 0$ V for longer periods of time. Fig. 5 indicates significant (>30%) drain dispersion at the maximum current when pulsing from the load-pull biasing conditions. Fig. 5 also includes a pinched-off condition, $V_{Gq} = -10$ V, $V_{Dq} = 20$ V, curve to differentiate the effects of drain dispersion from self-heating and a gate lag measurement $V_{Gq} = -10$ V, $V_{Dq} = 0$ V to show the gate dispersion. Unlike AlGaN/GaN HEMT devices where polarization causes surface charge leading to similar effects [13], surface charge in our device is likely related to traps at the surface of the Al_2O_3 or at the gate-oxide-Ga_2O_3 interface, either one being filled by electrons under positive drain biases. The drain dispersion therefore, may have been exacerbated by the processing of the drift region which includes a W dry etch; however, we have observed drain dispersion in devices without this dry etch. Mitigation of drain dispersion may be possible through an alternate surface preparation or passivation layers (gate oxides). These methods are currently under investigation.

The shorter 200 ns pulse widths in Fig. 5 do indicate less self-heating than those of Fig. 2c (10 μs pulse widths) as seen by the >20% reduction in the max current. Some of this reduction is likely related to degradation in the device as the measurements were taken at a midpoint and at the end of power measurements. Additional studies are ongoing to characterize, differentiate, and remedy the effects of drain dispersion, self-heating, and device degradation. Despite these limitations, the devices still performed significantly better than previous load-pulled Ga_2O_3 devices [10], [11].

We also point out that parasitic resistance plays a large role in limiting RF performance, as it does in power switch performance as described in [3]. The curves in Fig. 5 indicate that the power measurements at 20 V will quickly be limited by the high knee voltage of >15 V even under ideal pulsed conditions. In our devices, although the self-aligned Si implant has significantly reduced the source access resistance, the contact resistance and sheet resistance of the implanted regions remains unoptimized [12]. Others have shown reduced contact resistance by etching of the implant region under the contacts [14] or using regrown contact layers [15]. The evaluation of these methods and Si-implant optimization are also ongoing towards future high-performance β-Ga_2O_3 devices.

V. Conclusion

We have reported improved RF power performance up to L-band using β-Ga_2O_3 SAG MOSFETs with sufficient RF gain. The RF device performance indicates early promise for efficient RF power with $PAE > 23\%$ and $P_{OUT} > 700$ mW/mm at 1 GHz. Significant opportunities for device engineering remain to remove parasitic resistance, dc-to-RF dispersion and thermal challenges for β-Ga_2O_3 devices. A path to using the β-Ga_2O_3 material system for integration of RF and low-loss power conversion circuitry exists for future optimized devices.

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