A Study on the Effect of Pulse Rising and Falling Time on Amorphous Oxide Semiconductor Transistors in Driver Circuits

Hyeon-Jun Lee and Katsumi Abe

***Abstract*— This study is on the degradation phenomenon of oxide semiconductor thin-film transistor under dynamic stress applied to the drain. The current reduction that occurs during the rise and fall of the pulse was clearly observed through electrical measurements and the cause of the current drop was investigated via a two-dimensional device simulation. The results confirmed that while the instantaneous rise of the pulse provides high energy to the electrons ejected to the drain, the rapid drop of the pulse only produces impact ionization rates in very small areas with an electronic backflow to the drain. Furthermore, a model based on these relationships is proposed for asymmetric local degradation by high energy (*hot*) electrons.**

***Index Terms*— Oxide semiconductor, *a*-IGZO, impact ionization, impact generation, asymmetrical local defect, degradation, pulse stress.**

I. Introduction

AMORPHOUS oxide semiconductors are a promising material in high-performance displays because they have high electron mobility and extremely low leakage current compared to conventional amorphous silicon thin-film transistors (TFTs) [1]. Those based on oxide semiconductors that take advantage of this feature are used as pixel TFTs and in driver circuits.

Improving device reliability is a top priority for industrial applications. Thus far, when testing pixel TFTs, most studies [2]–[7] have been limited to the state generation caused by either the charging effect at the gate insulator's interface or the unbalanced potential distributions that act as traps at the interface [8]. However, there have been a few reports [9]–[11] that mention a serious current drop [12] with hump behavior [13] in the gate driver integrated circuit. It causes serious display issue and there has not yet been a solution to cope with or to detour around it. This current drop is assumed to be due to local defects resulting from the energy transfer [9], [10] of high-energy (*hot*) electrons moving under high electric field into a surrounding lattice. This could be an obstacle to the application of oxide semiconductors in these cases.

In this letter, we report the impact of the driving pulse signal on driver circuits to figure out the formation of the asymmetrical local defects. The contribution of pulse rise and fall to the current drop was evaluated through individual pulse timing control. In particular, the impact ionization rates (IIRs) were taken into account to estimate the quantity of the hot electron, and the IIR was calculated via a 2D Atlas device simulation.

II. Experiments

Amorphous $InGaZnO_x$(*a*-IGZO) TFTs with an inverted staged structure were used in this study. The *a*-IGZO 40 *nm* was deposited on a gate insulator SiO_x 200 *nm*. A gate electrode patterned with Mo metal was formed under the gate insulator and the source/drain electrode 100 *nm* was deformed (width of 10 μm and length of 10 μm) through the photolithography on the *a*-IGZO. The gate-via was formed by a reactive ion dry etching process. A passivation layer (SiO_x, 200 *nm*) was formed by PECVD on the *a*-IGZO TFTs and it was annealed at 350 $^\circ C$ for 1 hour in an air environment to improve the stability of the transistors.

The high-voltage drain pulsed stress (HVDS) was evaluated by injecting a pulse signal amplified through a high-speed bipolar amplifier (nF HSA 4011) into the device. The pulse was supplied by a pulse function arbitrary generator (KEYSIGHT 81160A). The pulse voltage whose peak intensity is 48 V, frequency is 1 Hz, and duty-cycle is 70 % is applied to the drain, and both the source and the gate is grounded. It makes the same stress condition as the display driver circuit. 1 Hz is a very low frequency for practical application of the TFT as a driver, but the HVDS test relies strongly on the number of pulses applied, *not* the speed of the frequency [9]. Therefore, this study was conducted at 1 Hz, which is easy to adjust the timing of the rising/fall time of the pulse. The total stress time is 1 hour.

The IIRs were calculated via Silvaco's ATLAS 2D simulator package [14]. A configuration similar to that in the fabricated materials and devices was employed in the simulator. Selberherr's impact ionization model was utilized as a function of the lattice temperature and bandgap. In this study, we assumed

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that there was no hole contribution in the oxide semiconductor system because the utilized a-IGZO is a native n-type semiconductor.

III. Results and Discussion

Items that evaluate the reliability of the unit TFT are divided into gate bias stress tests where threshold voltage shifts occur and HVDS tests that result in current degradation. HVDS, which injects high-voltage pulses into the drain electrodes, is known to significantly reduce the current ability (current ratio after reliability test compared to the initial value). Previous studies have shown that increasing the pulse rising/falling time under the same peak voltage gives rise to reducing current degradation. [9] The region of the source electrode in the HVDS evaluation cannot affect the electronic flow and is not discussed in this study. In this study, we applied pulses with different rising/falling times to investigate the origin of the asymmetrical- and additional- local defect states.

If the pulse rising and falling times of the injected HVDS were fixed at 0.2 s, no reduction in the current ability occurred, as shown in Fig. 1(a). The I-V characteristic V_{ds} (the maximum voltage between the drain and source) at 0.1 or 10 V attained the same current ability before and after the high-voltage pulse had been injected 100 times (the dashed line in Fig. 1). When the pulse falling time was drastically reduced, applying the pulse caused a little reduction in the current, as shown in Fig. 1(b). On the other hand, when the pulse was applied with a short rising time ($t_f = 10^{-7}s$), a significant decrease in current accompanied by a hump near $V_g = 7$ V was observed (Fig. 1(c)). Additionally, when reducing both timings, the falling and rising, the current drop became more severe (Fig. 1(d)) and the shape was very close to that in Fig. 1(c), i.e. rising for only a short time. It is possible to recover through thermal treatment. The current drop in the HVDS is reversible. This local degradation is not a permanent phenomenon of the bond breaking and is presumed to be the generation of local defects due to minute changes in the binding state.

The impact ionization phenomena arising from high voltage pulses are very important in understanding local degradation phenomena or asymmetrical local defect state generation. To analyze the correlation between asymmetrical local defect generation and the pulse rising contribution shown in Fig. 1, an ATLAS 2D simulation was used to identify the transient current and the IIR at the transient time. Figure 2 (a) and (b) show the IIR of the pulse rising time for $t_r = 10^{-7}$ and 0.2 s near the drain electrode edge at the transient time when the pulse approached its highest value of 48 V. The IIR increased significantly when the pulse increased quickly ($t_r = 10^{-7}s$) whereas the IIR at the 9.6 μm region was reduced when the pulse rose slowly. Meanwhile, the IIR depending on the pulse falling time showed similar behavior in both cases ($t_f = 10^{-7}$ and 0.2 s) near the drain electrode at the 9.6 μm region (not shown here). However, a very high IIR appeared at the edge of the drain electrode in a very local and small area when the pulse was quickly switched off to the ground (Fig. 2(c)). The current was back flowing at the edge of the drain electrode and the largest current was injected from the oxide semiconductor to drain at the highest IIR. When the pulse fell slowly, there was no impact ionization at the edge of the electrode (Fig. 2(d)).

In the case of rapid voltage rise during pulse signal injection, it seems that electrons with high potential energy give rise

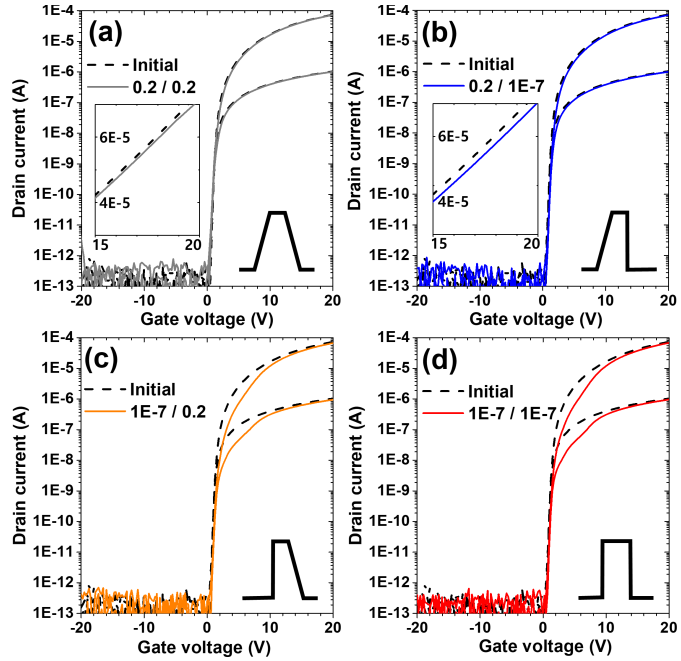

Fig. 1. Electrical transfer characteristics before and after the high voltage drain pulsed stress (HVDS): (a) pulse rising time (t_r) = 0.2 s/pulse falling time (t_f) = 0.2 s, (b) $t_r = 0.2$ s / $t_f = 10^{-7}$ s, (c) $t_r = 10^{-7}s$ / $t_f = 0.2$ s, and (d) $t_r = 10^{-7}s$ / $t_f = 10^{-7}s$. The dashed and solid lines represent the initial and stressed (after 100 pulses) characteristics, respectively. Insets show the linear scale I-V characteristics and the schematic pulse-shapes. The pulse peak amplitude is fixed at 48 V.

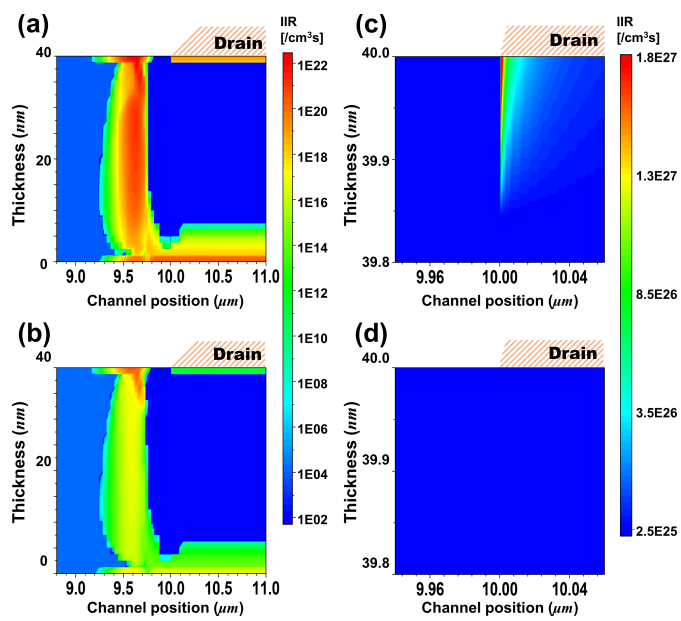

Fig. 2. Transient impact ionization rate (IIR) that occurs when the pulse reaches (pulse rising) 48 V or starts to decrease (pulse falling) at 48 V. IIR for the pulse rising time (t_r) of (a) $10^{-7}s$ and (b) $t_r = 0.2$ s, and the pulse falling time (t_f) of (c) $10^{-7}s$ and (d) 0.2 s.

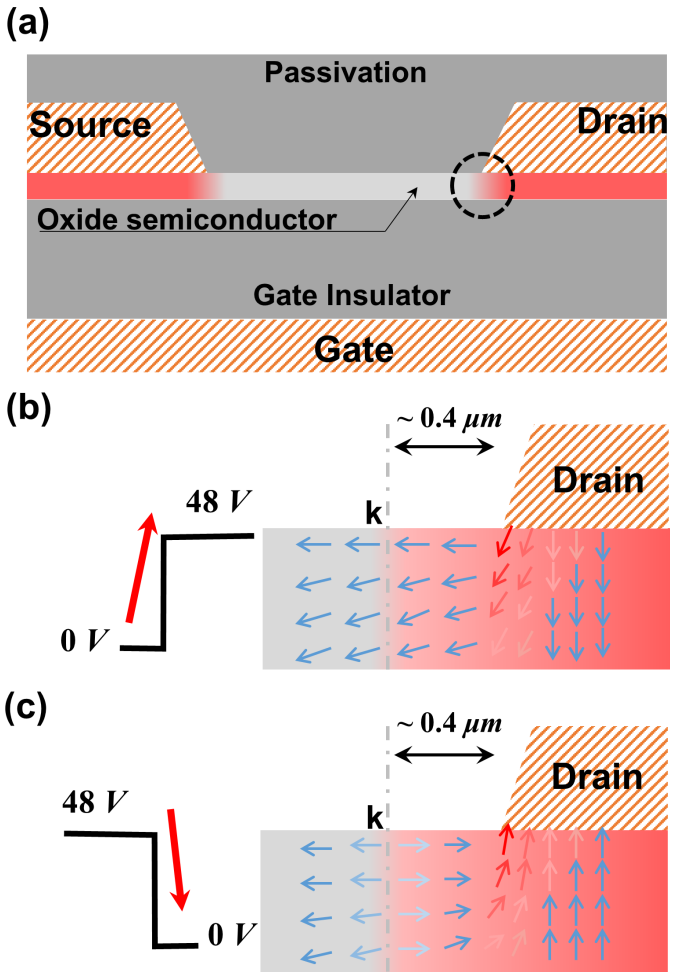

Fig. 3. The schematic figures of (a) the cross-sectional device and magnified drain electrode area when the pulse (b) rising and (c) falling in the oxide semiconductor. The assigned red color included region between k-point and the under Drain electrode is a high electron density area ($\sim 10^{19}/cm^3$). The gray area (from k-point) indicates the low electron density ($\sim 10^{16}/cm^3$). The arrow is the electron current density flow (Je^-).

to impact ionization near the drain area. The impact ionization seems one of the origins of the asymmetrical local defect states. This is due to energy transfer to the oxide semiconductor caused by the high energy electron collision with the lattice. [15] However, if the pulse's voltage rise occurs slowly, the generation of the *hot* electrons decreases or their energy becomes weak, resulting in weak impact ionization. This occurs most of the time in the drain edge area (the part shown in Fig. 3(a) dashed circle).

Figure 3(b) shows a schematic diagram of the electron current density (Je^-) flow occurring at the transient 48 V is. Je^- is quickly injected into an active layer from the drain. Especially in drain edge, Je^- is injected with high energy. In a structure where oxide semiconductors are used as active layers, the electronic concentrations under the electrodes are relatively high [16] for various reasons and donor concentrations. In this study, a structure with a high electron concentration ($10^{19}/cm^3$) (from the under the drain electrode to 0.4 μm (k point)) was considered, and the density of the semiconductor area operated by the channel was considered as the level of $10^{16}/cm^3$. The impact ionization appears to have risen locally due to the energy conversion of *hot* electrons at k-point, which is the boundary of rapid changes in electron concentration.

On the other hand, if the voltage drop of the injected pulse progresses rapidly, strong impact ionization occurs in the very local area of the drain edge as the electrons inside the oxide semiconductor are sucked into the drain as shown in Fig. 3(c). The backflow of current densities in the drain only occurs in a very narrow region, so the influence of the *I-V* characteristic test is slight and likely increases in the case of long driving periods or for an applied voltage higher than the critical voltage. A small IIR may occur at k-point when pulse falling, but a negligible level does not affect the macro *I-V* characteristics.

IV. Conclusion

We report the impact of altering the driving pulse signal in an oxide semiconductor transistor used in driver circuits. We discovered through experimentation that the current drop in the HVDS is caused by the pulse rising during the driven pulse. In addition, it was confirmed by device simulation that a rapid rise in pulse signal causes impact ionization near the drain side and provides a local defect state that disrupts the flow of electrons. Based on this dependence, we proposed a model considering asymmetrical local degradation by the *hot electron* contribution in the oxide semiconductor system under high voltage at the drain.

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