Stateful Logic Operations in One-Transistor-One-Resistor Resistive Random Access Memory Array

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***Abstract*—Nonvolatile and cascadable stateful logic operations are experimentally demonstrated within a 1 k-bit one-transistor-one-resistor (1T1R) resistive random access memory (RRAM) array, where NAND gates serve as the building blocks. A robust dual-gate-voltage operation scheme is proposed. The effects of the transistor ON logic operation and the robustness to device parameter variations are discussed. The parallel 4-bit bitwise XOR operation is experimentally implemented in the 1T1R array by cascading NAND gates. This letter presents a feasible approach to in-memory computing for large-scale circuits.**

***Index Terms*—Stateful logic, in-memory computing, resistive random access memory (RRAM), one-transistor-one-resistor (1T1R) array.**

I. Introduction

CONVENTIONAL von Neumann architecture with separated processing and memory unit is facing the bottleneck of computation speed and energy efficiency as applications become more data-centric [1]. In-memory Boolean computing is one of the most promising approaches that attempts to address this issue by performing Boolean computing within memory [2], [3]. Resistive random access memory (RRAM), featuring nonvolatile storage, fast switching speed, good endurance and compatibility to CMOS fabrication process, is expected to be a potential candidate for in-memory Boolean logic computing [4], [5].

Over the past 10 years, several RRAM-based Boolean logic operation schemes have been proposed, such as V-R logic, R-V logic, V-V logic and R-R logic, differing by the input and output [2]. The input of V-R logic [6]–[10] is the voltage applied to the computation cell, while the output is the resistance state of computation cell. R-V logic [11], [12] is performed by reading the resistance of input cells and comparing it with a threshold to determine the output voltage. As for V–V logic [13], input and output are both described by digital voltages. In R-R logic [14]–[22], the input and output are both resistance of the non-volatile memory elements. Such R-R logic is a truly nonvolatile and cascadable in-memory Boolean operation, which is also referred to as stateful logic [2]. Stateful logic is preferable since it needs no conversion overhead in contrast to V-R and R-V logic, and it is nonvolatile compared with V-V logic. So far most of works regarding stateful logic focus on 1R-based cross-point arrays [14]–[20], which suffer from sneak-path issue that leads to read/write/logic operations errors or failures. One-transistor-one-resistor (1T1R) architecture has been widely adopted to address the sneak path problem of crossbar array [23], [24]. However, the hardware implementation of stateful logic in 1T1R array is rarely reported.

In this work, we experimentally demonstrate the stateful logic operation in a 1k-bit 1T1R RRAM array, where the NAND gates serve as the building blocks. A dual-gate-voltage operation scheme is proposed for stateful logic operations in 1T1R array. The effect of the transistor on logic operation and the robustness to set voltage variation and resistance variation are discussed. The parallel 4-bit bitwise XOR operation is experimentally demonstrated in the 1T1R array by cascading NAND gates. The method to construct a complex logic gate and the array-level operation scheme are given.

II. 1T1R RRAM Array

Fig. 1(a) shows the structure of fabricated 1k-bit (32×32) 1T1R array for the logic operation. The 1T1R cell consists of a $TiN/TaO_x/HfO_2/TiN$ RRAM [24] and a NMOS transistor fabricated in 130 nm CMOS process. The fabricated array is shown in Fig. 1(a). The microphotograph of fabricated 1k-bit 1T1R RRAM chip, the photograph of DUT (Device Under Test) board and packaged 1T1R RRAM chip are shown in Fig. 1(b). The WL driver was integrated inside the chip. The analog multiplexers and serial reference resistors for logic operation were integrated on the DUT board. The typical quasi-static DC current-voltage (I-V) curve of the fabricated RRAM array is shown in Fig. 1(c). By applying SET voltage on the BL or RESET voltage on the SL,

Manuscript received June 30, 2019; revised July 25, 2019; accepted July 26, 2019. Date of publication July 30, 2019; date of current version August 23, 2019. This work was supported in part by the National Natural Science Foundation of China Program under Grant 61604005 and Grant 61841404 and in part by the National Key Research and Development Program under Grant 2017YFB0405600 and Grant 2018YFA0701501. The review of this letter was arranged by Editor B. Govoreanu. *(Corresponding authors: Peng Huang; Jinfeng Kang.)*

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Digital Object Identifier 10.1109/LED.2019.2931947

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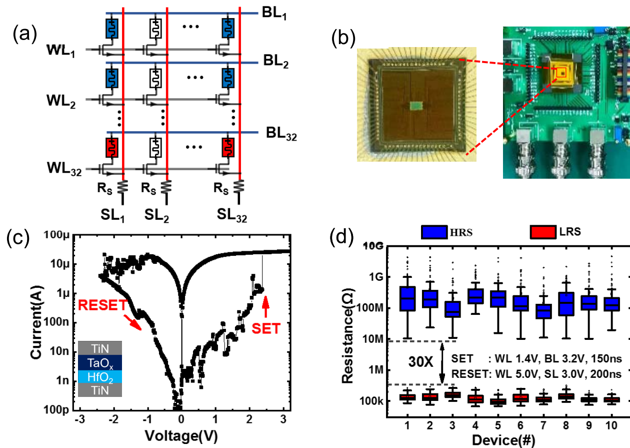

Fig. 1. (a) The structure of fabricated 1k-bit 1T1R array for the logic operation. (b) The microphotograph of fabricated 1T1R RRAM chip, the photograph of DUT board and packaged 1T1R RRAM chip. (c) Typical measured I-V curve of the 1T1R cell. (d) The box plot of resistance distribution of 10 typical devices measured over 100 consecutive SET/RESET pulse cycles.

the device can be switched between high resistance state (HRS) and low resistance state (LRS). Fig. 1(d) shows the resistance distribution of ten typical devices measured over 100 SET/RESET pulse cycles, exhibiting a resistance window larger than 30 even when cycle-to-cycle and device-to-device variations are considered, which is desirable for stateful logic. Electrical measurements were carried out using STM32F103 Series MCUs, Agilent B1500A semiconductor parameter analyzer, Agilent 81160A pulse function generator, and Agilent Infiniium MSO9404A Series Oscilloscopes.

III. Stateful Logic Operations

NAND gate is a universal logic gate, since any binary logic function can be realized using a finite number of NAND gates. In this work, NAND gates are selected to serve as the building blocks for large-scale logic circuits. A novel dual-gate-voltage operation scheme for stateful logic operations in 1T1R array is proposed, as illustrated in Fig. 2. There are three 1T1R cells in the NAND gate: two input cells denoted as A and B and one output cell denoted as Y, as shown in Fig. 2(a). The state variables for logic operations are represented by device resistance, where LRS is defined as logical ‘0’ and HRS is defined as logical ‘1’. A reference resistor R_S is serially connected to the common source line (SL). In this work, the resistance window R_H/R_L is assumed to be sufficiently large and R_S is chosen as 1MΩ to meet the requirement of $R_L << R_S << R_H$. Before logic operations, the output cell Y is initialized to HRS by RESET operation. A large voltage V_{gH} is applied to the gates of input cells A and B to guarantee that the corresponding transistors are turned “on” during the logic operation. The relatively small voltage V_{gL} is applied to the gate of output cell Y. The small reference voltage V_R is applied to the BL of A and B, while the relatively large voltage V_{DD} is applied to the BL of Y.

The proposed dual-gate-voltage operation scheme is illustrated by Fig. 2(b). When inputs A and B are both in HRS (2HRS), the potential of the common node V_{com} is nearly 0 and the transistor of Y is turned “on” (equivalent to a closed switch). Therefore, the voltage drop across RRAM Y (V_Y)

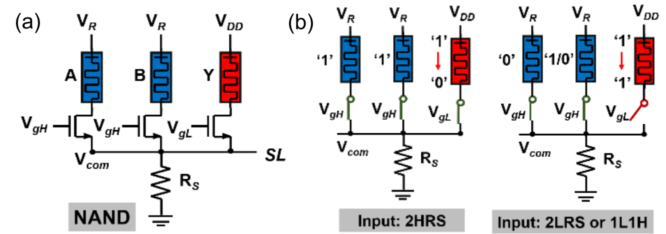

Fig. 2. Proposed operation method of NAND logic. (a) Basic circuit. (b) The principle of the logic operation. LRS is defined as logical ‘0’ and HRS is defined as logical ‘1’. The large voltage VgH is applied to the gates of input cells A and B, while the relatively small voltage VgL is applied to the gate of output cell Y.

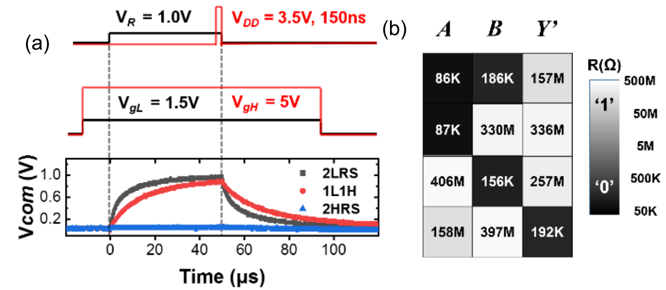

Fig. 3. Experimental results of NAND logic operation. (a) The applied voltage waveform and measured electrical potential on the common SL with different input combinations. (b) Measured truth table. The states of the input device (output device) before (after) logic operation are read out as resistance shown by grayscale maps.

approximates to V_{DD}, which is large enough to switch Y to LRS. If any input device is in LRS (2LRS or 1L1H), V_{com} will be charged to a high voltage close to V_R and the transistor of Y is “off” (equivalent to an open switch) since $V_{GS} = V_{gL} - V_R < V_{th}$. As a result, V_Y approximates to 0 and Y stays at HRS.

The proposed dual-gate-voltage operation scheme is experimentally demonstrated, as shown in Fig. 3. The applied voltage of V_R, V_{DD}, V_{gH}, and V_{gL} is shown in Fig. 3(a). To verify the process of logic operation, V_{com} is monitored by oscilloscope as shown in Fig. 3(a). When the inputs are 2HRS, $V_{com}$is close to 0. When inputs are 2LRS or 1L1H, $V_{com}$is charged to a relatively high level above 0.8V. Note that the threshold voltage of NMOS in this work is around 0.78V, implying that the transistor of Y works in cut-off mode, since $V_{GS} = V_{gL} - V_{com} \approx 1.5V - 0.8V < 0.78V$. Therefore, the principle of the proposed dual-gate-voltage scheme is verified by the experiment. The resistance of the input device (output device) before (after) logic operation is read out, as shown in Fig. 3b, which directly verifies the correct result of NAND operation.

Note that the voltage pulses of V_R and V_{DD} are not assigned at the same time in the experiment, considering the large parasitic capacitance in the peripheral PCB circuits, which results in such a large RC delay that the rise time of V_{com} is larger than the duration of SET process in the experiment. If V_R and V_{DD} are assigned simultaneously, the output RRAM will be set immediately, well before V_{com} is charged. Therefore, V_R should be applied in advance to charge the common SL. In this system, the speed of logic operation is chiefly limited by the rise time of V_{com}. The parasitic capacitance will be dramatically reduced [14] in

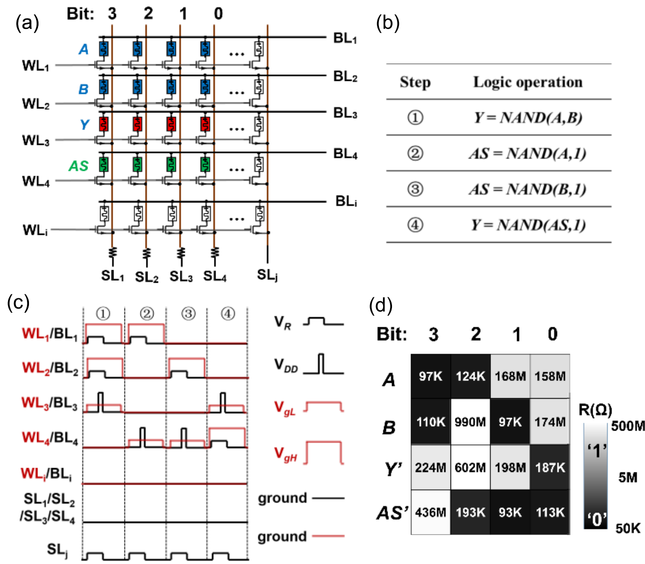

Fig. 4. Demonstration of 4-bit bitwise XOR. (a) Array configuration of XOR circuit, every single SL represents an independent 1-bit XOR. (b) Computation procedure of XOR. (c) The timing diagram of XOR, the red lines represent the signals applied to WL. (d) Experimental results of the 4-bit bitwise XOR with input A[3:0] = 0 0 1 1 and input B[3:0] = 0 1 0 1. The states of the output devices Y' and AS' after logic operation are read out and shown by grayscale maps.

a hybrid integrated circuit of 1T1R arrays and peripheral circuits. Therefore, the speed of the logic operation can be greatly improved.

Other arbitrary logic can be constructed by assembling NAND gates. XOR is a typical logic operation widely used in full adders. In order to show how to perform the logic operation at array-level, the parallel 4-bit bitwise XOR operation is experimentally implemented in the fabricated 1T1R array, as shown in Fig. 4. The array configuration of XOR is shown in Fig. 4(a) and every single SL represents an independent 1-bit XOR. Compared with NAND logic, an additional assistant cell AS is required. The XOR logic operation can be implemented in four steps as shown in Fig. 4(b). Here, open circuit is used as input logical '1' to execute 'Y = NAND(A, 1)' operation. In other words, 'Y = NAND (A, 1)' can be regarded as the INV logic 'Y $=\bar{A}$ ', while 'Y = AND(A, 1)' can be regarded as the TRANSFER logic 'Y = A'. More details about the assembling method to construct XOR logic can be found in [15]. Fig. 4(c) shows the timing diagram of trigger signals applied to the array with the red lines representing the signals applied to WL. The unselected WLs and BLs are connected to ground, while the unselected SLs are directly connected to V_R to avoid disturbs to the unselected cells. Experimental result of the 4-bit bitwise XOR with input A[3:0] = {0 0 1 1} and input B[3:0] = {0 1 0 1} is shown in Fig. 4(d). The experimental demonstration of the 4-bit bitwise XOR means that the parallel stateful logic operations can be implemented at array-level.

One significant challenge of RRAM technology is its device variations, including set voltage variation and resistance variation [25]. These variations may cause errors to the logic operation [21]. Therefore, the logic operation should be robust to the device variations. In order to quantitatively describe the robustness of the logic operation, the relationship between the

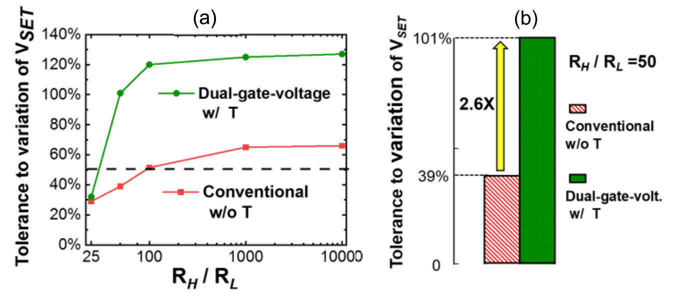

Fig. 5. (a) The relationship between the resistance window (RH/RL) and maximum tolerance to set voltage variation. The proposed dual-gate-voltage scheme is compared with the conventional operation scheme [15]. (b) The case of $R_H/R_L = 50$.

resistance window (R_H/R_L) and maximum tolerance to set voltage variation is investigated using HSPICE simulation. For each given resistance window, there is a limit to set voltage variation to ensure successful logic operation. The set voltage variation is defined as

$$\text{Variation of } V_{SET} = \frac{(V_{SET})_{max} - (V_{SET})_{min}}{(V_{SET})_{mean}} \times 100\%$$

In the simulation, we assume a symmetrical distribution of V_{SET} and $(V_{SET})_{mean} = 2$V. The resistance is assumed to vary around the geometric mean. $R_M = (R_H R_L)^{1/2} = 1\text{M}\Omega$. The NMOS model from HHGrace 130nm PDK is used. The simulation result is shown in Fig. 5. Compared with the conventional scheme [15] based on 1R cells, the dual-gate-voltage scheme shows higher robustness to set voltage variation as R_H/R_L varies from 25 to 10000. For example, in the case of $R_H/R_L = 50$, the tolerance to V_{SET} variation reaches 100% for the dual-gate-voltage, which means the NAND logic can be executed correctly when set voltage varies from $(2-1)$ V to $(2+1)$ V. The tolerance to set voltage variation is improved by 2.6 times compared with conventional method.

The variation exists in the low resistance and high resistance of the RRAM will reduce the effective resistance window. For each given set voltage variation, there is a lowest limit to resistance window to ensure successful logic operation. As shown in the Fig. 5(a), if V_{SET} variation is 50%, the dual-gate-voltage scheme can tolerate a smaller resistance window than conventional scheme, which means that the dual-gate-voltage scheme can tolerate larger resistance variation than conventional scheme.

IV. Conclusion

Stateful logic operations are successfully demonstrated in the fabricated 1k-bit 1T1R RRAM array. A dual-gate-voltage operation scheme is proposed for the stateful logic operation in 1T1R array. With the help of the transistor, the dual-gate-voltage operation scheme shows enhanced robustness compared with the conventional scheme in 1R array. The parallel 4-bit bitwise XOR operation is experimentally demonstrated in the 1T1R RRAM array by cascading NAND gates. This work provides a guideline for stateful logic operations in 1T1R array and paves the way for highly efficient in-memory computing for large-scale circuits.

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