ScAlN/GaN High-Electron-Mobility Transistors With 2.4-A/mm Current Density and 0.67-S/mm Transconductance

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***Abstract*— We report the dc and RF performance of ScAlN/GaN high-electron-mobility transistors (HEMTs). The ScAlN/GaN material was epitaxially grown onto a GaN template on a 4-in 4H-SiC substrate by molecular beam epitaxy. The sheet resistance was measured to be 236 ± 4 Ω/□ across the wafer by the transfer length measurement. Selective area regrowth of highly doped GaN was implemented to reduce contact resistance (R_C) as low as 0.1 Ω · mm. HEMT devices with 2 × 150 μm gate width and 140-nm T-gate process show a maximum current density and a transconductance of 2.4 A/mm and 0.67 S/mm, respectively. The extrinsic small-signal gain was measured as a function of drain bias and gate length with extrinsic cutoff frequency and maximum oscillation frequency reported up to 88 and 91 GHz, respectively.**

***Index Terms*— ScAlN, GaN, radio frequency, small-signal, large-signal, HEMT.**

I. Introduction

In the $Al_xGa_{1-x}N$ material system, a two dimensional electron gas (2-DEG) is formed when a net total polarization charge is presented at the heterostructure interface [1], [2]. The $Al_xGa_{1-x}N$/GaN material system has been researched heavily as the incumbent class of state of the art high power amplifier performance at microwave and millimeter-wave frequencies of operation. The combination of high power density [3]–[5] and high frequency [6] device characteristics has enabled impressive performance at X-band [7] and Ka-band [8] frequencies. Analogous to $Al_xGa_{1-x}N$, $Sc_xAl_{1-x}N$ can be a promising material for use as a barrier layer in GaN HEMTS, but with a higher spontaneous polarization charge [9], [10]. More recently, Hardy *et al*. have demonstrated the affect by growing a ScAlN barrier with a Sc mole fraction of 14 % [11]. They measure a sheet charge (n_s) of 3.4×10^{13} cm^{-2} with an electron mobility (μ) of 910 cm^2/V · s. Comparable sheet-resistance (R_{SH}) has been obtained with quaternary $Al_xIn_yGa_{1-x-y}N$ [12]–[19] and N-Polar GaN [20]–[22], though with stronger spontaneous polarization properties while maintaining the lattice matched condition, $Sc_xAl_{1-x}N$ has the capability of obtaining high RF performance with aggressive barrier scaling and gate length reduction. Here, we present the first report of a ScAlN/GaN HEMT with high-performance enabled by combination of selective area ohmic contact regrowth and T-gate process.

A TEM image of a typical device is shown in Fig. 1a. Low contact resistance (R_C) was achieved using an ohmic regrowth process which resulted in $R_C < 0.1$ Ω · mm. A symmetric T-gate design was used with a dose spread giving gate lengths (L_G) ranging from 110 nm to 180 nm. Maximum current density and transconductance were measured to be 2.4 A/mm and 0.67 S/mm, respectively. Maximum values for cutoff frequency (f_T) and maximum oscillation frequency ($f_{MAX,UPG}$) were measured to be 88 GHz and 91 GHz, respectively on a 2 × 150 μm device. Both single device and wafer scale results will be reported.

II. Epitaxial Growth and Device Fabrication

Epitaxial structure design and growth were performed by Qorvo. A four inch GaN-on-4H SiC template was prepared by MOCVD, which was immediately loaded into a gas source MBE reactor for the ScAlN heterostructure. The 6.5 nm ScAlN barrier was grown onto a 1 nm and 2 nm AlN and $Al_{0.25}Ga_{0.75}N$ spacer, respectively, and then capped with 1.2 nm of undoped GaN for a total thickness of ∼10.7 nm. A high resolution TEM of the heterostructure is shown in Fig 1c. A high temperature effusion cell was used to sublime elemental scandium at a temperature of approximately 1235 °C. A lattice-matched composition of $Sc_{0.18}Al_{0.82}N$ was targeted and was verified by the growth of thick (>200nm)

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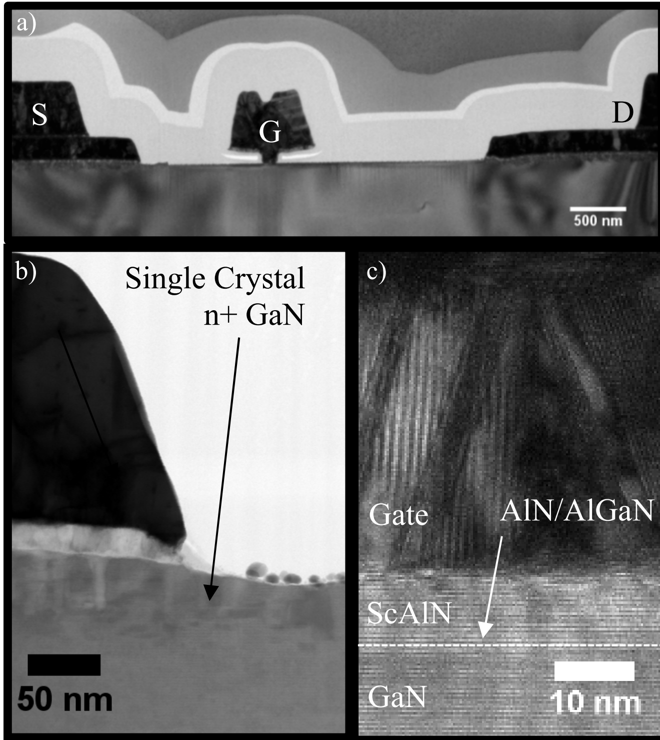

Fig. 1. (a) A device cross-section (TEM) is shown for the ScAlN/GaN HEMT. (b) A TEM image of the n+ GaN regrowth under an ohmic contact. (c) TEM image under the gate electrode showing the GaN and ScAlN layers.

calibration layers which were characterized by X-ray diffraction reciprocal space maps. The absence of relaxation in these thick samples is consistent with a composition close to lattice matching conditions. The detailed growth space will be published elsewhere as it is out of scope for this publication. MBE epitaxial regrowth of n+ GaN for contacts was performed in the same reactor.

The main fabrication challenge with this material system was the ability to make electrical contact to the 2DEG. Conventional AlGaN/GaN ohmic contact processes [7] resulted in contact resistances of ~1 $\Omega \cdot$ mm. A highly doped n^+ GaN regrowth process was used to overcome this limitation. A SiO_2 mask was deposited to protect the channel area of the device. The barrier was then etched using a chlorine plasma etch process prior to the MBE regrowth of n^+ GaN. Single crystal n+ GaN can be observed in Fig 1b. Following the regrowth process, ohmic metal was deposited (Ti/Au; 200 Å/2000) which was not annealed. This process resulted in an ohmic contact resistance as low as 0.1 $\Omega \cdot$ mm. Gates were processed using a source offset e-beam T-gate process (Ni/Au; 200 Å/3800 Å) and L_G ranged from 110 nm to 180 nm. The gate was offset 0.5 μm towards the source. The source-to-drain spacing (L_{SD}), source to-gate spacing (L_{SG}) and L_G measure to be 2.7 μm, 0.9 μm and 0.1 μm, as shown in Fig 1a. Ti/Au interconnect metal was evaporated followed by a silicon rich SiN chemical vapor deposition for passivation. The passivation was removed from the pad metal and in the field using a fluorine based dry etching process.

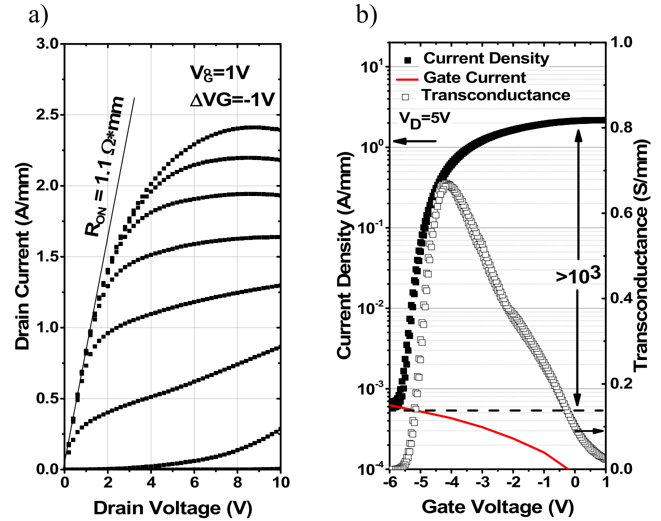

Fig. 2. a) Family of output curves for a 2 × 150 μm ScAlN/GaN HEMT. b) DC transfer characteristics are shown. I_{ON}/I_{OFF} and I_{MAX} at $V_{GS} = 1$V were measured to be >1,250 and 2.4 A/mm, respectively. Peak transconductance was measured to be 0.67 S/mm. Gate current is limiting pinch off shown in red.

III. PCM and DC Performance

TLM measurements were made using a Keithley System 450 parametric test set. TLM gaps were defined by channel length between n-plus GaN regrowth. Extracted contact resistance to the 2-DEG ranged from 0.10 $\Omega \cdot$ mm to 0.50 $\Omega \cdot$ mm across the wafer. We expect this may be a function of the barrier etch because the n+ regrowth shows very consistent sheet resistance ($\sim 50 \pm 16\Omega/\square$) across the wafer. The sheet resistance of the active area to be $236 \pm 4\Omega/\square$ via the TLM structures. We observe a 1.7% variation in sheet resistance across the 4 inch wafer.

The resulting device data is a subset of sites from the PCM data. All devices reported in this letter have 2×150 μm gate periphery. A family of output curves is shown in Fig 2a. The gate bias was swept starting with $V_G = 1$V to $V_G = -6$V with a voltage step of -1 V. A low on-resistance (R_{ON}) of 1.1 $\Omega \cdot$ mm was measured up to $V_G = 1$V and $V_D = 0.02$V. Forward and reverse sweeps of the transfer characteristics are shown in Fig 2b. We observe very little hysteresis after the silicon rich SiN [23] (index of refraction = 2.2) was deposited. DC performance prior to passivation was performed on a curve tracer and not recorded, but significant hysteresis was observed. This data was taken with the drain biased at $V_D = 5$V. A maximum current density was measured to be 2.4 A/mm. The I_{ON}/I_{OFF} ratio was measured to be $>10^3$. The relatively low I_{ON}/I_{OFF} ratio was due to high leakage current into a Schottky gate electrode. The red line in Fig 2b. shows the gate current for this device. An impressive peak transconductance of 0.67 S/mm was measured owing to the low contact resistance, thin barrier, short gate length and high charge density. Average values of maximum drain current (I_{DMAX}) and peak transconductance at $V_G = 1$V are shown in Table 1. Fig 2. demonstrates achieved device performance with optimal low contact resistance as compared with average wafer-scale results reported in Table 1.

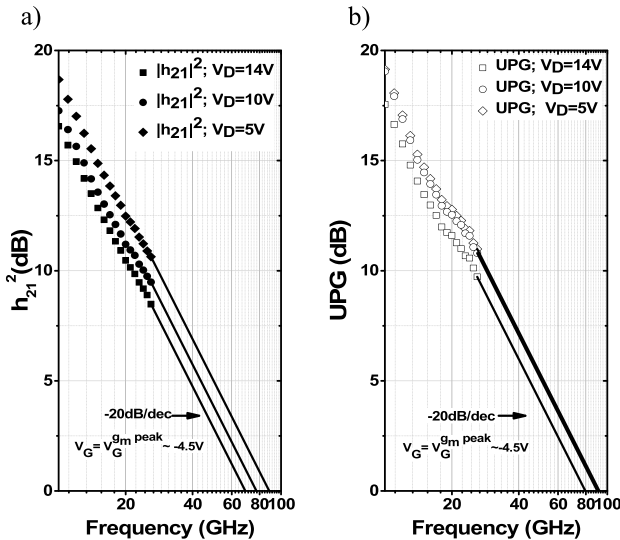

Fig. 3. Extrinsic small signal RF gain (a) $|h_{21}|^2$, b) UPG) performance recorded at peak transconductance with various drain biases ($V_D = 5$V, 10V, and 14V). A gain decay of −20 dB/dec is plotted with the solid line to show $f_T/f_{MAX,UPG}$ extrapolation.

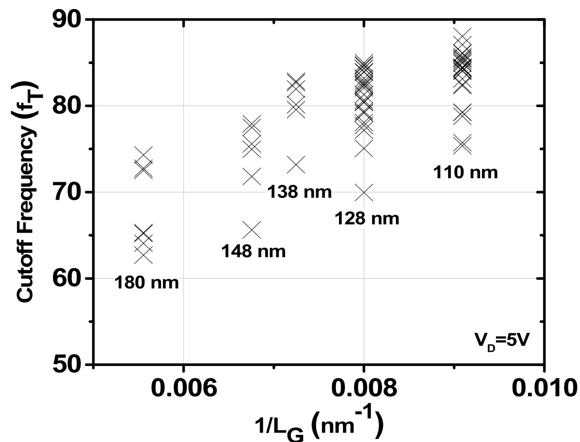

Fig. 4. Cutoff frequency (f_T) is plotted a function of $1/L_G$.

IV. RF Performance

Fig 3. shows the extrinsic small signal current gain ($|h_{21}|^2$) and unilateral power gain (UPG) for the same device measured at multiple drain biases ($V_D = 5$V, 10V, and 14V). We observe a reduction in f_T partially due to short channel effects at higher drain biases. This can be observed in Fig 2a. where the output conductance becomes appreciable with higher gate to drain biases.

Cutoff frequency is plotted as a function of $1/L_G$ in Fig 4 [24]. An increase in the frequency response is observed with shrinking gate length as expected. It should be noted that only one gate length was measured for each electron beam lithography dose. We expect an approximate 2% variation of gate length for our 140 nm gate process. We do observe a change in contact resistance across the wafer as noted, which affects the source resistance and therefore gain of the transistor. We anticipate this attributing to the significant variance in the cutoff frequency.

TABLE I

The Mean and Standard Deviation of the DC and RF Performance Is Reported for $n = 75$ Devices With Multiple Gate Lengths

L_G (nm)	110 nm	125 nm	138 nm	148 nm	180 nm
n	25	27	6	6	7
I_{DMAX} (A/mm) V_G=1V	1.96 ± 0.14 A/mm	1.90 ± 0.16 A/mm	1.88 ± 0.17 A/mm	1.89 ± 0.18 A/mm	1.88 ± 0.19 A/mm
g_m (S/mm) V_D=5V	0.62 ± .03 S/mm	0.60 ± .05 S/mm	0.61 ± .04 S/mm	0.61 ± .04 S/mm	0.61 ± .04 S/mm
f_T (GHz) V_D = 5V	83 ± 3 GHz	80 ± 6 GHz	80 ± 4 GHz	74 ± 5 GHz	69 ± 5 GHz
$f_{MAX,UPG}$ (GHz)	84 ± 7 GHz	83 ± 9 GHz	85 ± 6 GHz	79 ± 7 GHz	74 ± 8 GHz

Table 1 shows DC and RF performance for all devices measured in this data set. Seventy-five devices were measured and reported showing good correlation of device performance with respect to gate length. The g_m, f_T, and $f_{MAX,UPG}$ are reported at the gate bias which results in the highest g_m. All values shown are measured at $V_D = 5$ V.

V. Conclusions

Device functionality and performance is reported for the first time on a ScAlN/GaN heterostructure. ScAlN was grown by MBE onto a SiC substrate. An ohmic regrowth process was implemented to eliminate high contact resistances. Impressive DC characteristics show high current density (2.4 A/mm) and high transconductance (0.67 S.mm). Extrinsic small signal performance is reported for devices with gate lengths varying from 110 nm to 180 nm. A maximum f_T and f_{MAX} was reported to be 88 GHz and 91 GHz, respectively.

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