Low-Temperature, High-Performance InGaZnO Thin-Film Transistors Fabricated by Capacitive Coupled Plasma-Assistant Magnetron Sputtering

Chang Liu, Ying Sun, Houyun Qin, Yiming Liu, Song Wei, and Yi Zhao

***Abstract*— This letter demonstrates a novel approach to fabricate the high-performance a-InGaZnO thin-film transistors via using the capacitive coupled plasma-assistant magnetron sputtering with low post annealing temperature (100 °C). The influence of radio frequency generated plasma power during the a-InGaZnO deposition has been intensively investigated. With the plasma-assistant magnetron sputtering at room temperature, the best thin-film transistor exhibits a high mobility of 26.03 cm^2/Vs, a threshold voltage of 2 V, a subthreshold swing of 0.33 V/decade, and I_{ON}/I_{OFF} of more than 10^7. The proposed capacitive coupled plasma-assistant magnetron sputtering fabrication process in this letter could be a potential approach to be applied for the flexible electronic devices.**

***Index Terms*— Capacitive coupled plasma assistant magnetron sputtering, low temperature, high performance, a-IGZO, thin film transistors.**

I. Introduction

IN RECENT years, the amorphous oxide semiconductor thin film transistors (TFTs) based on indium-gallium-zinc-oxide (IGZO) have been regarded as the most promising candidates for active matrix organic light emitting display (AMOLED) pixel arrays [1] and large scale integrated circuit (LSI) [2] owing to their high performance, applicability to large-scaled substrate and compatibility with the conventional a-Si TFT. So far, magnetron sputtering is the standard technique to fabricate a-IGZO channel layer due to its advantage of low temperature process, and high quality of reproducibility. However, most of the high-performance a-IGZO TFTs deposited by magnetron sputtering require post annealing with temperature higher than 300 °C to reduce the defects formation in sputtering process [3]–[5]. A higher temperature annealing process helps to decrease the density of subgap states by reorganizing the metal oxide bonds in the semiconductor. Nevertheless, such temperature limits the application of a-IGZO for flexible electronic devices since most cost-effective flexible substrates (PET, PEN, PC, PS, PP) are deteriorated at this temperature. Therefore, it is still challenging to fabricate the a-IGZO TFT at low temperature with high performance for flexible electronic devices.

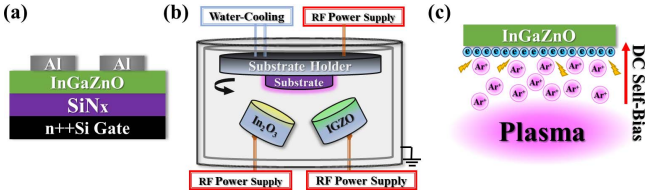

Fig. 1. (a) Schematic diagram of the a-IGZO TFT fabricated by CCP assistant magnetron sputtering. (b) Equipment diagram of CCP assistant magnetron sputtering system. (c) The principle of the RF-bias power generated bombardment.

Capacitive coupled plasma (CCP) assistant technique has been developed to effectively reduce the deposit temperature and boost the thin film quality in chemical vapor deposition (CVD) [6]–[8] and pulsed laser deposition (PLD) [9]. Up to now, there is no report about utilization of capacitive coupled plasma assistant in magnetron sputtering process to fabricate the high-performance a-IGZO transistors at low temperature. In this work, we employ a radio frequency (13.56 MHz) power supply and match network to generate the plasma at the surface of the substrate during the a-IGZO channel layer sputtering process. After the a-IGZO TFT fabrication, we use only 100°C post annealing process to get a high field effect mobility (μ_{FE}) of 26.03 cm^2/Vs, threshold voltage (V_{th}) of 2 V, subthreshold swing (SS) of 0.33 V/decade and $I_{on/off}$ larger than 10^7.

II. Experiments

The bottom-gate and top-contact structure a-IGZO TFTs are fabricated on the heavily doped silicon gate electrodes with 210-nm-thickness SiN_x gate insulators (low pressure chemical vapor deposited). The a-IGZO layers are carried out in the customized CCP assistant magnetron sputtering system (PVD Products Co. Ltd) which is schematically illustrated in Figure 1(b). The system is pumped to 1×10^{-7} Torr prior to introducing 7% O_2 mixed Ar gas at the chamber pressure of 5×10^{-3} Torr for sputtering a-IGZO layers. The 30 nm a-IGZO layers have been deposited by co-sputtering $InGaZnO_4$ and In_2O_3 ceramic targets with power of 100 W and 70 W to obtain high performance In-rich IGZO TFTs [10].

Manuscript received December 26, 2018; revised January 18, 2019, January 24, 2019 and January 25, 2019; accepted January 25, 2019. Date of publication February 14, 2019; date of current version March 6, 2019. This work was supported by the National Natural Science Foundation of China under Grant 61675089. The review of this letter was arranged by Editor S. Hall. *(Corresponding author: Yi Zhao.)*

The authors are with the State Key Laboratory of Integrated Optoelectronics, Jilin University, Changchun 130012, China (e-mail: yizhao@jlu.edu.cn).

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Digital Object Identifier 10.1109/LED.2019.2896111

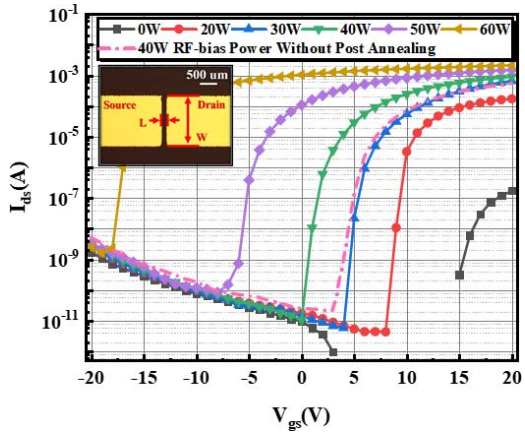

Fig. 2. I_{ds}-V_{gs} curves for a-IGZO TFTs with varies RF-bias power from 0 W to 60 W. Dashed line is the TFT with 40W RF-bias power and without post annealing. Inset is the microscopy image of the TFT.

The substrate radio frequency bias (RF-bias) power is varied from 0W to 60W during the a-IGZO layers deposition. The source and drain electrodes are thermal evaporate deposited 30-nm-thickness Al by the shadow mask process with the channel length (L) of 100 μm and width (W) of 1000 μm, respectively. The schematic diagram of a-IGZO TFT is shown in Figure 1(a). Finally, the a-IGZO TFTs are treated by contact-annealing at 100 °C in air atmosphere for 2 hours. Electrical characteristics are measured in the dark at room temperature via using Keithley 2636B Source Measure Unit. The structure and morphology are investigated by the X-ray diffraction (XRD, Rigaku TTR-III), atomic force microscope (AFM, Veeco Dimension icon), and scanning electron microscope (SEM, JEOL JSM7500F), respectively.

III. Results and Discussions

Figure 2 shows the source and drain current (I_{ds}) as the function of gate voltage (V_{gs}) of a-IGZO transistor at drain voltage of 10 V under different substrate RF-bias Power (from 0 W to 60 W). The field effect mobility (μ_{FE}) is calculated by the equation:

$$\mu_{FE} = 2L/WC_{ox}\left(\partial\sqrt{I_{ds}}/\partial V_{gs}\right)^2 \quad (1)$$

where C_{ox} is the gate capacitance per unit area. Subthreshold swing (SS) is extracted from the linear part of the log (I_{ds}) vs. V_{gs} curses via the following formula:

$$SS = \left(\partial V_{gs}/\partial \log_{10}(I_{ds})\right)_{min} \quad (2)$$

Basing on the calculated SS value, the density of the interface states (D_{it}) of the a-IGZO could be calculated by using the equation [11]:

$$D_{it} = (C_{ox}/q)\,(SSlog\,(e)\,/(kT/q) - 1) \quad (3)$$

where q, k, T is the elementary electron charge, Boltzmann constant and temperature. The threshold voltage (V_{th}) is usually extracted from the linear extrapolation of the $I_{ds}{}^{1/2}$ curve to the voltage axis. All the calculated parameters of the devices are listed in Table I and plotted in Figure 3(a). It is worthwhile to mention that if we further decrease the a-IGZO TFT post annealing temperature to room temperature (without post annealing, marked as 'wopa' device in Table I),

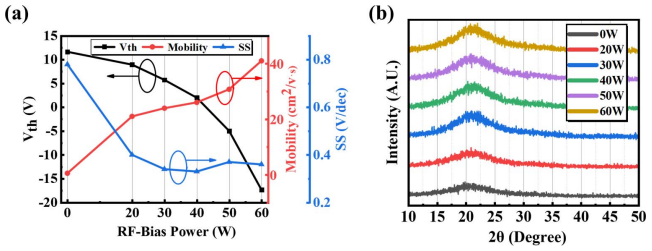

Fig. 3. (a) Mobility, threshold voltage and subthreshold swing of the TFTs as the functions of the RF-bias power. (b) The XRD pattern of IGZO thin films deposited under different RF-bias power.

TABLE I
Electrical Characteristics of a-IGZO TFTs Deposited Under Different RF-Bias Power

Power (W)	Mobility (cm^2/Vs)	SS (V/decade)	V_{th} (V)	I_{on}/I_{off}	D_{it} ($cm^{-2}eV^{-1}$)
0	0.52	0.78	11.65		2.17×10^{12}
20	20.99	0.40	8.94	3.95×10^{7}	1.02×10^{12}
30	23.95	0.34	5.74	1.14×10^{8}	8.42×10^{11}
40	26.03	0.33	2.00	8.52×10^{7}	8.12×10^{11}
50	30.74	0.37	-4.97	1.78×10^{7}	9.33×10^{11}
60	41.01	0.36	-17.34	1.31×10^{6}	9.02×10^{11}
40(wopa)	20.52	0.52	5.04	2.59×10^{7}	1.38×10^{12}

the device performance is slightly inferior than the device with 100 °C post annealing (We use 40W RF-bias TFT as the reference device). Furthermore, during the sputtering process, the highest temperature detected by the thermocouple is lower than 65 °C (Under RF-bias power of 60 W for about 10 minutes). Actually, when TFTs are operated in the AMOLED or LSI, the working temperature could not be the room temperature due to the self-heating of the devices. Hence, to further reduce the post annealing temperature is of little significance for IGZO TFT in AMOLED or LSI application. So, we choose the 100°C as the post annealing temperature which can provide a better performance and be applicable to most of the plastic substrate.

Table I represents the electrical characteristics of a-IGZO TFTs deposited under different RF-bias power. It is obvious that the electrical characteristics of the a-IGZO TFTs are critical sensitive with the RF-bias Power. The mobility is dramatically boosted with RF-bias power from 0.52 cm^2/Vs (without RF-bias) to 41.01 cm^2/Vs (60 W RF-bias). Besides, as the RF-bias power increasing, the threshold voltages are negatively shifted from 11.65 V to −17.34 V. In order to investigate the origin of the performance promotion, we perform the XRD, SEM and AFM measurement. Figure 3(b) shows the XRD patterns of IGZO films on the quartz glass with respect to the increasing RF-bias power from 0 to 60 W. All the XRD patterns of deposited IGZO films only show the halos around $2\theta \approx 21°$ which indicate that the films are in amorphous phase [12]. Two-dimensional AFM topographies and SEM images of a-IGZO films on the Si/SiN_x substrates are shown in Figure 4(a)-(l). The SEM image Figure 4(a) and AFM topography Figure 4(g) represent that the a-IGZO film without RF-bias has large amounts of protrusions with open voids, and the amounts of them are both reduced along with the RF-bias increasing. The roughness of the films is analyzed by NanoScope Analysis Software attached to the AFM instrument. The a-IGZO film without RF-bias shows a higher

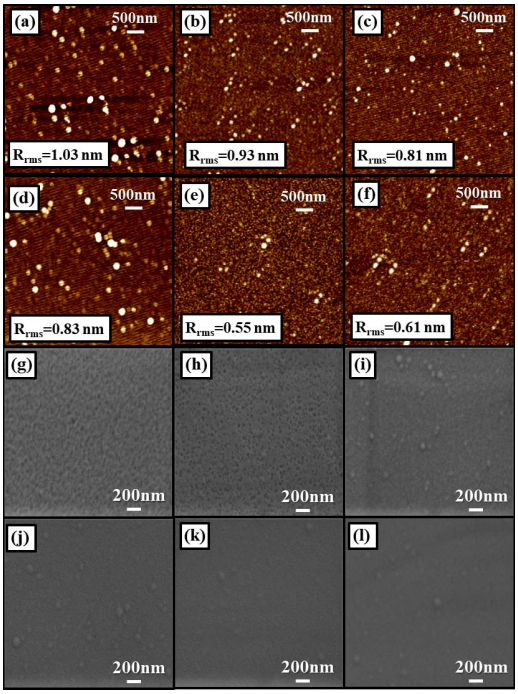

Fig. 4. AFM topographies and SEM images of a-IGZO under different RF-bias power: (a), (g) Without RF-bias; (b), (h) 20W; (c), (i) 30W; (d), (j) 40W; (e), (k) 50W; (f), (l) 60W.

roughness value of R_{rms}∼1.03 nm. As RF-bias power increases from 20 W to 60 W, the R_{rms} decreases from 0.93 nm to 0.55 nm and slightly increases to 0.61nm. The reason why the a-IGZO films get the roughness improvement can be elaborated by the following explanation. While the alternative electric field is applied on the substrate through the RF-power supply and match network, a DC self-bias potential difference builds up at the surface of the substrate. This is mainly because that electrons accumulate on the deposited surface since the mass of an electron is much smaller than that of an ion. Hence, more electrons are attracted to the substrate than positive charged ions in the same period of time. The schematic diagram is shown in Figure 1(c). Such DC potential difference accelerates the positive charged ions to collide with the atoms which are sputtered from the targets and to transfer the essential energy for the structural modification of the sputtered particles. With the higher energy transferred by the RF-bias power, the smoother thin films are formed as a result of the atoms and ions migrating more and locating in stable positions. Hence, the IGZO films with higher RF-bias power exhibit smooth and featureless surfaces with less defects such as pinholes, cracks. Besides, the flat amorphous surface feature of a-IGZO channel layer probably causes smooth contacts between the IGZO channel layers and source/drain electrodes for obtaining a high I_{on}/I_{off} larger than 10^7. Furthermore, with the higher energy from the ion's bombardment, the bonding between the channel layer and insulation layer becomes more tightly which leads to a better channel-insulator interface. In addition, such ion's bombardment process can peel off the molecules with weak bonding, hence the bonding between the metal and oxygen atoms becomes stronger and the defects are less likely to be formed even with low temperature post annealing process. This deduction is also verified by the reduction of the SS and D_{it} from $2.17 \times 10^{12}\text{cm}^{-2}\text{eV}^{-1}$, 0.78 V/decade (without RF-bias power) to $9.02 \times 10^{11}\text{cm}^{-2}\text{eV}^{-1}$, 0.36 V/decade (60 W RF-bias power), respectively. Owing to the less defect formation and better channel-insulator interface, the mobility is boosted from 0.52 cm^2/Vs to 41.01 cm^2/Vs with RF-bias power increasing. Although TFT with 60W RF-bias power can obtain a quite high mobility of 41.01 cm^2/Vs, the threshold voltage is negatively shifted to −17.34 V which indicates that the TFT almost loses its gate control ability and such TFT makes no sense for electronic device. Therefore, we have not further improved the RF-bias power. Moreover, the devices with appropriate RF-bias power show an I_{on}/I_{off} larger than 10^7 indicating that the TFTs represent good characteristics as the backplanes of AMOLED which demand quite large I_{on} and small I_{off} to obtain a fast response time and low energy consumption. A comparison between our CCP assistant a-IGZO best TFT (with 40W RF-bias power) and other low temperature process IGZO TFTs is listed in Table II which indicates that the a-IGZO TFT in our work have a high mobility, comparable SS, and large I_{on}/I_{off}.

TABLE II
THE PERFORMANCE COMPARISONS BETWEEN OUR WORK AND RELATED LOW TEMPERATURE PROCESSED IGZO TFTS

References	Temperature (°C)	Mobility (cm/Vs^2)	V_{th} (V)	SS (V/decade)	I_{on}/I_{off}
This work	100	26.03	2.00	0.33	$\sim10^7$
[13]	RT	15.30	2.80	0.28	$\sim10^7$
[14]	RT	12.00	1.40	0.20	$\sim10^8$
[15]	150	13.40	-1.50	0.13	$\sim10^6$
[16]	RT	61.50	0.25	0.61	$\sim10^5$

In summary, high-performance a-IGZO TFTs are successfully fabricated with CCP assistant magnetron sputtering with low-temperature post annealing process. The best TFT in this work exhibits a high mobility of 26.03 cm^2/Vs, V_{th} of 2 V and I_{on}/I_{off} of 10^7 demonstrating that the capacitive coupled plasma assistant magnetron sputtering fabrication process in this letter could be a potential candidate for fabricating high-performance flexible electronic devices.

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