

3.8 W/mm RF Power Density for ALD Al₂O₃-Based Two-Dimensional Hole Gas Diamond MOSFET Operating at Saturation Velocity

Shoichiro Imanishi¹, Kiyotaka Horikawa, Nobutaka Oi, Satoshi Okubo, Taisuke Kageura, Atsushi Hiraiwa, and Hiroshi Kawarada

Abstract—This letter reports the small-signal and large-signal performances at high drain voltage (V_{DS}) ranging up to 60 V for a 0.5 μm gate length two-dimensional hole gas diamond metal-oxide-semiconductor field-effect transistor with a 100-nm-thick atomic-layer-deposited Al₂O₃ film on a 11a-type polycrystalline diamond substrate with (110) preferential surfaces. This diamond FET demonstrated a cutoff frequency (f_T) of 31 GHz, indicating that its carrier velocity was reaching 1.0×10^7 cm/s for the first time in diamond. In addition, a f_T of 24 GHz was obtained at $V_{DS} = -60$ V, thus giving a $f_T \times V_{DS}$ product of 1.44 THz·V. This diamond FET is promising for use as a high-frequency transistor under high voltage conditions. Under application of a high voltage, a maximum output power density of 3.8 W/mm (the highest in diamond) with an associated gain and power added efficiency were 11.6 dB and 23.1% was obtained when biased at $V_{DS} = -50$ V using a load-pull system at 1 GHz.

Index Terms—Diamond, high frequency, high voltage, MOSFET, output power.

I. INTRODUCTION

THE cutoff frequency of a transistor is governed by its carrier velocity and carrier transport length [1]. Carrier mobility is not a crucial factor when the transistor is operating near the saturation velocity that is obtained under high electric fields. Hydrogen-terminated (C-H) diamond with a two-dimensional hole gas (2DHG) is promising as a surface channel field-effect transistor (FET) material [2] for high-frequency and high-power transistors due to high breakdown electric fields and highest thermal conductivity. Traditionally, high-frequency diamond FETs have been fabricated using a self-aligned gate process that was customized for C-H diamond [3], [4] and many groups reported excellent high-frequency performance for these diamond FETs. Fig. 1 summarizes the cutoff frequency (f_T) as a function

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The authors are with the Faculty of Science and Engineering, with the Institute of Nano-Science and Nano-Engineering, and also with the Kagami Memorial Laboratory for Material Science and Technology, Waseda University, Shinjuku, Japan (e-mail: kawarada@waseda.jp).

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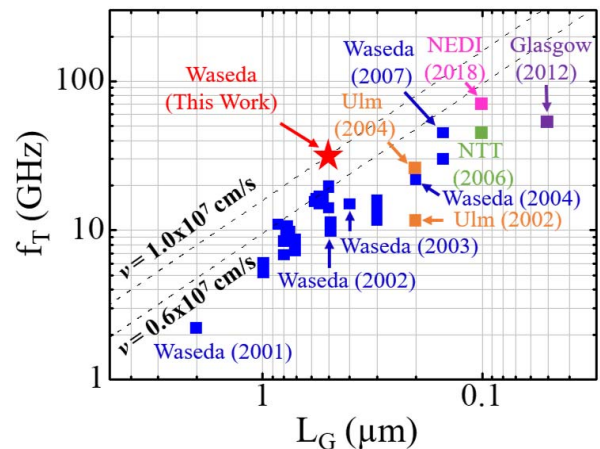


Fig. 1. Cutoff frequency as a function of gate length for diamond FETs. The two dashed lines represent carrier velocities of 0.6×10^7 cm/s and 1.0×10^7 cm/s. 4 of 33 this works devices with $L_G = 0.5 \mu\text{m}$ demonstrated the maximum f_T between 30 GHz and 31 GHz.

of gate length (L_G) that has been reported for these diamond FETs [4]–[13]. From 2001 onwards, the high-frequency performance milestones for diamond FETs include the first reported GHz operation in metal-semiconductor field-effect transistors (MESFETs) [4], metal-insulator-semiconductor field-effect transistors (MISFETs) with $f_T > 20$ GHz [8], MESFETs with $f_T = 45$ GHz, a maximum oscillation frequency (f_{max}) of 120 GHz [9], and an output power density > 2.0 W/mm [13]. The most recently reported device has $f_T = 70$ GHz [12]. However, the carrier velocities of these diamond FETs were still below 0.6×10^7 cm/s (Fig. 1) because they were operating at less than 10^5 V/cm (i.e., 10 V per 1 μm). Application of an electric field of more than 4×10^5 V/cm is required for the carrier velocity to reach the saturation velocity because the reported hole mobility of C-H diamond was approximately $100 \text{ cm}^2/\text{V}\cdot\text{s}$ [14], [15]. The breakdown voltage is relatively low at 20 V because the high-frequency diamond FETs, fabricated using a self-aligned gate process, have thin gate oxides and no passivation layers. The electric field required to reach the saturation velocity could not be applied to these FETs. The carrier velocity would approach the saturation velocity and the output power density would be improved by high-voltage operation. Recently, we reported a high average electric field [15] in metal-oxide-semiconductor field-effect transistors (MOSFETs) with thick Al₂O₃ layers acting as gate insulator [15] and passivation layers [16] that were deposited by high-temperature atomic layer deposition

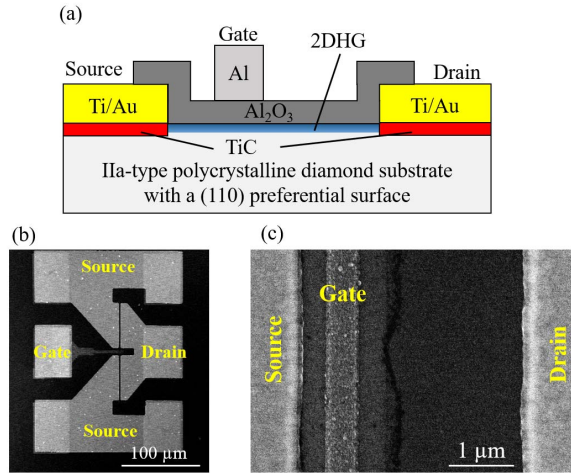


Fig. 2. (a) Cross-sectional schematic, (b) top-view SEM, and (c) enlarged image of ALD- Al_2O_3 2DHG diamond MOSFET.

(ALD) [17]. In this present work, we fabricated $0.5\text{-}\mu\text{m}$ -gate-length ALD- Al_2O_3 2DHG diamond MOSFETs with a structure that is capable of withstanding high voltage and report the small-signal and large-signal performances of these devices during high voltage operation ($|V_{\text{DS}}|$ up to 60 V).

II. DEVICE FABRICATION

A cross-sectional view of the MOSFET structure is shown in Fig. 2(a). The devices were fabricated on a IIa-type polycrystalline diamond substrate with (110) preferential surfaces [18]. The devices that were fabricated on the IIa-type polycrystalline diamond substrate showed excellent DC and radio-frequency (RF) performances [9], [10], [19]. First, Ti/Au (30/100 nm) structure was evaporated and lifted off to act as the source and drain electrodes and TiC layers were formed at the interface between the diamond film and Ti by annealing for ohmic contact formation [20]. Second, the diamond surface was hydrogen-terminated by remote plasma processing. Third, the active devices were isolated through an O_2 treatment. Subsequently, an Al_2O_3 film (100 nm thick) was deposited by high-temperature ALD to act as the gate insulator and passivation layer. The deposition temperature was 450° and the oxidant was H_2O . The gate electrode was defined using electron beam lithography and an Al (100 nm) layer was evaporated and lifted off. In this work, the source-gate length (L_{SG}), the gate length (L_{G}) and the gate width (W_{G}) were fixed at 0.5, 0.5 and $100\ \mu\text{m}$, respectively, while the gate-drain length (L_{GD}) ranged from 1 to $3\ \mu\text{m}$. Fig. 2(b) and (c) show the top-view and the enlarged image of fabricated ALD- Al_2O_3 2DHG diamond MOSFET.

III. RESULTS AND DISCUSSION

Fig. 3 shows the drain current-voltage characteristics of a diamond MOSFET with $L_{\text{SG}} = 0.5\ \mu\text{m}$, $L_{\text{G}} = 0.5\ \mu\text{m}$, $L_{\text{GD}} = 1\ \mu\text{m}$ and $W_{\text{G}} = 100\ \mu\text{m}$. The drain current density (I_{DS}) was $-730\ \text{mA/mm}$ at $V_{\text{GS}} = -20\ \text{V}$ and $V_{\text{DS}} = -40\ \text{V}$, while the transconductance (g_{m}) was as high as $15\ \text{mS/mm}$ at $V_{\text{DS}} = -40\ \text{V}$ with $-20 \leq V_{\text{GS}} \leq 16\ \text{V}$ and the lowest ON-resistance (R_{on}) was $30\ \Omega\ \text{mm}$. The drain current performance degradation that occurs at higher drain current and voltage due to temperature-dependent carrier transport was not observed around $V_{\text{DS}} = -40\ \text{V}$ because of the high heat dissipation that occurred as a result of the high thermal conductivity of diamond.

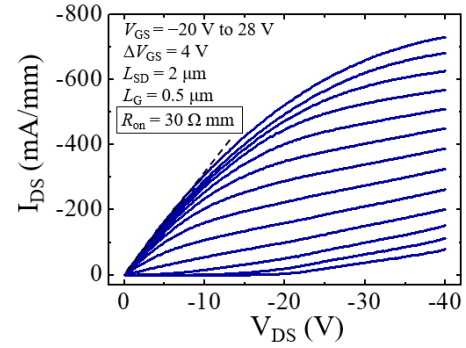


Fig. 3. $I_{\text{DS}}-V_{\text{DS}}$ characteristics of device with $L_{\text{SG}} = 0.5\ \mu\text{m}$, $L_{\text{G}} = 0.5\ \mu\text{m}$, $L_{\text{GD}} = 1\ \mu\text{m}$ and $W_{\text{G}} = 100\ \mu\text{m}$. The maximum I_{DS} was $730\ \text{mA/mm}$ at $V_{\text{GS}} = -20\ \text{V}$ and $V_{\text{DS}} = -40\ \text{V}$.

S-parameters were measured on-wafer over the range from 1 GHz to 40 GHz using an Agilent 8722ES vector network analyzer. Prior to measurement of the S-parameters, calibration was performed using the short-open-load-thru method and an impedance standard substrate to determine the reference planes for the probe tips. f_{T} and f_{max} were defined as the frequencies at which the current gain ($|H_{21}|^2$) and the extrapolation of Mason's unilateral power gain (U) were equal to unity, respectively. The f_{T} and f_{max} were not de-embedded and included the parasitic pad capacitance and inductance. To investigate the dependence of both f_{T} and f_{max} on bias voltage, the small-signal performances were evaluated at various bias points. Fig. 4(a) and (b) show the extrinsic f_{T} and f_{max} contour plots against the drain current-voltage characteristics, respectively, over a wide drain voltage range ($10\ \text{V} \leq |V_{\text{DS}}| \leq 60\ \text{V}$) for a device with $L_{\text{SG}} = 0.5\ \mu\text{m}$, $L_{\text{G}} = 0.5\ \mu\text{m}$, $L_{\text{GD}} = 3\ \mu\text{m}$ and $W_{\text{G}} = 100\ \mu\text{m}$. From Fig. 4(a) and (b), both f_{T} and f_{max} tend to be higher for a lower I_{DS} and a higher V_{DS} . The positive V_{DS} dependence of f_{T} and f_{max} indicates carrier velocity increases until V_{DS} of 30–40 V and saturates above that. The maximum f_{T} of 31 GHz in this device was found at $V_{\text{GS}} = 28\ \text{V}$ and $V_{\text{DS}} = -30\ \text{V}$ (see Fig. 4(a) and (c)). The f_{max} continues increasing as V_{DS} increases due to mitigation of the Miller effect. The maximum f_{max} of 35 GHz in this device was found at $V_{\text{GS}} = 32\ \text{V}$ and $V_{\text{DS}} = -60\ \text{V}$ (see Fig. 4(b) and (d)), while the device also demonstrated a f_{T} of 24 GHz at $V_{\text{DS}} = -60\ \text{V}$, thus giving an $f_{\text{T}} \times V_{\text{DS}}$ product of 1.44 THz-V, which is used as a figure of merit to evaluate high-frequency performance under high voltage operating conditions [21], and is the highest reported value in diamond FETs. Overall the average of the maximum f_{T} for 33 devices with $L_{\text{G}} = 0.5\ \mu\text{m}$ was 25.6 GHz and 4 of 33 devices demonstrated the maximum f_{T} between 30 GHz and 31 GHz (see Fig. 1). When the f_{T} was 31 GHz, the carrier velocity (v) that was calculated from the simple equation $f_{\text{T}} = v/2\pi L_{\text{G}}$ was $1 \times 10^7\ \text{cm/s}$, which is reaching the saturation carrier velocity of $1 \times 10^7\ \text{cm/s}$ for the first time in diamond microwave FETs shown in Fig. 1. The carrier velocity of the device in this work is 40% higher than those reported in the diamond FETs so far. A sufficiently high electric field can be applied to reach this saturation velocity because the device structure is capable of withstanding high electric fields.

The large-signal performance was evaluated on-wafer using a load pull system at 1 GHz. The source and load impedances were tuned to give maximum gain and maximum output power, respectively. Fig. 5(a) shows the large-signal performance for device A with $L_{\text{SG}} = 0.5\ \mu\text{m}$, $L_{\text{G}} = 0.5\ \mu\text{m}$,

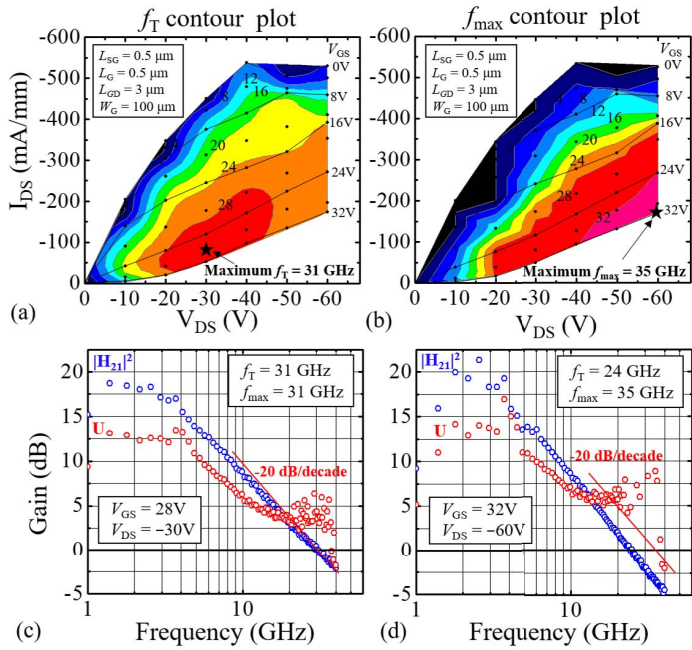


Fig. 4. (a) f_T and (b) f_{max} contour plots against the drain current-voltage characteristics of a device with $L_{SG} = 0.5 \mu\text{m}$, $L_G = 0.5 \mu\text{m}$, $L_{GD} = 3 \mu\text{m}$, and $W_G = 100 \mu\text{m}$. (c), (d) Small-signal performances that gave the maximum extrinsic f_T and f_{max} . The maximum f_T was 31 GHz at $V_{GS} = 28$ V and $V_{DS} = -30$ V and the maximum f_{max} was 35 GHz at $V_{GS} = 32$ V and $V_{DS} = -60$ V.

$L_{GD} = 2 \mu\text{m}$ and $W_G = 100 \mu\text{m}$. The bias point for A-class operation was at $V_{DS} = -50$ V, $V_{GS} = 12$ V and $I_{DS} = -405$ mA/mm. The maximum output power density reached 3.8 W/mm, which is the highest reported value for diamond FETs. The associated gain and power added efficiency (PAE) were 11.6 dB and 23.1%, respectively. In the same bias condition ($V_{DS} = -50$ V and $V_{GS} = 12$ V), device B with $L_{SG} = 0.5 \mu\text{m}$, $L_G = 0.5 \mu\text{m}$, $L_{GD} = 3 \mu\text{m}$ and $W_G = 100 \mu\text{m}$ demonstrated the following characteristics: the maximum output power density of 3.8 W/mm, the associated gain of 9.6 dB and the associated PAE of 23.8 % (see Fig. 5(b)). Under application of $V_{DS} = -40$ V and $V_{GS} = 8$ V, the device A demonstrated the maximum output power density of 3.1 W/mm. In addition, for device C with $L_{SG} = 0.5 \mu\text{m}$, $L_G = 0.5 \mu\text{m}$, $L_{GD} = 1 \mu\text{m}$ and $W_G = 100 \mu\text{m}$, the large-signal performance was evaluated at V_{DS} of -20 V to -40 V. The maximum output power density was 1.0, 1.9 and 2.8 W/mm at V_{DS} of -20 , -30 and -40 V, respectively. Those data are plotted in Fig. 5(c). To enable comparison of the output power densities of the diamond FETs used in this work with those of various solid-state devices reported to date, Fig. 5(c) shows the output power densities during RF operation for various solid-state devices as a function of V_{DS} [7], [10], [13], [22]–[24]. The application of a high V_{DS} such as 50 V that applied to SiC and GaN devices was not previously realized because conventional diamond FETs break down at less than 20 V [12]. In this work, the large-signal characteristics of the ALD- Al_2O_3 diamond FET were evaluated at a drain voltage of more than 30 V for the first time and the device demonstrated power density of 3.8 W/mm at $V_{DS} = -50$ V, which is the highest ever reported for diamond FETs. As opposed to decreasing gain and PAE of large-signal performance when increasing frequency, high output power density at 10 GHz can be expected since the mason's unilateral

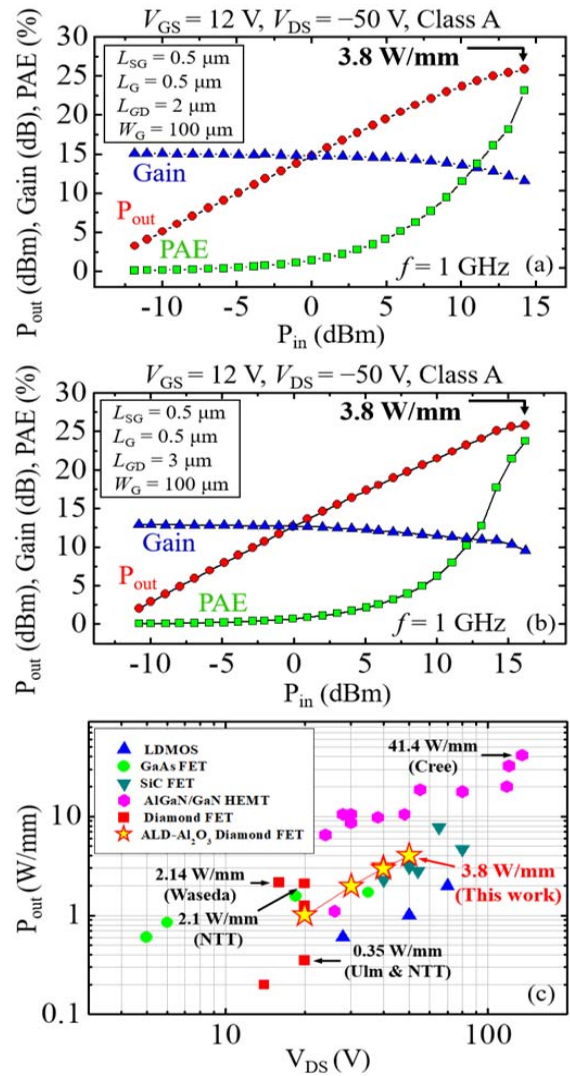


Fig. 5. (a) Large-signal performance of device A with $L_{SG} = 0.5 \mu\text{m}$, $L_G = 0.5 \mu\text{m}$, $L_{GD} = 2 \mu\text{m}$, and $W_G = 100 \mu\text{m}$. The output power density was 3.8 W/mm at $V_{DS} = -50$ V. (b) Large-signal performance of device B with $L_{SG} = 0.5 \mu\text{m}$, $L_G = 0.5 \mu\text{m}$, $L_{GD} = 3 \mu\text{m}$, and $W_G = 100 \mu\text{m}$. The output power density was 3.8 W/mm at $V_{DS} = -50$ V. (c) Output power density during RF operation for various solid devices as a function of V_{DS} .

power gain at this frequency is approximately 6 dB. Higher voltage application can furthermore enhance the output power density of the diamond FETs.

IV. CONCLUSION

We have reported the small-signal and large-signal performance characteristics of ALD- Al_2O_3 diamond FETs at $|V_{DS}|$ of up to 60 V for the first time. The small-signal performance shows a f_T of 31 GHz for $L_G = 0.5 \mu\text{m}$, thus indicating that the carrier velocity is approaching the saturation velocity of 1×10^7 cm/s; this carrier velocity is the highest reported value for diamond FETs. Large-signal characteristics evaluation at a drain voltage of more than 30 V was demonstrated for the first time for these diamond FETs and the device output 3.8 W/mm, which is the highest for p-channel FETs. Diamond FETs are the most suitable for high power microwave transistors next to AlGaIn/GaN HEMTs. Complementary S-class amplifiers might be feasible with GaN n-FETs and diamond p-FETs on diamond substrates.

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