Pulsed Large Signal RF Performance of Field-Plated Ga_2O_3 MOSFETs

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***Abstract*— Comparison between pulsed and CW large signal RF performance of field-plated β-Ga_2O_3 MOSFETs has been reported. Reduced self-heating when pulse resulted in a power added efficiency of 12%, drain efficiency of 22.4%, output power density of 0.13 W/mm, and maximum gain up to 4.8 dB at 1 GHz for a 2-μm gate length device. Increased power dissipation for higher V_{DS} and I_{DS} resulted in a degradation in performance, which, thermal simulation showed, could be entirely explained by self-heating. Buffer and surface trapping contributions have been evaluated using gate and drain lag measurements, showing minimal impact on device performance. These results suggest that β-Ga_2O_3 is a good candidate for future RF applications.**

***Index Terms*— Ga_2O_3 MOSFET, large signal RF, pulsed RF, power added efficiency (PAE), pulsed IV.**

I. Introduction

THE material of β-Ga_2O_3 with a bandgap of 4.9 eV and large electric breakdown strength of 8 MVcm^{-1} has garnered great interest in the power conversion community; however, there are also opportunities for RF applications [1], [2]. Ga_2O_3 features a Baliga's figure of merit (BFOM), which is based on the mobility and bandgap, more than 10× higher than for SiC and 4× higher than for GaN [3]. High breakdown voltages up to 755 V with a high drain current on/off ratio of 10^9 have been demonstrated for lateral Ga_2O_3 transistors [4]. Johnson's figure of merit (saturation velocity times critical electric field product, $vsat{\cdot}Ec$) for high frequency devices is very much comparable to GaN [1], [5].

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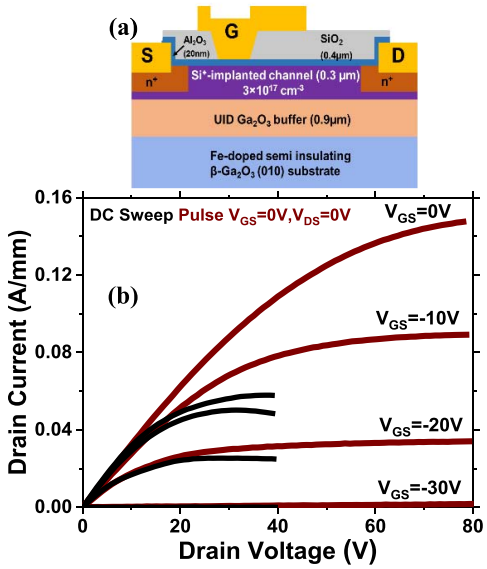

Fig. 1. (a) Schematic cross-section of the field-plated MOSFET used in this study. (b) DC output characteristics with V_{GS} from −30 V to 0V and V_{DS} up to 40 V, with droop observed due to self-heating at higher drain bias. Pulsed IV from a quiescent bias of $V_{GS} = V_{DS} = 0$ V up to $V_{DS} = 80$ V with 1 μs pulse length and 1 ms period is overlaid.

Green *et al.* [6] demonstrated RF performance with an output power density (P_{out}) of 0.23 W/mm along with a power added efficiency (PAE) of 6.3% at 800 MHz. These initial results show promising future for RF electronics based on Ga_2O_3, but they also demonstrate the challenges this material system has in terms of thermal management due to its low thermal conductivity. Here we calculate the thermal resistance of Ga_2O_3 metal-oxide-semiconductor field-effect transistors (MOSFETs) based on a combination of device and thermal simulations. This work demonstrates a comparison of CW and pulsed large signal RF operation for Ga_2O_3 MOSFETs and the benefit of pulsed IV for circumventing device heating. We also demonstrate that neither surface nor buffer traps have any sizable impact on device performance.

II. Sample Details

Devices used in this study were grown on an Fe-doped semi-insulating β-Ga_2O_3 (010) substrate by ozone MBE with a 1.2 μm unintentionally-doped (UID) epilayer as the starting material [7], [8]. The MOSFET channel was defined by selective-area Si ion implants at multiple energies to form a 0.3-μm-deep box-like profile with a plateau concentration of 3×10^{17} cm^{-3}. Source and drain contacts were also doped

by Si ion implantation (5×10^{19} cm^{-3}). Capless implant activation annealing was performed at 950°C for 30 min in N_2 ambient. A metal stack of Ti (20 nm)/Au (230 nm), which was annealed at 470°C for 1 min, was used as the ohmic electrode. A 20 nm Al_2O_3 gate dielectric was then deposited at 250°C by plasma atomic layer deposition, on top of which a 0.4 μm SiO_2 dielectric was formed by chemical vapor deposition. CF_4 RIE gate recess through the SiO_2 was followed by depositions of Ti (3 nm)/Pt (12 nm)/Au (280 nm) for the gate electrode and Ti/Au for a gate-connected field plate. The device had a gate length of 2 μm, gate width of 500 μm, gate-source spacing of 5 μm, gate-drain spacing of 15 μm, and field plate length of 1 μm [4]. The cross-section of the device is shown in Fig. 1(a).

III. Results and Discussion

DC output characteristics are shown in Fig. 1(b) with a maximum I_{DS} of 58 mA/mm, a threshold voltage (V_{TH}) of −28 V, and off-state leakage on the order of 10^{-9} A/mm. Pulsed measurements with 1 μs pulse length and 1 ms period from a quiescent point of $V_{GS} = 0$ V and $V_{DS} = 0$ V, which corresponds to a stress-free steady state, show excellent performance with the maximum I_{DS} increasing to 150 mA/mm. Pulsed operation allowed DC measurements to be extended from $V_{DS} = 40$ V up to $V_{DS} = 80$ V without inducing thermal breakdown.

To evaluate the reduction in channel temperature for pulsed versus steady state operation, the transient thermal response was simulated using a 3–D ANSYS finite element model, with dimensions matching the measured device and channel Joule heating distribution obtained from a drift-diffusion model simulated using Silvaco ATLAS [9]. In the thermal simulation anisotropic thermal conductivities of $23.4 \times (300/T)^{1.27}$ W/m · K and $13.7 \times (300/T)^{1.12}$ W/m · K in the out-of-plane [010] direction and in-plane [001] direction, respectively, were used [10]. Thermal conductivity values of 3 W/m · K, 1 W/m · K and 315 W/m · K were applied to the Al_2O_3, SiO_2 and gold pad layers respectively; standard bulk specific heat capacity and density values were used for all materials. An isothermal boundary condition was applied to the back of the 600-μm-thick Ga_2O_3 substrate. Thermal simulation results shown in Fig. 2 illustrate that the peak channel temperature is predicted to reach 39°C after a duration of 1 μs and then rise to 325°C after about 100 ms at a constant power dissipation (P_{diss}) of 2.4 W/mm, which corresponds to the DC condition of $V_{DS} = 40$ V and $I_{DS} = 0.058$ A/mm in Fig. 1. For the pulsed IV measurement, the worst-case temperature rise at $V_{DS} = 80$ V and $I_{DS} = 150$ mA/mm was about 200°C. The self-heating induces the severe thermal droop observed in the DC IV curve of Fig.1.

Thermally induced current slump could therefore be mitigated by using short pulse lengths; however, traps in the devices could then potentially result in significant current collapse and knee walkout due to surface or buffer traps, with well-known examples for GaN high electron mobility transistors [11]–[13]. The temporal charging of these traps will be a function of varying gate and drain potentials, with charge trapping under the gate leading to a threshold shift and trapping in the gate-source or gate-drain region a drop in transconductance. Using 1 μs pulse length and 1 ms period for gate lag ($V_{GS} = -50$ V, $V_{DS} = 0$ V) and drain lag ($V_{GS} = -50$ V, $V_{DS} = 80$ V) quiescent points, almost no drop in

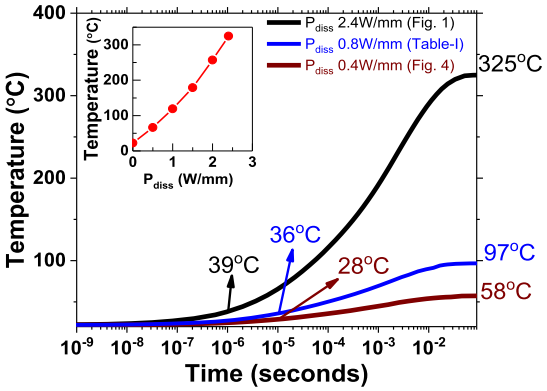

Fig. 2. Single pulse thermal simulation showing the transient peak channel temperature at $V_{DS} = 40$V and power dissipations of 2.4, 0.8 and 0.4 W/mm at 25°C ambient temperature. Durations of 1 μs and 10 μs that match the pulsed IV and pulsed RF measurement conditions, respectively, are highlighted. The simulated steady state peak channel temperature rise versus power dissipation is shown as an inset.

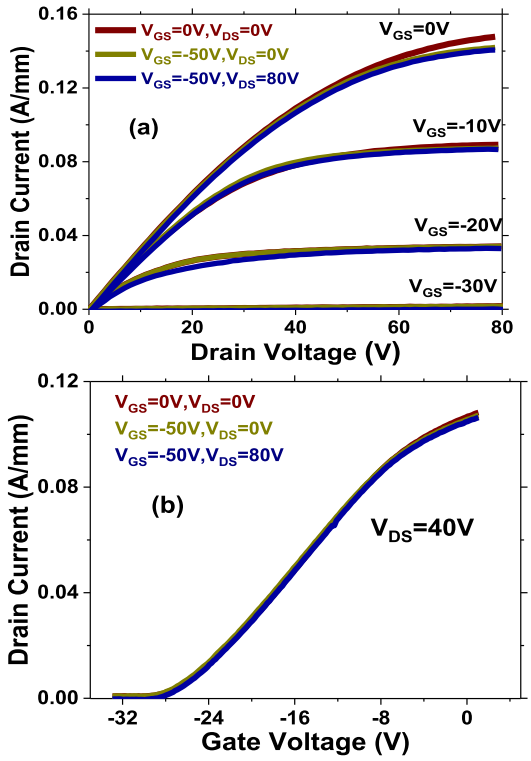

Fig. 3. (a) Gate and drain lag measurements comparing different quiescent biases, with 1 μs pulse length and 1 ms pulse period: unstressed (brown line) $V_{GS} = 0$ V, $V_{DS} = 0$ V; gate lag (green line) $V_{GS} = -50$ V, $V_{DS} = 0$ V; and drain lag (blue line) $V_{GS} = -50$ V, $V_{DS} = 80$ V. (b) Gate and drain lag measurements comparing different quiescent biases, showing almost no shift in threshold voltage and no drop in transconductance at $V_{DS} = 40$ V.

output conductance was observed, as illustrated in Fig. 3(a). This has been further confirmed by using the same quiescent bias conditions and measuring transfer characteristics at $V_{DS} = 40$ V, under which the device showed almost no shift in V_{TH} and minimal drop in transconductance as shown in Fig. 3(b). Hence there is no significant trapping in the gate dielectric or Ga_2O_3 bulk and only minimal surface trapping for these devices. Trapping is a major challenge in the device community and these results are encouraging given this is

TABLE I
COMPARISON OF CW AND PULSE LARGE SIGNAL MEASUREMENTS PERFORMED AT TWO DIFFERENT OPERATING POWER LEVELS OF 0.4 W/mm AND 0.8 W/mm. LARGER DIFFERENCES IN PERFORMANCE BETWEEN CW AND PULSED MODES CAN BEEN SEEN WITH INCREASING OPERATING POWER

Parameters	Operating condition 0.4 W/mm (I_{DS} = 5 mA, V_{DS} = 40 V)		Operating condition 0.8 W/mm (I_{DS} = 10 mA, V_{DS} = 40 V)	
	25°C		25°C	
	CW	Pulse	CW	Pulse
P_{out} (dBm)	17.42	18.28	17.63	19.52
P_{out} (W/mm)	0.11	0.13	0.11	0.17
Drain Eff (%)	19.56	22.40	13.83	17.04
PAE (%)	9.09	12.01	3.23	6.85
Max Gain (dB)	4.17	4.81	2.08	3.68
Channel temperature (°C)	58	28	97	36

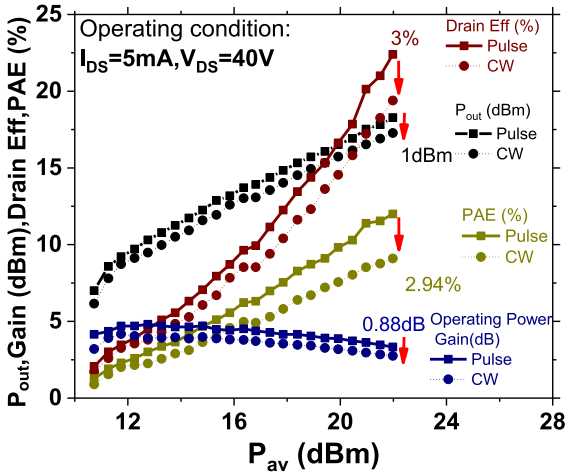

Fig. 4. Pulsed and CW large signal measurements at 1 GHz with input available power sweep up to 22 dBm, measured at V_{DS} = 40 V with I_{DS} = 5mA.

a relatively new technology with process and material still evolving.

Large signal CW and pulsed RF measurements have been performed based on the stable pulse performance. A large signal measurement system based on a VTD SWAP-X402 receiver has been used. A high-speed FET switch modulates the drain bias during DC while an external modulator with high-speed RF switches has been used to provide the RF pulse [14]. This provides an ability to independently switch the RF and DC drain bias between CW and pulse without making any changes to the sampling regime. At V_{DS} = 40 V and I_{DS} = 5mA (0.4 W/mm power dissipation) for 10 μs duration pulsed RF, a maximum P_{out} of 0.13 W/mm with a PAE of 12% and a drain efficiency up to 22.4% along with a maximum gain of 4.8 dB were obtained at 1 GHz as shown in Fig. 4. By comparison, CW large signal performance dropped to a peak P_{out} of 0.11 W/mm with 19.5% drain efficiency and 9.1% PAE as is also shown in Fig. 4. The difference in RF performance is due to self-heating: based on the thermal resistance extracted from simulation (Fig. 2), the predicted temperature is 58°C during CW RF and 28°C for pulsed RF. The forward available power (P_{av}) rather than input power into the device (P_{in}) is plotted since the high reflection at the input in these long gate length devices makes P_{in} noisy and error prone. Rollover in the PAE and degradation in gain beyond an available power of 22 dBm were the reasons to limit the sweep at 22 dBm. These PAE and drain efficiency values exceed those reported by Green *et al.* for CW RF measurements at 800 MHz [6].

Measurements of CW and pulsed RF at higher operating power and ambient temperature have been performed as is summarized in Table I, together with the calculated channel temperatures at the RF pulse length of 10 μs and for CW. In all cases CW operation showed a lower gain, PAE, drain efficiency and P_{out} than pulsed operation. Despite the fact that the load-pull was optimized for maximum power, meaning that the load is somewhat different in each case, there is a fairly consistent drop in performance with increasing channel temperature. Comparisons of CW and pulsed measurements at V_{DS} = 40 V and 25°C but different bias currents (resulting in power dissipation increasing from 0.4 W/mm to 0.8 W/mm) showed that the difference in P_{out} increased from 1.01 to 1.89 dBm and the gain difference increased from 0.64 to 1.6 dB, but the change in PAE was similar at 2.92% and 3.62%. RF measurements performed at an elevated temperature of 100°C further degraded the performance for CW and pulsed modes with the device not showing any gain consistent with a thermal origin (not shown here).

These results demonstrate good quality epitaxy and surface treatment/passivation. We note that the RF performance is constrained by the long gate length, and that scaling will result in further improvements in P_{out} and gain. These results show a promising future for RF electronics based on Ga_2O_3 as well as the need for better heat dissipation during DC or CW operation.

IV. CONCLUSION

β-Ga_2O_3 MOSFETs have been evaluated with pulsed IV and show minimal dispersion during gate and drain lag measurements. Pulsed large signal RF measurements show record PAE of 12% at 1 GHz for a 2μm gate length and 22 μm source-drain spacing. These values can be further improved by scaling of the devices and improved heat management concepts.

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REFERENCES

[1] M. Higashiwaki and G. H. Jessen, "Guest editorial: The dawn of gallium oxide microelectronics," *Appl. Phys. Lett.*, vol. 112, no. 6, p. 060401, 2018, doi: 10.1063/1.5017845.

[2] S. J. Pearton, J. Yang, P. H. Cary, IV, F. Ren, J. Kim, M. J. Tadjer, and M. A. Mastro, "A review of Ga_2O_3 materials, processing, and devices," *Appl. Phys. Rev.*, vol. 5, no. 1, p. 011301, 2018, doi: 10.1063/1.5006941.

[3] B. J. Baliga, "Semiconductors for high-voltage, vertical channel field-effect transistors," *J. Appl. Phys.*, vol. 53, no. 3, pp. 1759–1764, 1982, doi: 10.1063/1.331646.

[4] M. H. Wong, K. Sasaki, A. Kuramata, S. Yamakoshi, and M. Higashiwaki, "Field-plated Ga_2O_3 MOSFETs with a breakdown voltage of over 750 V," *IEEE Electron Device Lett.*, vol. 37, no. 2, pp. 212–215, Feb. 2016, doi: 10.1109/led.2015.2512279.

[5] E. Johnson, "Physical limitations on frequency and power parameters of transistors," in *Proc. IRE Int. Conv. Rec.*, Mar. 1966, pp. 27–34, doi: 10.1109/IRECON.1965.1147520.

[6] A. J. Green, K. D. Chabak, M. Baldini, N. Moser, R. Gilbert, R. C. Fitch, G. Wagner, Z. Galazka, J. McCandless, A. Crespo, K. Leedy, and G. H. Jessen, "β -Ga2O3 MOSFETs for radio frequency operation," *IEEE Electron Device Lett.*, vol. 38, no. 6, pp. 790–793, Jun. 2017, doi: 10.1109/led.2017.2694805.

[7] K. Sasaki, M. Higashiwaki, A. Kuramata, T. Masui, and S. Yamakoshi, "Growth temperature dependences of structural and electrical properties of Ga_2O_3 epitaxial films grown on β-Ga_2O_3 (010) substrates by molecular beam epitaxy," *J. Crystal Growth*, vol. 392, pp. 30–33, Apr. 2014, doi: 10.1016/j.jcrysgro.2014.02.002.

[8] K. Sasaki, A. Kuramata, T. Masui, E. G. Víllora, K. Shimamura, and S. Yamakoshi, "Device-quality β-Ga_2O_3 epitaxial films fabricated by ozone molecular beam epitaxy," *Appl. Phys. Express*, vol. 5, no. 3, p. 035502, 2012, doi: 10.1143/apex.5.035502.

[9] [Online]. Available: www.silvaco.com

[10] Z. Guo, A. Verma, X. Wu, F. Sun, A. Hickman, T. Masui, A. Kuramata, M. Higashiwaki, D. Jena, and T. Luo, "Anisotropic thermal conductivity in single crystal β-gallium oxide," *Appl. Phys. Lett.*, vol. 106, no. 11, p. 111909, 2015, doi: 10.1063/1.4916078.

[11] S. C. Binari, K. Ikossi, J. A. Roussos, W. Kruppa, D. Park, H. B. Dietrich, D. D. Koleske, A. E. Wickenden, and R. L. Henry, "Trapping effects and microwave power performance in AlGaN/GaN HEMTs," *IEEE Trans. Electron Devices*, vol. 48, no. 3, pp. 465–471, Mar. 2001, doi: 10.1109/16.906437.

[12] S. A. Jauss, S. Schwaiger, W. Daves, S. Noll, and O. Ambacher, "Charge trapping in gate-drain access region of AlGaN/GaN MIS-HEMTs after drain stress," in *Proc. 45th Eur. Solid State Device Res. Conf. (ESSDERC)*, Sep. 2015, pp. 56–59, doi: 10.1109/ESSDERC.2015.7324712.

[13] C. Roff, J. Benedikt, P. J. Tasker, D. J. Wallis, K. P. Hilton, J. O. Maclean, D. G. Hayes, M. J. Uren, and T. Martin, "Analysis of DC–RF dispersion in AlGaN/GaN HFETs using RF waveform engineering," *IEEE Trans. Electron Devices*, vol. 56, no. 1, pp. 13–19, Jan. 2009, doi: 10.1109/ted.2008.2008674.

[14] M. A. Casbon, P. J. Tasker, and J. Benedikt, "Waveform engineering beyond the safe operating region: Fully active harmonic load pull measurements under pulsed conditions," in *Proc. IEEE Compound Semiconductor Integr. Circuit Symp. (CSICS)*, Oct. 2011, pp. 1–4, doi: 10.1109/CSICS.2011.6062435.