

One-Volt IGZO Thin-Film Transistors With Ultra-Thin, Solution-Processed Al_xO_y Gate Dielectric

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Abstract— Indium–gallium–zinc–oxide thin-film transistors (TFTs) with solution-processed, high-capacitance Al_xO_y gate dielectrics have been fabricated at room temperature. The morphology and electrical properties of the anodized, ultra-thin Al_xO_y film have been studied. Several anodization voltages were used to create the gate dielectrics and the results showed that the TFTs gated with aluminum oxide anodized at 2.3 V (~ 3 nm) exhibited the best performance. The TFTs operate at an ultra-low voltage of 1 V with a high current on/off ratio $>10^5$ and a subthreshold swing (SS) as low as 68 mV/dec, which is very close to the theoretical limit of SS at 300 K. As a result, the presented devices possess a great potential for low-power electronics.

Index Terms— Indium-gallium-zinc-oxide (IGZO) thin-film transistors (TFTs), anodized Al_xO_y , low operating voltage.

I. INTRODUCTION

INDIUM-GALLIUM-ZINC-OXIDE (IGZO) thin-film transistors (TFTs) have drawn a lot of attention since first being reported by Nomura *et al.* [1]. Due to their excellent electrical properties, such as high field-effect mobility, good uniformity and low temperature processability, such TFTs have shown potential in a wide range of electronic applications [1]–[3].

For applications such as displays, sensors and battery-powered electronics, it is highly desirable for TFTs to have a low operating voltage, ideally at or below 1 V. One method to achieve a low operating voltage is to decrease the thickness of dielectric layer. However, the gate leakage current can be too large if a conventional gate dielectric layer, e.g., SiO_2 ,

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is too thin [4], [5]. Both liquid and solid-state electrolytes have been used to form electric-double-layers with very high capacitance and have been shown to enable an operating voltage as low as 1 V [6], [7]. Alternatively, high dielectric constant (high- κ) materials, such as Al_2O_3 , HfO_2 and Ta_2O_5 , have been used as a dielectric layer because they can provide a large specific gate capacitance without dramatically increasing the gate leakage current [8]–[10]. Among all high- κ dielectric materials, Al_2O_3 is often used because of its advantages such as low cost, low deposition temperature, low leakage-current density and good compatibility with oxide semiconductors [11], [12].

A very common way to deposit highly conformal and pinhole-free aluminum oxide films is by atomic-layer deposition (ALD) [13], [14]. However, ALD typically suffers from slow growth rate and it is still challenging to use ALD for large-area non-vacuum deposition. An alternative approach towards high-quality Al_2O_3 is anodization, which has been demonstrated as a cost-efficient method of corrosion protection and for manufacturing of capacitors at room temperature [15]. Importantly, anodization is a self-limiting process so pinholes close themselves during the process, resulting in pinhole-free, homogenous oxides [16]. Moreover, the low process temperature of anodic aluminum oxide makes it compatible with flexible electronic devices. Efforts have been made to use anodized aluminum oxide as the dielectric layer for organic field-effect transistors, enabling a very low operating voltage [17], [18]. However, in reports of oxide semiconductor-based TFTs using anodized aluminum oxide as a gate dielectric layer, the operating voltage was higher than 3 V due to the thickness of the anodized films [8], [11], [19], [20]. For ultra-low power devices, it is desirable to achieve an operating voltage at or below 1 V by decreasing the thickness of the anodized dielectric.

Here, IGZO TFTs using solution-processed, ultra-thin Al_xO_y as gate dielectrics have been fabricated with high yield at room temperature. The fabricated devices exhibit excellent and highly reproducible performance with a very low operating voltage of 1 V, a high current on/off ratio $>10^5$ and a low subthreshold swing close to the theoretical limit at 300 K. This work may find applications in areas such as aqueous sensing and ultralow power electronics.

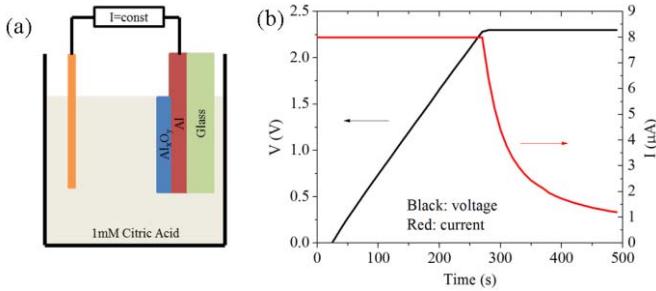


Fig. 1. (a) Schematic diagram of anodization bath for growth of Al_xO_y layer. (b) Voltage (left axis) and current (right axis) as a function of the anodization time.

II. EXPERIMENTS

An Al_xO_y film was formed in an electrolyte consisting of 1 mM citric acid with an Al film as the anode electrode and a gold cathode, as shown in Fig. 1(a). Three Al gate fingers were connected to a large Al contact pad. During anodization, only these three gate fingers were submerged in the solution. A constant anodization current ($0.1 \text{ mA}/\text{cm}^2$) was applied to the large Al contact pad until the targeted anodization voltage was achieved. The sample was held at this voltage until the current fell below $0.015 \text{ mA}/\text{cm}^2$. Fig. 1(b) shows typical anodization current and voltage as a function of anodization time. With an anodization ratio of $c_{\text{Al}} = 1.3 \text{ nm/V}$ [18], a 2.3 V anodization voltage corresponds to an estimated insulator thickness of $\sim 3 \text{ nm}$.

The gate electrode for the IGZO TFTs was formed by thermal evaporation of a 200 nm-thick Al film. The gate lines were then anodized to form the Al_xO_y gate dielectric. Next, a 25 nm-thick IGZO (In:Ga:Zn = 1:1:1) channel layer was deposited by radio-frequency magnetron sputtering at 40 W at room temperature. Finally, 150 nm-thick Al was thermally evaporated to form the source and drain electrodes. All layers were patterned using shadow masks. The channel length and width were $60 \mu\text{m}$ and 2 mm, respectively. The electrical characteristics of the devices were measured using an Agilent E5270B semiconductor analyzer and an Agilent E4980A LCR meter at room temperature.

III. RESULTS AND DISCUSSIONS

The specific capacitance of the Al_xO_y layer was measured using an Al/ Al_xO_y /Al structure, as shown in the inset of Fig. 2(b). 15 capacitors were chosen randomly among about 100 devices to measure the capacitance and an average specific capacitance of $1000 \text{ nF}/\text{cm}^2$ was obtained in the case of an anodization voltage of 2.3 V with a standard deviation of only $30 \text{ nF}/\text{cm}^2$, confirming a high uniformity. This value is lower than the expected theoretical value for Al_2O_3 of the same thickness, possibly due to the formation of highly polar $\text{Al}(\text{OH})_3$ in anodized Al film [21]. In order to confirm this, X-ray photoelectron spectroscopy (XPS) was carried out, the results of which are displayed in Fig. 2(a). By comparing the areas beneath the Al 2p and O 1s peaks, the atomic ratio of Al to O is found to be less than 2:3, demonstrating that the anodized film is not made of pure Al_2O_3 . The O 1s peak

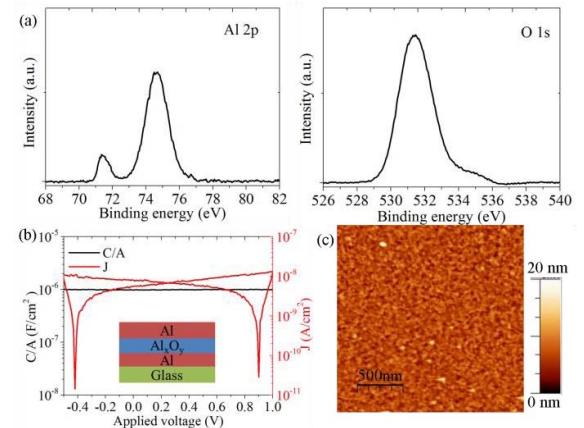


Fig. 2. (a) XPS spectra of Al 2p and O 1s of the Al_xO_y film. (b) C-V (black) and J-V (red) characteristics of Al/3 nm-thick Al_xO_y /Al capacitor. Inset: A schematic diagram of the Al/ Al_xO_y /Al capacitors. (c) Surface morphology of Al_xO_y by atomic-force microscope.

is found to be 531.5 eV, which suggests a superposition of two individual peaks, namely Al-O occurring at $\sim 531.0 \text{ eV}$ and Al-OH occurring at $\sim 532.0 \text{ eV}$. The capacitance-voltage (C-V) and leakage-voltage (J-V) of the capacitors were also measured. The left axis of Fig. 2(b) shows that the capacitance per unit area remains constant at $\sim 1 \text{ } \mu\text{F}/\text{cm}^2$ when varying the voltage from -0.5 V to 1 V . In addition, as shown in the right axis of Fig. 2(b), the maximum leakage current density throughout the whole test is only slightly above $10^{-8} \text{ A}/\text{cm}^2$, which is comparable to or indeed lower than those anodized amorphous dielectrics reported previously [10], [11].

The surface morphology of the film was studied using an atomic-force microscope (AFM), as shown in Fig. 2(c). The RMS roughness of the film was found to be 1.54 nm, indicating that the anodized film is smooth and uniform, and hence suitable for TFT applications.

In order to investigate the influence of anodization voltages to the electrical properties of the obtained TFTs, three anodization voltages were examined: 1.54, 2.30 and 3.08 V, corresponding to devices A, B and C, respectively. The transfer characteristics of these devices are shown in Fig. 3(a) and their electrical properties are summarized in Table I.

The TFT current on/off ratios are found to be on the order of 10^6 in all devices. Gate leakage currents, I_G , only slightly increase with the decrease of Al_xO_y anodization voltage, confirming a high quality and the pinhole free film. The subthreshold swing, SS , is found to be 75 mV/dec for device A, 68 mV/dec for device B and 70 mV/dec for device C, which are all very close to the theoretical limit of ideal field-effect transistor at 300 K [22]. The interface trap density, D_{it} , can be calculated through:

$$D_{it} = \left(\frac{SS \log(e)}{kT/q} - 1 \right) \frac{C}{q^2}, \quad (1)$$

where k is the Boltzmann's constant, e is the base of the natural logarithm, T is the temperature, q is the electron charge and C is the capacitance per unit area. By using the capacitance shown in Table I, D_{it} is found to be $1.7 \times 10^{12} \text{ cm}^{-2} \text{ eV}^{-1}$ for device A, $8.5 \times 10^{11} \text{ cm}^{-2} \text{ eV}^{-1}$ for device B

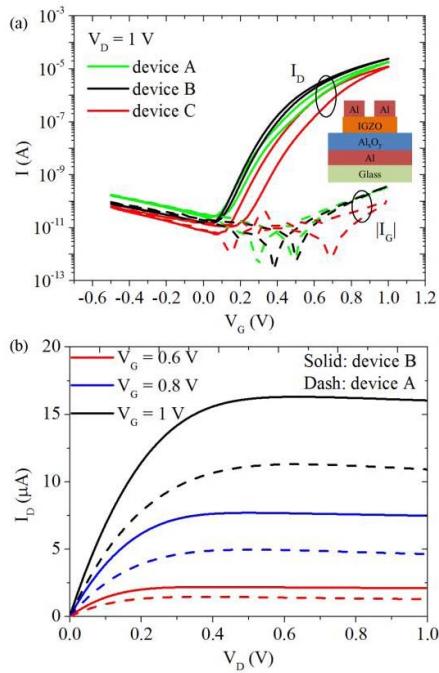


Fig. 3. Electrical properties of the IGZO TFTs. (a) Typical transfer characteristics. Inset: A schematic structure of the IGZO TFTs. (b) Typical output characteristics. The anodization voltages for the dielectric layer of devices A, B and C are 1.54 V, 2.3 V and 3.08 V, respectively.

TABLE I

ELECTRICAL PROPERTIES OF IGZO TFTs GATED WITH Al_xO_y ANODIZED USING DIFFERENT VOLTAGES

Device	A	B	C
Anodization voltage (V)	1.54	2.30	3.08
Approximate Al_xO_y thickness (nm)	2	3	4
C/A (nF/cm ²)	1100	1000	875
Current on/off ratio	7.2×10^5	1.6×10^6	2.1×10^6
SS (mV/dec)	75	68	70
D_{it} (cm ² eV ⁻¹)	1.7×10^{12}	8.5×10^{11}	9.2×10^{11}
RMS roughness (nm)	1.58	1.54	1.53
V_{TH} (V)	0.52	0.48	0.51
μ (cm ² /Vs)	~ 4.3	~ 5.4	~ 3.5

and $9.2 \times 10^{11} \text{ cm}^{-2} \text{ eV}^{-1}$ for device C. These values are either comparable or even better than D_{it} of similar interfaces reported previously [8], [23]. Device A shows higher interface trap density than device B and C, which may be due to the presence of a greater proportion of native aluminum oxide formed before anodization. The interface trap density is found to be quite similar for device B and C, which is in agreement with their surface roughness. The threshold voltage, V_{TH} , is found to be ~ 0.5 V for all three types of devices. The field-effect mobility, μ , in the saturation region has been derived from the following equation:

$$I_D = \left(\frac{\mu W C}{2L} \right) (V_G - V_{TH})^2, \quad (2)$$

where I_D is the drain current, L is the channel length, W is the channel width and V_G is the applied gate voltage. The mobility values are calculated to be $\sim 4.3 \text{ cm}^2/\text{Vs}$ for device A, $\sim 5.4 \text{ cm}^2/\text{Vs}$ for device B and $\sim 3.5 \text{ cm}^2/\text{Vs}$ for device C, comparable to previously reported results [24]–[26].

The corresponding output characteristics of devices A and B are shown in Fig. 3(b). It can be seen that both devices work

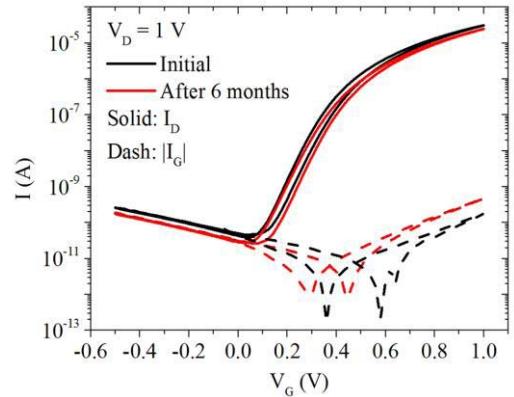


Fig. 4. Transfer characteristics of IGZO TFT before and after being stored in ambient air without any encapsulation layer for six months.

in enhancement-mode, and the drain current exhibits a clear pinch off and saturates at higher drain voltages. I_D of device B is found to be higher than that of device A, in agreement with the transfer curves shown in Fig. 3(a). A combination of the highest on-current, the lowest interface trap density and the highest mobility is clearly found in the transistor gated with 2.3 V anodized Al_xO_y .

In order to investigate the uniformity and reproducibility of the devices, 20 IGZO TFTs gated with 2.3 V anodized Al_xO_y were selected randomly among 100 devices that were fabricated in different batches to compare their electrical properties. The devices fabricated in different batches showed very similar performances with $V_{TH} = 0.45 \pm 0.09$ V, $SS = 72 \pm 8$ mV/dec and $\mu = 5 \pm 1 \text{ cm}^2/\text{Vs}$, demonstrating very good uniformity and reproducibility. The current on/off ratios for all measured devices were found to be larger than 10^5 and the maximum gate leakage current was around 1 nA. The hysteresis of the TFTs was calculated using the threshold voltage difference between forward and backward curves. For all the measured devices, it was found to be less than 50 mV, which is much smaller than most IGZO TFTs without an encapsulation layer or post-annealing treatment [27]–[29].

We also measured the devices again after storing them in air without any encapsulation layer for six months and the obtained transfer characteristics are shown in Fig. 4. The current on/off ratio, V_{TH} , SS and μ were 8.1×10^5 , 0.43 V, 70 mV/dec and $5.6 \text{ cm}^2/\text{Vs}$ before the storage, and 9×10^5 , 0.46 V, 72 mV/dec and $5.1 \text{ cm}^2/\text{Vs}$ after being stored in ambient air for six months. Only small changes of electrical properties are found here, which demonstrates that our devices have a superb stability. It is expected that the stability of our devices can be further improved by adding a capping layer.

In conclusion, high-performance IGZO TFTs based on solution-processed Al_xO_y gate dielectrics were fabricated at room temperature. Al_xO_y dielectrics with different anodization voltages have been studied. It has been shown that the transistors gated with 2.3 V anodized Al_xO_y exhibited the optimum performances with an operating voltage of 1 V, a high current on/off ratio $> 10^5$ and a subthreshold swing as low as 68 mV/dec. These devices show potential for applications in low-cost, low-power electronics.

REFERENCES

- [1] K. Nomura, H. Ohta, A. Takagi, T. Kamiya, M. Hirano, and H. Hosono, "Room-temperature fabrication of transparent flexible thin-film transistors using amorphous oxide semiconductors," *Nature*, vol. 432, no. 4016, pp. 488–492, 2004, doi: [10.1038/nature03090](https://doi.org/10.1038/nature03090).
- [2] T. Hirao, M. Furuta, T. Hiramatsu, T. Matsuda, C. Li, H. Furuta, H. Hokari, M. Yoshida, H. Ishii, and M. Kakegawa, "Bottom-gate zinc oxide thin-film transistors (ZnO TFTs) for AM-LCDs," *IEEE Trans. Electron Devices*, vol. 55, no. 11, pp. 3136–3142, Nov. 2008, doi: [10.1109/TED.2008.2003330](https://doi.org/10.1109/TED.2008.2003330).
- [3] P. Görnn, M. Sander, J. Meyer, M. Kröger, E. Becker, H. H. Johannes, W. Kowalsky, and T. Riedl, "Towards see-through displays: Fully transparent thin-film transistors driving transparent organic light-emitting diodes," *Adv. Mater.*, vol. 18, no. 6, pp. 738–741, 2006, doi: [10.1002/adma.200501957](https://doi.org/10.1002/adma.200501957).
- [4] G. D. Wilk, R. M. Wallace, and J. Anthony, "High-k gate dielectrics: Current status and materials properties considerations," *J. Appl. Phys.*, vol. 89, no. 10, pp. 5243–5275, 2001, doi: [10.1063/1.1361065](https://doi.org/10.1063/1.1361065).
- [5] J. Robertson, "High dielectric constant gate oxides for metal oxide Si transistors," *Rep. Prog. Phys.*, vol. 69, no. 2, pp. 327–396, 2005, doi: [10.1088/0034-4885/69/2/R02](https://doi.org/10.1088/0034-4885/69/2/R02).
- [6] X. Ma, J. Zhang, W. Cai, H. Wang, J. Wilson, Q. Wang, Q. Xin, and A. Song, "A sputtered silicon oxide electrolyte for high-performance thin-film transistors," *Sci. Rep.*, vol. 7, p. 809, Apr. 2017, doi: [10.1038/s41598-017-00939-6](https://doi.org/10.1038/s41598-017-00939-6).
- [7] H. Yuan, H. Shimotani, A. Tsukazaki, A. Ohtomo, M. Kawasaki, and Y. Iwasa, "High-density carrier accumulation in zno field-effect transistors gated by electric double layers of ionic liquids," *Adv. Funct. Mater.*, vol. 19, no. 7, pp. 1046–1053, 2009, doi: [10.1002/adfm.200801633](https://doi.org/10.1002/adfm.200801633).
- [8] L. Lan and J. Peng, "High-performance indium–gallium–zinc oxide thin-film transistors based on anodic aluminum oxide," *IEEE Trans. Electron Devices*, vol. 58, no. 5, pp. 1452–1455, May 2011, doi: [10.1109/TED.2011.2115248](https://doi.org/10.1109/TED.2011.2115248).
- [9] C. J. Chiu, S. P. Chang, and S. J. Chang, "High-performance a-IGZO thin-film transistor using Ta₂O₅ gate dielectric," *IEEE Electron Device Lett.*, vol. 31, no. 11, pp. 1245–1247, Nov. 2010, doi: [10.1109/LED.2010.2066951](https://doi.org/10.1109/LED.2010.2066951).
- [10] Y. Shao, X. Xiao, X. He, W. Deng, and S. Zhang, "Low-voltage a-InGaZnO thin-film transistors with anodized thin HfO₂ gate dielectric," *IEEE Electron Device Lett.*, vol. 36, no. 6, pp. 573–575, Jun. 2015, doi: [10.1109/LED.2015.2422895](https://doi.org/10.1109/LED.2015.2422895).
- [11] H. Xu, J. Pang, M. Xua, M. Lia, Y. Guo, Z. Chen, L. Wang, J. Zoua, H. Taoa, Lei Wanga, and J. Peng, "Fabrication of flexible amorphous indium-gallium-zinc-oxide thin-film transistors by a chemical vapor deposition-free process on polyethylene naphthalate," *ECS J. Solid State Sci. Technol.*, vol. 3, no. 9, pp. Q3035–Q3039, 2014, doi: [10.1149/2.007409jss](https://doi.org/10.1149/2.007409jss).
- [12] J. B. Kim, C. Fuentes-Hernandez, W. J. Potscavage, Jr., X.-H. Zhang, and B. Kippelen, "Low-voltage InGaZnO thin-film transistors with Al₂O₃ gate insulator grown by atomic layer deposition," *App. Phys. Lett.*, vol. 94, no. 14, p. 142107, 2009, doi: [10.1063/1.3118575](https://doi.org/10.1063/1.3118575).
- [13] X.-H. Zhang, B. Domercq, X. Wang, S. Yoo, T. Kondo, Z. L. Wang, and B. Kippelen, "High-performance pentacene field-effect transistors using Al₂O₃ gate dielectrics prepared by atomic layer deposition (ALD)," *Organic Electron.*, vol. 8, no. 6, pp. 718–726, 2007, doi: [10.1016/j.orgel.2007.06.009](https://doi.org/10.1016/j.orgel.2007.06.009).
- [14] M. Groner, F. Fabreguette, J. Elam, and S. George, "Low-temperature Al₂O₃ atomic layer deposition," *Chem. Mater.*, vol. 16, no. 4, pp. 639–645, 2004, doi: [10.1021/cm0304546](https://doi.org/10.1021/cm0304546).
- [15] M. M. Lohrengel, "Thin anodic oxide layers on aluminium and other valve metals: High field regime," *Mater. Sci. Eng., R, Rep.*, vol. 11, no. 6, pp. 243–294, 1993, doi: [10.1016/0927-796X\(93\)90005-N](https://doi.org/10.1016/0927-796X(93)90005-N).
- [16] M. J. Jeng and J. G. Hwu, "Thin-gate oxides prepared by pure water anodization followed by rapid thermal densification," *IEEE Electron Device Lett.*, vol. 17, no. 12, pp. 575–577, Dec. 1996.
- [17] B. Urasinska-Wojcik, N. Cocherel, R. Wilson, J. Burroughes, J. Opoku, M. L. Turner, and L. A. Majewski, "1 volt organic transistors with mixed self-assembled monolayer/Al₂O₃ gate dielectrics," *Organic Electron.*, vol. 26, pp. 20–24, Nov. 2015, doi: [10.1016/j.orgel.2015.07.009](https://doi.org/10.1016/j.orgel.2015.07.009).
- [18] L. A. Majewski, R. Schroeder, and M. Grell, "Flexible high capacitance gate insulators for organic field effect transistors," *J. Phys. D, Appl. Phys.*, vol. 37, no. 1, pp. 21–24, 2003, doi: [10.1088/0022-3727/37/1/005](https://doi.org/10.1088/0022-3727/37/1/005).
- [19] X. Xiao, Y. Shao, X. He, W. Deng, L. Zhang, and S. Zhang, "Back channel anodization amorphous indium gallium zinc oxide thin-film transistors process," *IEEE Electron Device Lett.*, vol. 36, no. 4, pp. 357–359, Apr. 2015, doi: [10.1109/LED.2015.2407578](https://doi.org/10.1109/LED.2015.2407578).
- [20] L. Lan, M. Zhao, N. Xiong, P. Xiao, W. Shi, M. Xu, and J. Peng, "Low-voltage high-stability indium–zinc oxide thin-film transistor gated by anodized neodymium-doped aluminum," *IEEE Electron Device Lett.*, vol. 33, no. 6, pp. 827–829, Jun. 2012, doi: [10.1109/LED.2012.2190966](https://doi.org/10.1109/LED.2012.2190966).
- [21] L. A. Majewski, M. Grell, S. D. Ogier, and J. Veres, "A novel gate insulator for flexible electronics," *Organic Electron.*, vol. 4, no. 1, pp. 27–32, 2003, doi: [10.1016/S1566-1199\(03\)00005-3](https://doi.org/10.1016/S1566-1199(03)00005-3).
- [22] V. V. Zhirnov and R. K. Cavin, "Nanoelectronics: Negative capacitance to the rescue?" *Nature Nanotechnol.*, vol. 3, pp. 77–78, 2008, doi: [10.1038/nnano.2008.18](https://doi.org/10.1038/nnano.2008.18).
- [23] J.-M. Lee, B.-H. Choi, M.-J. Ji, J.-H. Park, J.-H. Kwon, and B.-K. Ju, "The improved performance of a transparent ZnO thin-film transistor with AlN/Al₂O₃ double gate dielectrics," *Semicond. Sci. Technol.*, vol. 24, no. 5, p. 055008, 2009, doi: [10.1088/0268-1242/24/5/055008](https://doi.org/10.1088/0268-1242/24/5/055008).
- [24] K. Nomura, T. Kamiya, and H. Hosono, "Interface and bulk effects for bias—Light-illumination instability in amorphous-In–Ga–Zn–O thin-film transistors," *J. Soc. Inf. Display*, vol. 18, no. 10, pp. 789–795, 2010, doi: [10.1889/JSID18.10.789](https://doi.org/10.1889/JSID18.10.789).
- [25] Y. Kikuchi, K. Nomura, H. Yanagi, T. Kamiya, M. Hirano, and H. Hosono, "Device characteristics improvement of a-In–Ga–Zn–O TFTs by low-temperature annealing," *Solid Films*, vol. 518, no. 11, pp. 3017–3021, 2010, doi: [10.1016/j.tsf.2009.10.132](https://doi.org/10.1016/j.tsf.2009.10.132).
- [26] C.-S. Fuh, S. M. Sze, P.-T. Liu, L.-F. Teng, and Y.-T. Chou, "Role of environmental and annealing conditions on the passivation-free in-Ga–Zn–O TFT," *Solid Films*, vol. 520, no. 5, pp. 1489–1494, 2011, doi: [10.1016/j.tsf.2011.08.088](https://doi.org/10.1016/j.tsf.2011.08.088).
- [27] S. Y. Lee, S. Chang, and J.-S. Lee, "Role of high-k gate insulators for oxide thin film transistors," *Solid Films*, vol. 518, no. 11, pp. 3030–3032, 2010, doi: [10.1016/j.tsf.2009.09.165](https://doi.org/10.1016/j.tsf.2009.09.165).
- [28] M. Kimura, T. Nakanishi, K. Nomura, T. Kamiya, and H. Hosono, "Trap densities in amorphous-InGaZnO_x thin-film transistors," *Appl. Phys. Lett.*, vol. 92, no. 13, p. 133512, 2008, doi: [10.1063/1.2904704](https://doi.org/10.1063/1.2904704).
- [29] S. W. Tsao, T. C. Chang, S. Y. Huang, M. C. Chen, S. C. Chen, C. T. Tsai, Y. J. Kuo, Y. C. Chen, and W. C. Wu, "Hydrogen-induced improvements in electrical characteristics of a-IGZO thin-film transistors," *Solid-State Electron.*, vol. 54, no. 12, pp. 1497–1499, 2010.