High Voltage Gain Inverters From Artificially Stacked Bilayer CVD Graphene FETs

Himadri Pandey, *Student Member, IEEE*, Satender Kataria, Amit Gahoi, *Student Member, IEEE*, and Max C. Lemme, *Senior Member, IEEE*

***Abstract*— In this letter, we report on inverters made from graphene field effect transistors with channels of artificially stacked bilayer graphene (ASBLG). The materials were grown by scalable chemical vapor deposition. The devices demonstrate enhanced voltage gain (A_V) figures at relatively lower input voltages when compared with devices with single layer graphene channels. A gain value as high as 7.134 is obtained using ASBLG-based inverters without any applied back-gate voltage. The improved performance is discussed in terms of transconductance and contact resistance. Our results suggest that ASBLG-based inverters may be useful for future RF circuit applications.**

***Index Terms*— Artificially stacked bilayer graphene, chemical vapor deposited graphene, inverters, voltage gain.**

I. Introduction

AN INVERTER is a complementary NOT gate, typically consisting of a co-joined pair of p-doped and n-doped field effect transistors (FET). It is the most fundamental circuit building block and it demonstrates the capability of any FET technology for signal inversion and thus, circuit applications. Single layer graphene has zero band gap which results in poorly saturating output characteristics of graphene field effect transistors (GFETs), and in turn poor intrinsic voltage gain values in both transistor [1], [2] and inverter configurations [3]. Improvements have been achieved by enhancing gate control through thin top gate dielectrics [4]–[7]. Alternatively, Bernal stacked bilayer graphene with electrically tunable band gaps of the order of a few hundred meV have been proposed and successfully demonstrated to improve current saturation, intrinsic transistor voltage gain and inverter gain [8]–[12]. However, the scalable production of Bernal stacked bilayer is yet to be optimized due to technological limitations encountered in its growth using chemical vapor deposition (CVD) [13].

Even though there have been several reports of large area growth of Bernal stacked bilayer graphene [14]–[16], the device performance obtained from such grown material was found to be largely varying [15]. Recently, we have reported improved voltage gain in FETs made with channels of artificially stacked bilayer graphene (ASBLG), which we attributed to enhanced carrier-carrier scattering under certain biasing conditions [17]. In this letter, we demonstrate and discuss inverters made from ASBLG fabricated by stacking two single layers of graphene (SLG), grown in-house using a thermal CVD method [18]. We demonstrate improved voltage gain at zero back gate voltage conditions in these inverters compared to those based on SLG channels at ambient conditions. Our results suggest possible radio frequency (RF) circuit applications of ASBLG inverters.

II. Device Fabrication

We fabricated graphene based inverters on thermally oxidized Si substrates using optical lithography with gate lengths (L_g) between 3 and 12 μm. Channel widths (W) in different cases were 10 μm to 60 μm (in steps of 10 μm). Two sets of devices were simultaneously prepared, each consisting of a co-fabricated pair of SLG & ASBLG CVD graphene devices. For the first set, electron-beam evaporated silicon dioxide (SiO_2) and for the second set, ambient oxidized aluminum (i.e. AlO_x, $t_{ox} \sim 4$ to 8 nm) were used as gate dielectrics [5], [12]. Contact metal in all devices was 100 nm thick e-beam evaporated gold (Au). Device fabrication details can be found in [17].

III. Results & Discussions

The devices were characterized under ambient and vacuum conditions using a Keithley 4200 SCS Semiconductor parameter analyzer. The measurements under vacuum were carried out using Lakeshore TTPX probe station connected to a similar analyzer. Fig. 1 (a) shows a schematic of an inverter circuit with ASBLG channels and Fig. 1 (b) shows the optical micrograph of a fabricated ASBLG device in co-planar waveguide layout, along with the equivalent circuit diagram for the inversion functionality overlaid to the real device image for easy reference to the reader. Complementary-like inverters are obtained from these co-joined parallel gate

Manuscript received September 30, 2017; revised October 18, 2017; accepted October 18, 2017. Date of current version November 22, 2017. This work was supported in part by the German Research Foundation under Grant LE 2440/1-2, Grant LE 2440/2-1, and Grant LE 2440/3-1 and in part by the European Commission through an ERC starting grant (InteGraDe, 307311). The review of this letter was arranged by Editor D. Akinwande. *(Corresponding author: Max C. Lemme.)*

H. Pandey and S. Kataria are with the Chair for Electronic Devices, RWTH Aachen University, 52074 Aachen, Germany.

A. Gahoi is with Graphene-based Nanotechnology, Universität Siegen, 57076 Siegen, Germany.

M. C. Lemme is with the Advanced Microelectronic Center Aachen, AMO GmbH, 52074 Aachen, Germany, and with the Chair for Electronic Devices, RWTH Aachen University, 52074 Aachen, Germany, and also with the Graphene-based Nanotechnology, Universität Siegen, 57076 Siegen, Germany (e-mail: lemme@amo.de).

Color versions of one or more of the figures in this letter are available online at http://ieeexplore.ieee.org.

Digital Object Identifier 10.1109/LED.2017.2768076

0741-3106 © 2017 IEEE. Translations and content mining are permitted for academic research only. Personal use is also permitted, but republication/redistribution requires IEEE permission. See http://www.ieee.org/publications_standards/publications/rights/index.html for more information.

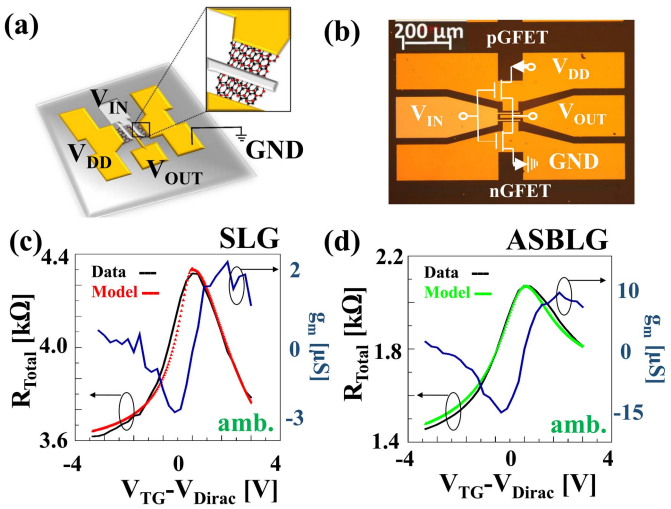

Fig. 1. (a) Schematic of ASBLG inverters showing biasing scheme used in this work (Input voltage: V_{IN}; Output voltage: V_{OUT}; Supply voltage: V_{DD}; ground: GND; inset: randomly stacked graphene channel. (b) Optical micrograph of a graphene FET in coplanar waveguide layout with conventional equivalent circuit diagram for the inverter functionality overlaid for easy reference. (c)(d) Total device resistance as a function of gate overdrive for co-fabricated single layer (SLG) and ASBLG FETs for a source drain voltage of $V_{DS} = 0.1$ V. The right axes show corresponding DC transconductance (g_m) values. The ASBLG FET shows improved g_m. $L_g = 3$ μm and W = 50 μm, respectively.

GFETs by electrostatically doping them using a supply voltage (V_{DD}), as described by the equivalent circuit diagram. Since both GFETs are co-fabricated with similar geometry and parameters, they behave very similarly at low V_{DD} (~0.1V). However, when a large V_{DD} (>1V in this work) is applied at the drain terminal of one of the GFETs and the source terminal of the other GFET is grounded, while the output is measured at the common terminal (V_{OUT}), the V_{DD} connected GFET behaves like a p-FET while the ground (GND) connected GFET behaves like a n-FET [12]. This is because the voltage drop across the source-drain terminals of the two GFETs is different with respect to each other as the lateral electric field "dopes" them differently. Note that this electrostatic doping is entirely different from classic semiconductor doping. As a result, the drain induced Dirac shifts (DIDS) [19] observed in the two GFETs are different, when their respective channels are modulated by a common input (gate) voltage V_{IN}. This approach of obtaining complementary-like inversion through electrostatic doping is similar to that reported in [12] and [5], and in contrast to literature reports where one of the GFETs was modified (i.e. "doped") by methods such as current annealing [3] or polymer doping [20].

We measured the transfer characteristics of the individual FETs in the inverter devices. Fig. 1 (c) and 1 (d) show the variation of total resistance (R_{Total}) as a function of gate overdrive (V_{TG}-V_D, where V_{TG} is the top gate voltage and V_D is the Dirac voltage) for a SLG and ASBLG FET, respectively. The data is presented for two randomly chosen devices with equal gate length, channel width and oxide thicknesses for a fair comparison. On the corresponding right axes, the DC transconductance (g_m) values are shown for each case. We observe a decrease in R_{Total} for the ASBLG FET compared to SLG FET by around 50%. Moreover, improved g_m is also observed in the case of the ASBLG FET. The mobility (μ) and contact resistance (R_c) values were extracted by fitting a model [21] to the respective transfer curves. We extracted typical values of $\mu = 1000$ cm^2/Vs and $R_c = 8.25$ k$\Omega \cdot \mu$m for the SLG FET, and $\mu = 1100$ cm^2/Vs and $R_c = 4.09$ k$\Omega \cdot \mu$m for the ASBLG FET. The slightly higher mobility and a lower contact resistance point towards somewhat improved electronic properties of the ASBLG FET. Moreover, the highest mobility and DC g_m values measured in ASBLG FETs are $\mu = 2200$ cm^2/Vs at $V_{DS} = 10$ mV and $g_m = 41$ μS/μm at $V_{DS} = 4.1$ V, respectively. Transfer length method (TLM) structures (not shown) confirmed the trend: The R_c value for SLG TLMs was ~ 1628 $\Omega\mu$m and ~ 632 $\Omega\mu$m for the ASBLG TLM for a channel width of 40 μm. The R_c values were obtained at a back-gate bias of 0V, and hence are generally much lower compared to the ones obtained using the fit model. An additional reason for the large difference between the values obtained from the model and the TLM is that the model assumes constant mobility and R_c, which is not the case in reality, as they both depend on the back gate bias [22]. Nevertheless, these independent results confirm the better electronic properties of ASBLG FETs, including improved g_m. This may be attributed to screening of one graphene layer by the other, resulting in improved transport in the screened layer. In order to understand the device performances obtained in our experiments, we consider the transport in ASBLG devices. There could possibly be two scenarios: either the top layer screens the gate field while the bottom layer acts predominantly as a channel where carrier transport takes place, or the bottom layer screens the substrate effects while the top layer acts predominantly as the channel. In the latter case, the carrier transport would be improved as the top layer would demonstrate more intrinsic-like transport. In the former case, screening of the gate field by the top layer would at least to some extent deteriorate the (top) gate modulation and thus, the transport properties observed in the device. Also, if the bottom graphene layer acted as channel, quantities like transconductance would instead degrade because of substrate interactions; i.e., SiO_2/Si surface below. As this is not the case in the experimental results, we attribute the improved voltage gain performance in ASBLG inverters to improved carrier transport in the top graphene layer while the bottom layer screens the substrate effects.

Fig. 2 (a) and 2 (b) show characteristics of SLG & ASBLG inverters in ambient conditions, respectively. The ASBLG inverter shows much steeper switching and improved gain, as A_v is the direct derivative of the inverter transfer curve [23]. We attribute this to improved g_m in these devices, as discussed above. We further characterized some ASBLG inverters under vacuum. The corresponding data in Fig. 2 (c) shows reduced steepness in transfer curves and reduced voltage gain under vacuum conditions. In addition, R_{Total} increases, which effectively reduces g_m. This is a result of ambient (humidity) doping of graphene which decreases in vacuum [24], leading to a shift in V_D and an increase of R_c at $V_{BG} = 0$V [25], [26].

Furthermore, for the ambient condition, the ASBLG FET shows the maximum voltage gain in a region closer to the

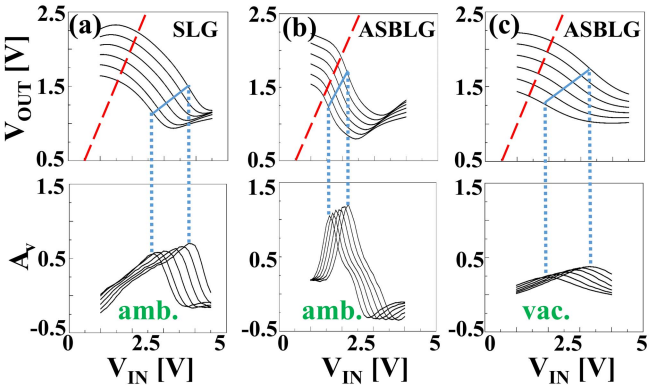

Fig. 2. (a) Inverter characteristics and voltage gain of a SLG inverter in ambient. (b) ASBLG inverter in ambient and (c) in vacuum conditions. The red line indicates the mid point voltage condition in each case, whereas the blue solid line indicates the points where respective maximum gains occur. The maximum gain region lies between the two dotted lines for 2.5 V $< V_{DD} <$ 3.5 V in each case. ASBLG inverters show higher gain than SLG inverters when measured in ambient, and when measured in vacuum. $L_g = 4$ μm and $W = 40$ μm in each case.

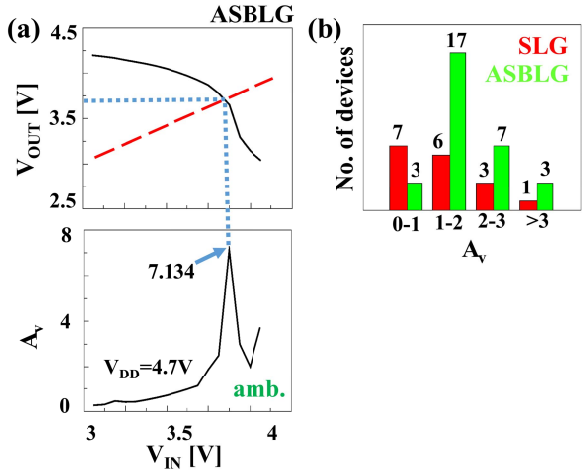

Fig. 3. (a) The best gain observed in artificially stacked BLG FET inverters, where also a near perfect input-output matching could be realized at a $V_{DD} = 4.7$ V in ambient conditions ($L_g = 12$ μm and $W = 20$ μm). This improvement in voltage gain was observed as a trend in a total of 47 devices characterized in this experiment. (b) Statistical summary of inverter gain of 47 devices, measured in ambient and at zero back gate voltage.

threshold voltage condition. The threshold voltage or mid-point voltage (V_M) condition is marked in Fig. 2 as a red dotted line along which $V_{IN} = V_{OUT} = V_M$. Generally, maximum gain in conventional CMOS inverters is obtained at $V_M = V_{DD}/2$ [23]. However, this condition is not fulfilled if there is asymmetry in hole and electron mobilities, as it is often the case in graphene FETs (e.g. Fig. 1 (c) and (d)).

ASBLG inverters show higher A_v at lower input voltages for the same V_{DD}. In other words, the maximum gain is observed closer to the switching threshold in ASBLG inverters. This results in improved noise margins and faster switching in ASBLG inverters compared to SLG inverters [23]. The maximum gain of $A_v = 7.134$ was observed in ASBLG inverters for $V_{DD} = 4.7$ V, which occurs around the input-output matched condition of $V_M = V_{IN} = V_{OUT} = 3.7$ V under ambient condition (Fig. 3 (a)). In contrast, a maximum of $A_v = 4$ was observed in all fabricated SLG inverters at $V_{DD} = 4.1$ V. The top gate oxide in both cases was thin ambient oxidized aluminum (AlO_x). For the other two chips with 10 nm e-beam evaporated SiO_2 top gate dielectric, the ASBLG and SLG inverters exhibit $A_v = 3.42$ ($V_{DD} = 3.9$ V) and $A_v = 2.21$ ($V_{DD} = 3.5$ V), respectively. A total of 47 inverters of both SLG and ASBLG type were characterized and summarized in Fig. 3 (b). The values reported in this work are compared to previously reported best inverter gain figures along with their respective technological metrics in Table I.

TABLE I
COMPARISON WITH PREVIOUS REPORTS

Graphene type	Dielectric type	Voltage Gain A_V	Measurement Conditions
Exfoliated, SLG	Thermal SiO_2	0.04 [3]	Only back gated, 300K, ambient
Exfoliated, SLG, $V_{BG} \neq 0$	Al_2O_3	4 [12]	77 K
Exfoliated, BLG, $V_{BG} \neq 0$	Al_2O_3	7 [12]	77 K
Exfoliated, SLG, side gated	Al_2O_3	1.5 [4]	300 K
CVD, SLG, cascaded, V_{BG}=0V	Al_2O_3	≥5 [5]	300 K, ambient
CVD, SLG, locally embedded backgate	Al_2O_3	5-14 [6]	300 K, ambient
CVD, SLG, dual gated	AlO_x	≥4 [7]	300 K, ambient
CVD, SLG, V_{BG}=0V, Au contacts	SiO_2	2.21	300 K, ambient (This work)
CVD, ASBLG, V_{BG}=0V, Au contacts	SiO_2	3.42	300 K, ambient (This work)
CVD, SLG, V_{BG}=0V, Au contacts	AlO_x	4	300 K, ambient (This work)
CVD, ASBLG, V_{BG}=0V, Au contacts	AlO_x	7.134	300 K, ambient (This work)

IV. CONCLUSIONS

Artificially stacked bilayer large-area CVD graphene inverters offer performance improvements over single layer graphene devices irrespective of the top gate dielectric used. An output matched $A_v > 4$ is obtained for several devices on the same chip in our experiments, enabling cascading into more complex circuit architectures in the future. A maximum gain of > 7 was observed under input-output matching condition at a supply voltage of 4.7 V. This improvement appears to have its origins in higher transconductance and lower contact resistance. The present results indicate the potential of large-area artificially stacked bilayer CVD graphene for future device & circuit applications.

ACKNOWLEDGMENT

The authors would like to acknowledge fruitful discussions with M. Iannazzo, E. Alarcon, S. Fregonese, and T. Zimmer.

REFERENCES

[1] M. C. Lemme, T. J. Echtermeyer, M. Baus, and H. Kurz, "A graphene field-effect device," *IEEE Electron Device Lett.*, vol. 28, no. 4, pp. 282–284, Apr. 2007, doi: 10.1109/LED.2007.891668.
[2] F. Schwierz, "Graphene transistors: Status, prospects, and problems," *Proc. IEEE*, vol. 101, no. 7, pp. 1567–1584, Jul. 2013, doi: 10.1109/JPROC.2013.2257633.
[3] F. Traversi, V. Russo, and R. Sordan, "Integrated complementary graphene inverter," *Appl. Phys. Lett.*, vol. 94, no. 22, p. 223312, 2009, doi: 10.1063/1.3148342.

[4] H.-Y. Chen and J. Appenzeller, "Complementary-type graphene inverters operating at room-temperature," in *Proc. 69th Annu. Device Res. Conf.*, Jun. 2011, pp. 33–34, doi: 10.1109/DRC.2011.5994408.

[5] L. G. Rizzi, M. Bianchi, A. Behnam, E. Carrion, E. Guerriero, L. Polloni, E. Pop, and R. Sordan, "Cascading wafer-scale integrated graphene complementary inverters under ambient conditions," *Nano Lett.*, vol. 12, no. 8, pp. 3948–3953, Aug. 2012, doi: 10.1021/nl301079r.

[6] D. Schall, M. Otto, D. Neumaier, and H. Kurz, "Integrated ring oscillators based on high-performance graphene inverters," *Sci. Rep.*, vol. 3, Sep. 2013, Art. no. 2592, doi: 10.1038/srep02592.

[7] E. Guerriero, L. Polloni, M. Bianchi, A. Behnam, E. Carrion, L. G. Rizzi, E. Pop, and R. Sordan, "Gigahertz integrated graphene ring oscillators," *ACS Nano*, vol. 7, no. 6, pp. 5588–5594, Jun. 2013, doi: 10.1021/nn401933v.

[8] B. N. Szafranek, G. Fiori, D. Schall, D. Neumaier, and H. Kurz, "Current saturation and voltage gain in bilayer graphene field effect transistors," *Nano Lett.*, vol. 12, no. 3, pp. 1324–1328, 2012, doi: 10.1021/nl2038634.

[9] J. B. Oostinga, H. B. Heersche, X. Liu, A. F. Morpurgo, and L. M. K. Vandersypen, "Gate-induced insulating state in bilayer graphene devices," *Nature Mater.*, vol. 7, no. 2, pp. 151–157, Feb. 2008, doi: 10.1038/nmat2082.

[10] Y. Zhang, Y. Zhang, T. Tang, C. Girit, Z. Hao, M. C. Martin, A. Zettl, M. F. Crommie, Y. R. Shen, and F. Wang, "Direct observation of a widely tunable bandgap in bilayer graphene," *Nature*, vol. 459, pp. 820–823, Jun. 2009, doi: 10.1038/nature08105.

[11] W. Zhang, C.-T. Lin, K.-K. Liu, T. Tite, C.-Y. Su, C.-H. Chang, Y.-H. Lee, C.-W. Chu, K.-H. Wei, J.-L. Kuo, and L.-J. Li, "Opening an electrical band gap of bilayer graphene with molecular doping," *ACS Nano*, vol. 5, no. 9, pp. 7517–7524, Sep. 2011, doi: 10.1021/nn202463g.

[12] S.-L. Li, H. Miyazaki, A. Kumatani, A. Kanda, and K. Tsukagoshi, "Low operating bias and matched input–output characteristics in graphene logic inverters," *Nano Lett.*, vol. 10, no. 7, pp. 2357–2362, Jul. 2010, doi: 10.1021/nl100031x.

[13] H. Zhou, W. J. Yu, L. Liu, R. Cheng, Y. Chen, X. Huang, Y. Liu, Y. Wang, Y. Huang, and X. Duan, "Chemical vapour deposition growth of large single crystals of monolayer and bilayer graphene," *Nature Commun.*, vol. 4, Jun. 2013, Art. no. 2096, doi: 10.1038/ncomms3096.

[14] Z. Sun, A.-O. Raji, Y. Zhu, C. Xiang, Z. Yan, C. Kittrell, E. L. G. Samuel, and J. M. Tour, "Large-area Bernal-stacked Bi-, Tri-, and tetralayer graphene," *ACS Nano*, vol. 6, no. 11, pp. 9790–9796, Nov. 2012, doi: 10.1021/nn303328e.

[15] W. Liu, S. Kraemer, D. Sarkar, H. Li, P. M. Ajayan, and K. Banerjee, "Controllable and rapid synthesis of high-quality and large-area Bernal stacked bilayer graphene using chemical vapor deposition," *Chem. Mater.*, vol. 26, no. 2, pp. 907–915, Jan. 2014, doi: 10.1021/cm4021854.

[16] X. Chen, R. Xiang, P. Zhao, H. An, T. Inoue, S. Chiashi, and S. Maruyama, "Chemical vapor deposition growth of large single-crystal Bernal-stacked bilayer graphene from ethanol," *Carbon*, vol. 107, pp. 852–856, Oct. 2016, doi: 10.1016/j.carbon.2016.06.078.

[17] H. Pandey, J.-D. Aguirre-Morales, S. Kataria, S. Fregonese, V. Passi, M. Iannazzo, T. Zimmer, E. Alarcon, and M. C. Lemme, "Enhanced intrinsic voltage gain in artificially stacked bilayer CVD graphene field effect transistors," *Ann. Phys.*, p. 1700106, Sep. 2017, doi: 10.1002/andp.201700106.

[18] S. Kataria, S. Wagner, J. Ruhkopf, A. Gahoi, H. Pandey, R. Bornemann, S. Vaziri, A. D. Smith, M. Ostling, and M. C. Lemme, "Chemical vapor deposited graphene: From synthesis to applications," *Phys. Status Solidi A*, vol. 211, no. 11, pp. 2439–2449, Nov. 2014, doi: 10.1002/pssa.201400049.

[19] S. Rodriguez, S. Vaziri, M. Ostling, A. Rusu, E. Alarcon, and M. C. Lemme, "RF performance projections of graphene FETs vs. silicon MOSFETs," *ECS Solid State Lett.*, vol. 1, no. 5, pp. Q39–Q41, Aug. 2012, doi: 10.1149/2.001205ssl.

[20] J. M. Yun, S. Park, Y. H. Hwang, E.-S. Lee, U. Maiti, H. Moon, B.-H. Kim, B.-S. Bae, Y.-H. Kim, and S. O. Kim, "Complementary p- and n-Type polymer doping for ambient stable graphene inverter," *ACS Nano*, vol. 8, no. 1, pp. 650–656, Jan. 2014, doi: 10.1021/nn4053099.

[21] S. Kim, J. Nah, I. Jo, D. Shahrjerdi, L. Colombo, Z. Yao, E. Tutuc, and S. K. Banerjee, "Realization of a high mobility dual-gated graphene field-effect transistor with Al_2O_3 dielectric," *Appl. Phys. Lett.*, vol. 94, no. 6, p. 62107, 2009, doi: 10.1063/1.3077021.

[22] T. Cusati, G. Fiori, A. Gahoi, V. Passi, M. C. Lemme, A. Fortunelli, and G. Iannaccone, "Electrical properties of graphene-metal contacts," *Sci. Rep.*, vol. 7, Jul. 2017, Art. no. 5109, doi: 10.1038/s41598-017-05069-7.

[23] Y. Taur and T. H. Ning, *Fundamentals of Modern VLSI Devices*, 2nd ed. Cambridge, U.K.: Cambridge Univ. Press, 2010.

[24] A. D. Smith, K. Elgammal, F. Niklaus, A. Delin, A. C. Fischer, S. Vaziri, F. Forsberg, M. Råsander, H. Hugosson, L. Bergqvist, S. Schröder, S. Kataria, M. Östling, and M. C. Lemme, "Resistive graphene humidity sensors with rapid and direct electrical readout," *Nanoscale*, vol. 7, no. 45, pp. 19099–19109, 2015, doi: 10.1039/C5NR06038A.

[25] D. H. Tien, J.-Y. Park, K. B. Kim, N. Lee, and Y. Seo, "Characterization of graphene-based FET fabricated using a shadow mask," *Sci. Rep.*, vol. 6, no. 1, Jul. 2016, Art. no. 25050, doi: 10.1038/srep25050.

[26] A. Gahoi, S. Wagner, A. Bablich, S. Kataria, V. Passi, and M. C. Lemme, "Contact resistance study of various metal electrodes with CVD graphene," *Solid-State Electron.*, vol. 125, pp. 234–239, Nov. 2016, doi: 10.1016/j.sse.2016.07.008.