Implementing p-bits With Embedded MTJ

Kerem Yunus Camsari, Sayeef Salahuddin, and Supriyo Datta

***Abstract*— Magnetic tunnel junctions (MTJs) utilizing unstable magnets with low barriers have been shown to be well-suited for the implementation of random number generators (RNGs). It has recently been shown that completely new applications involving optimization, inference, and invertible Boolean logic would be enabled if many RNGs can be interconnected to form large scale correlated networks. However, this requires a new device, namely, a three-terminal tunable RNG or a p-bit, whose input terminal can be used to pin its output to 0 or 1. In this letter, we show that a voltage driven p-bit can be implemented simply by incorporating existing RNGs into a transistor circuit using experimentally demonstrated 2-terminal MTJs, without requiring a new device. Using established SPICE models, we show that this proposed p-bit can be interconnected to build correlated p-circuits to implement useful functionalities including a representative example of an invertible AND gate that "factors" the output of an AND gate into consistent input combinations.**

***Index Terms*— Embedded MTJ, invertible logic, MTJ, neuromorphic computing, probabilistic computing**

MAGNETIC tunnel junctions (MTJs) using unstable magnets with low barriers whose magnetization m_z fluctuate randomly in the range $(-1,+1)$ have been shown to be well-suited for the implementation of random number generators (RNGs) [1]–[3], which have many applications in modern electronic systems. It has also been shown that completely new applications involving optimization [4], inference [5] and invertible Boolean logic [6]–[8] would be enabled if the individual RNG's can be interconnected to form large scale correlated networks. However, this requires three-terminal *tunable* RNG's or p-bits, whose input $V_i(t)$ can be used to pin the stochastic output $m_i(t)$ to 0 or 1 described by a characteristic sigmoidal function:

$$m_i(t) = \mathrm{sgn}\Big(\mathrm{rand}(-1,1) + \tanh[V_i(t)/V_0]\Big) \qquad (1)$$

Large scale correlated networks are created by interconnecting the p-bits such that the inputs {V} are obtained from a bias {h} and a weighted sum of the outputs {m}, scaled by a constant V_0:

$$V_i(t)/V_0 = h_i(t) + \sum J_{ij} m_j(t) \qquad (2)$$

Different functionalities are implemented through a proper choice of the *synaptic* matrix [J] and bias vector {h} which can be implemented either in software or in hardware making use of resistive or capacitive networks [9]–[12].

This letter presents a composite structure (Fig. 1) that *can be assembled out of existing devices* and behaves approximately like a p-bit described by (1). Using established SPICE models we show that this proposed p-bit can be interconnected to build large scale p-circuits to implement useful functionalities including an adder and a factorizer [7], [8]. Note that unlike previous 3-terminal proposals for hardware p-bits [7], the present proposal does *not* require any spin transfer torque (STT) which may or may not be present.

The key contribution of this letter lies in demonstrating that an existing 2-terminal MTJ with a randomly switching free layer [13]–[15] connected to the drain of a conventional transistor provides a p-bit with controllable statistics, exactly like the new 3-terminal device proposed in [7]. To establish their equivalence, we simulate the same AND gate and show identical results. Similar 2-Terminal MTJ-based designs may also be useful for ensemble-averaged implementations [5], [16] but this is not discussed further.

Embedded MTJ-Based p-bit: The proposed p-bit consists of a standard two-terminal MTJ connected to the drain of an NMOS transistor exactly as in the well-known embedded

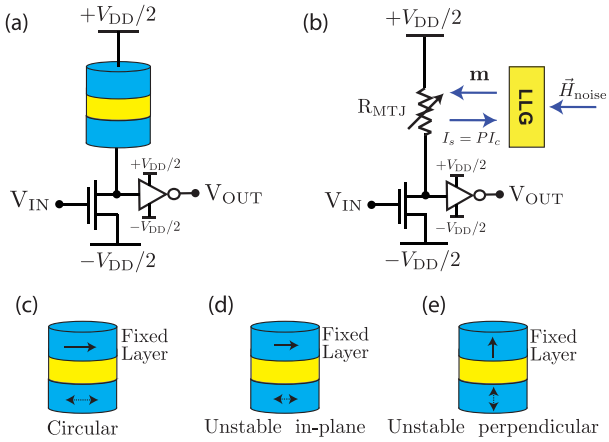

Fig. 1. (a) **Embedded MTJ-based p-bit**. (b) The circuit model uses a 14nm HP-FinFET predictive model, and the stochastic Landau-Lifshitz model that includes the magnetization dynamics, self-consistently with transistor equations. Three possible types of MTJs that can be used in (a) are: (c) An MTJ with a circular free layer [13] that rotates in the plane in the presence of thermal noise without a preferred easy axis. (d) An MTJ with an unstable, in-plane free-layer demonstrated in [14]. (e) Unstable perpendicular free layer demonstrated in [15].

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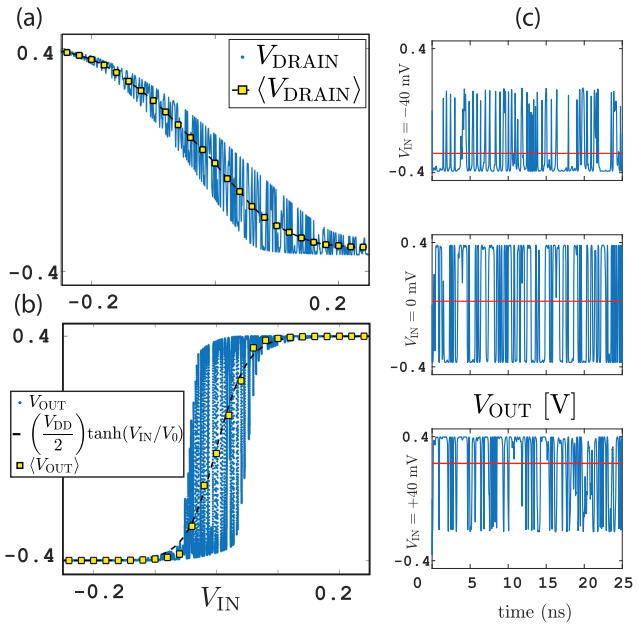

Fig. 2. **p-bit characteristics** (a) Transient simulation of the V_{DRAIN}, where dashed lines show the time-averaged value over 250 ns per each point. (b) V_{OUT} as a function of V_{IN} that is linearly swept from −0.4 V to 0.4 V in 100 ns. Dashed line is a tanh fit (See text). (c) Time-dependent V_{OUT} at different bias voltages. Red lines indicate the time averages. Note that during operation, no intermediate averaging is needed and the outputs are directly connected to other p-bits according to Eq. 2.

1T/1MTJ structure [17]. The only difference is that the magnets are low barrier ones with fluctuating magnetization giving rise to a fluctuating MTJ conductance that can be written in terms of the average conductance G_0 and the low-bias tunneling magnetoresistance defined as $(\text{TMR}) \equiv (G_P - G_{AP})/G_{AP}$ [18] where G_P, G_{AP} are the parallel ($m_{zi}(t) = 1$) and anti-parallel ($m_{zi}(t) = -1$) conductances for the MTJ, respectively.

$$G_i(t) = G_0\left[1 + m_{zi}(t)\ \text{TMR}/(2 + \text{TMR})\right] \tag{3}$$

where $m_{zi}(t) = \text{rand}(-1, 1)$. The circuit in Fig. 1 converts this fluctuating conductance to a fluctuating voltage at the drain:

$$\frac{V_{\text{DRAIN,i}}(t)}{V_{DD}} = -\frac{1}{2} + \frac{(2 + \text{TMR}) + \text{TMR}\ m_{zi}(t)}{(2 + \text{TMR})(1 + \alpha) + \text{TMR}\ m_{zi}(t)} \tag{4}$$

where we define the parameter $\alpha \equiv G_T(V_{DS}, V_{GS})/G_0$, G_T being the conductance of the NMOS transistor that is modeled using 14 nm HP-FinFET PTM [19]. In the current design, the average MTJ conductance G_0 is chosen to be exactly equal to the NMOS conductance ($\alpha = 1$) when $(V_{DS}, V_{GS}) = (V_{DD}/2, V_{DD}/2)$. It is then easy to see from Eq. 4 that

- With $V_{IN,i} < 0$, the transistor is OFF, $\alpha \to 0$ and $V_{\text{DRAIN,i}} \to V_{DD}/2$, independent of $m_{zi}(t)$.
- With $V_{IN,i} = 0$, $\alpha = 1$ and $V_{\text{DRAIN,i}}$ will show fluctuations $\sim [\text{TMR}/(2 + \text{TMR})]V_{DD}$ with an average of 0.
- With $V_{IN,i} > 0$, the transistor is ON, $\alpha \to \infty$ and $V_{\text{DRAIN,i}} \to -V_{DD}/2$, independent of $m_{zi}(t)$.

Note that the magnetization m_{zi} need not be pinned by the current as required by (1). Even if m_{zi} is completely unaffected, Eq. 4 along with an inverter makes $V_{OUT,i}$ behave qualitatively like (1) in response to $V_{IN,i}$. This anticipated behavior is confirmed by a detailed SPICE simulation (Fig. 2), where the average input/output relationship is closely approximated by $V_{OUT} = (V_{DD}/2)\tanh[V_{IN}/V_0]$, where $V_{DD} = 0.8$ V and $V_0 = 50$ mV (Fig. 2b). V_0 sets the input range of the sigmoid and is determined entirely by the transistor characteristics. The MTJ simply adds a noise to the transistor characteristics in this input range.

We thus have a voltage driven tunable RNG or a p-bit that behaves similar to (1), *simply through a circuit transformation of an existing RNG device, without requiring a new tunable RNG device.* Note that with experimentally demonstrated values of TMR, the maximum drain voltage fluctuation $\sim \text{TMR}/(2 + \text{TMR})V_{DD}$ can be fairly large. Our simulation uses a demonstrated $TMR = 110\%$ ([17]) giving fluctuations up to ∼200 mV at the drain (Fig. 2a), which is much larger than the expected thermal noise at room temperature across a ∼100 aF input capacitance (C) of the inverter: $\sqrt{kT/C} \sim 5$ mV. These large fluctuations in the drain voltage are able to drive the following minimum size inverter from rail-to-rail (Fig. 2b) for a range of input values. The inverter mid-point is designed to be zero by using two supply voltages: $\pm V_{DD}/2 = \pm 0.4$ V. The fluctuations are not rail-to-rail for all values of V_{IN}, as predicted by Eq. 1, but this does not seem to be a crucial requirement for constructing large scale p-circuits, as noted in [6]. Table I summarizes one set of parameters for the the results shown in Fig. 2 which is by no means special. Using circular nanomagnets to achieve a low-barrier free layer allows their diameter to be much larger, until about 100 nm when they are in the monodomain regime [13], [20]. There is no strict requirement on the MTJ resistance, but it is preferable to keep it of the order of tens of $k\Omega$'s so that the MTJ and NMOS on resistance can be conveniently matched. Greater TMR values convert the magnetization fluctuations to even larger voltage swings, reducing the static dissipation on the biased inverter (Fig. 1b) and helping obtain rail-to-rail voltage outputs. We have confirmed by numerical simulations that the results of Fig. 2 remain essentially the same at elevated temperatures (T = 150°C) since there is no "pinning" of magnetization that might have a strong temperature dependence.

We would like to stress that the principle of obtaining the tunable randomness we describe here is not limited to the physics of a stochastic MTJ: Any other unit that produces a stochastic resistance change could be used to obtain the desired behavior [21]. Complementary MOS-like symmetric designs including a PMOS transistor to eliminate the static power dissipation of the p-bit are possible. A comparative energy-delay analysis of such variants will be discussed elsewhere.

Model: The proposed p-bit relies on a fluctuating magnetization giving rise to a measurable resistance difference through the TMR effect. As such, it can be realized using

TABLE I
EXPERIMENTALLY DEMONSTRATED PARAMETERS USED FOR ALL SIMULATIONS

Parameters	Value
Saturation magnetization (CoFeB) (M_s)	1100 emu/cc [22]
Free Layer (FL) diameter (Φ), FL thickness (t)	22 nm, 2 nm
Polarization (P), TMR $[2P^2/(1-P^2)]$	0.59, TMR=110% [17]
MTJ RA-Product ($1/G_0 \times$ Area)	9 $\Omega - \mu m^2$ [17]
Damping coefficient (α)	0.01 [22]
Temperature (T)	26.85 °C
CMOS Models, Size	14nm HP-FinFET [19], nfin=1
Timestep for transient sim. (SPICE)	Δt = 1 ps

different classes of stochastic nanomagnets. Fig. 1 shows three possibilities for free layers: (1) Circular in-plane nanomagnet with a low coercivity ($H_K \ll 1$ Oe) that rotates in the plane, in the presence of thermal fluctuations. Such magnets have been experimentally shown to exhibit monodomain behavior with no preferred axis within sub-100 nm diameters [13]. The other possibilities are: (2) Elliptical in-plane magnets with a coercive field ($H_K \gg 1$ Oe) exhibit telegraphic resistance changes as demonstrated in [14], and (3) Perpendicular magnets that show similar telegraphic behavior, as demonstrated in [15]. In this letter we use the first type, with circular in-plane magnets.

For simplicity, we use a simple, bias-independent MTJ model described by Eq. 3 within the SPICE framework based on [23]. For more detailed simulations, bias-dependence of the MTJ could be included using voltage dependent TMR and polarization data within the same framework [24]–[26]. The stochastic magnetization dynamics is modeled by the stochastic Landau-Lifshitz-Gilbert equation,

$$(1+\alpha^2)d\hat{m}/dt = -|\gamma|\hat{m}\times\vec{H} - \alpha|\gamma|(\hat{m}\times\hat{m}\times\vec{H}) + 1/qN(\hat{m}\times\vec{I_S}\times\hat{m}) + (\alpha/qN(\hat{m}\times\vec{I_S})) \quad (5)$$

where α is the damping coefficient, q is the electron charge, γ is the electron gyromagnetic ratio, $\vec{I_S} = PI_c\,\hat{z}$ is the spin current along the fixed layer ($\hat{z}$), I_c being the charge current flowing through the MTJ. N is the total number of spins in the free layer (CoFeB), $N = M_s\text{Vol.}/\mu_B$, where M_s is the saturation magnetization of CoFeB and μ_B being the Bohr magneton. The spin-current that is incident to the free layer is assumed to be uniformly distributed over the entire volume of the magnet in the macrospin approximation employed here, and therefore normalized by this quantity N. The effective field $\vec{H}$ is given as $-4\pi M_s m_x\hat{x} + \vec{H}_n$, $\hat{x}$ being the out-of-plane direction of the magnet. $\vec{H}_n$ is the isotropic thermal noise field, uncorrelated in three directions: $(H_n^{x,y,z})^2 = 2\alpha kT/(|\gamma|M_s\text{Vol.})$ [Oe^2/Hz].

READ Disturbance: As noted, the operation of the p-bit does not rely on the magnetization being pinned, and we do not see any appreciable pinning with the chosen parameters even when the transistor is fully on. However, depending on $M_s\times$ (Vol.) there could be some pinning but this generally seems to aid the device operation.

Resistor Network Based Synapse: To achieve specific functionalities, the p-bits have to be interconnected into a network in accordance with the synaptic matrix [J] and the bias vector {h} [Eq. (2)]. For this purpose we employ the standard crossbar architecture with a transimpedance amplifier appropriate for driving our high input impedance p-bits [28]. The resistors are chosen to implement specific [J], {h} obtained "offline". The possibility of online memristive learning [29] or capacitive weighting [11] is left for future work.

p-Circuit Implementation of Invertible AND: To demonstrate that our proposed p-bit is suitable for invertible logic, we present an identical example as in [7]. Fig. 3 shows an AND gate (Fig. 4), with the three p-bits representing the inputs A, B and the output C. In the usual forward mode, A and B are clamped to specific values (0 or 1) through the bias vector {h}, and the network makes the p-bit C take on the corresponding value dictated by the AND truth table: {00 → 0}, {01 → 0}, {10 → 0}, {11 → 1}. What is remarkable is the inverse operation: if we clamp

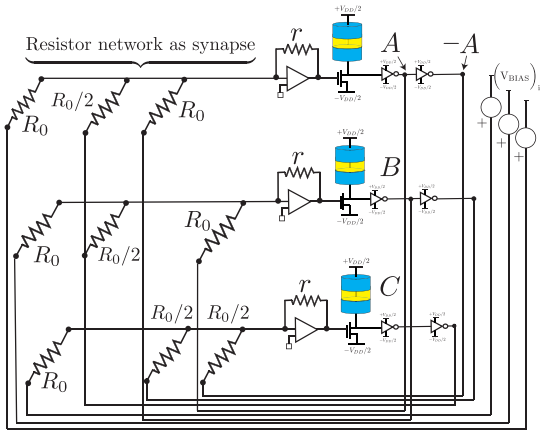

Fig. 3. **Full circuit implementation of an invertible AND gate ($A \cap B \leftrightarrow C$)** using a crossbar array resistor-network and embedded MTJ based neurons. The weights for the AND gate are based on [27]. The current to voltage conversion is made by a transimpedance amplifier achieved by an ideal OP-AMP in our simulations. The inverting nature of the summing amplifier inserts an overall minus sign to the weights. The ratio of resistances r/R_0 controls the interconnection parameters {h}, [J] in Eq. (2).

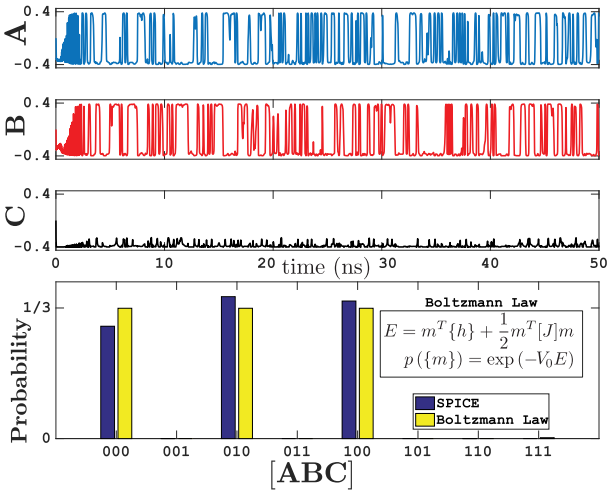

Fig. 4. **SPICE-simulation of invertible AND** Time dependent simulation results for the circuit in Fig. 3. C is clamped to bit 0 and inputs (A,B) fluctuate among three possible configurations. Histogram of the binary word [ABC] obtained from the data in (a), after thresholding by comparison to 0 ($V < 0 \equiv -1$, $V > 0 \equiv +1$). The invertible AND gate here is similar to those discussed in the context of memcomputing [30], [31]. The circuit simulation (for 500 ns) is compared with the Boltzmann Law for a universal model for p-bits whose dimensionless variables (V_0, h_i, [J]) are mapped to the hardware parameters, and results are in good agreement even though we introduced variations: (A, B, C) are assumed to have different TMRs (110%, 118%, 96%), diameters (22, 23.5, 20.5) nm and M_s (1100, 1070, 1130) emu/cc.

C, A and B cycle through the appropriate value(s) *even when the answer is not unique*: {0 → 00, 01, 10}, {1 → 11} (Fig. 4). This invertible operation [7] is particularly interesting because many hard problems like the k-sum [32] problem and factorization are inverses of simpler problems like addition and multiplication respectively.

Conclusion: We propose and evaluate a p-bit that makes minimal modifications to the existing embedded MRAM technology. Large scale integration of this proposed p-bit might enable an emerging computation paradigm that can augment standard CMOS with additional functionalities such as invertible operation.

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