Proposal of a Single Nano-Magnet Memory Device

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***Abstract*— We propose a non-volatile memory device using ferromagnetic (FM) contacts fabricated on a channel exhibiting spin-momentum locking observed in diverse materials with spin-orbit coupling like heavy metals and topological insulators. The writing is enabled by the current induced spin–orbit torque, which has been used previously to switch the storage layer of a magnetic tunnel junction (MTJ). The reading is enabled by a relatively lower current-induced spin voltage measurement through the FM contact, which is high or low depending on the magnetization direction for a particular current direction. This new read mechanism significantly reduces the fabrication difficulties compared with MTJ-based designs. Simpler interconnects and control circuits can be used, since both read and write currents share the same path. Our proposal offers *on-cell* reference voltage generation with a normal metal contact on the channel at the same position as the FM, which is expected to improve the performance in a large array. The estimated read signal based on available materials is smaller compared with MTJ, but the noise is also expected to be smaller in our metallic device compared with those involving tunnel barriers.**

***Index Terms*— MRAM, spin voltage, spin-orbit coupling, spin-momentum locking, spin-orbit torque, spin-transfer torque, self-reference, MTJ.**

I. Introduction

MAGNETORESISTIVE random access memory (MRAM) is one of the emerging memory technologies due to faster read and write, high endurance, and low power consumption [1]–[4]. Conventional MRAM uses two-terminal magnetic tunnel junctions (MTJ), which employ two ferromagnetic (FM) layers (reference and storage) sandwiching a thin oxide barrier [4]–[7]. Usually the storage FM is written with spin-transfer-torque (STT) from a large current flowing through the MTJ [6], [7], leading to large power consumption, possible oxide breakdown, and larger control transistors. These issues were addressed in spin-orbit torque (SOT) driven MRAM where switching of storage FM is achieved by running a current through a material with spin-orbit coupling (SOC) in a direction perpendicular to both the MTJ stack and the storage magnetization direction [2], [8]–[10]. Room temperature switching has been demonstrated with heavy metals (HM) (e.g. Pt [11], Ta [12], and W [13]) and topological insulators (TI) (e.g. Bi_2Se_3 [14]) and switching is reversible by reversal of the current direction. Switching can be achieved with smaller current by adjusting the cross-sectional area of the SOC material without changing the MTJ dimension, which leads to lower write power and smaller transistors as compared to STT MRAM [2]. Both STT and SOT MRAM usually employ a synthetic antiferromagnetic (SAF) reference layer to compensate for dipole field and achieve symmetric write operation [15].

However, most of the state-of-the-art MRAMs rely on the MTJ resistance to read out the storage FM, which is either low or high if it is parallel or anti-parallel to the reference magnetization respectively. Both SOT and STT MRAMs have similar read power consumption as the read current flows through the high resistance MTJ. The performance and lifetime of a MTJ is highly sensitive to the oxide thickness which is subject to process variation in a large array. Pinholes and other defects during the formation of the oxide layer cause additional degradation and often lead to breakdown [16], [17]. Integration with CMOS often over anneals the MTJ [18] causing formation of dead layers, lattice mismatch between magnet and oxide layers etc., which in turn, create challenges in realizing high density memory [19].

In this letter, we propose a new read mechanism in a structure similar to SOT MRAM (see Fig. 1) which replaces the MTJ and associated material layers with only a storage FM contact, thus making the fabrication much simpler. The writing is enabled by the same SOT driven mechanism with large write current. The reading is enabled by relatively lower current (i_c) induced spin voltage in the SOC channel exhibiting high degree of spin-momentum locking (SML) [20], [21]. The spin voltage when measured using the storage FM (V_{fm}) gives either high or low for a particular i_c direction depending on whether the magnetization (m_z) is aligned with the majority or minority spins in the channel respectively. This phenomena has been demonstrated on both HM [22] and TI [23] at room temperature. V_{fm} is compared to a reference (V_{ref}) using a sense amplifier or a comparator to read-out the m_z.

In our proposal, V_{ref} can be generated on-cell by measuring the channel potential with a normal metal (NM) contact at the same position along the channel as the FM contact. We believe such simple on-cell self-referencing will improve the read operation in a large array as it has been shown in the past for MTJ based systems that self-referencing using carefully

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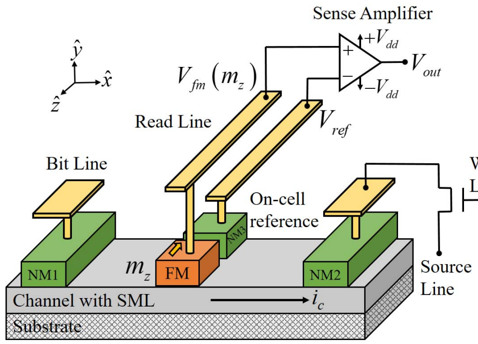

Fig. 1. **Proposed memory device.** The device comprises a ferromagnet (FM) and three normal metal (NM) contacts fabricated on a channel with spin-momentum locking (SML) e.g. heavy metals or topological insulators, which is grown on a substrate like silicon. NM1 is connected to the bit line and NM2 is connected to the source line via a switch, controlled by the word line. The magnetization (m_Z) is read by measuring the current (i_c) induced spin voltage between FM and NM3 using a sense amplifier.

designed external circuitry can overcome bit to bit variations and enhance the read performance [24]–[26]. The estimated read signal in our proposal is smaller as compared to state-of-the-art MTJ and may require amplification. However, the sense noise is expected to be much smaller in our metallic device as compared to MTJ's with high resistance tunnel barrier.

The reading of m_z using spin induced charge signal in SOC materials has been discussed previously [27], [28] which has the same magnitude as our read signal due to Onsager reciprocity [21]. However, in our proposal both read and write operations are enabled by charge current induced spins in the low resistance SML channel, with lower write power consumption than STT and lower read power consumption than both STT and SOT MRAMs. Read and write currents having same path allows us to use interconnections and control circuits similar to that used for STT MRAM but with smaller transistor size. The discussions in this letter are based on in-plane FM that yields lower integration density than magnets with perpendicular anisotropy which we leave for future assesment.

II. Unit Memory Cell

The current i_c in the SML channel flows between two NM contacts NM1 and NM2 (see Fig. 1) where NM1 is connected to the bit line (BL) and NM2 is connected to the source line (SL) via a switch (e.g. MOSFET or MEMS). The switch is turned on or off by a control voltage from the word line (WL). The storage FM (m_z along $\hat{z}$-direction) is deposited along the current path and the distance from FM to NM1 and NM2 are irrelevant for device operation and can be adjusted accordingly. The FM can be written '1' (or '0') i.e. $m_z = +1$ (or -1) by applying a write pulse of amplitude V_{dd} to BL (or SL) while keeping the SL (or BL) to circuit ground, which injects a charge current $|i_c| > I_{c0}$ in the $\hat{x}$ (or $-\hat{x}$) -direction of the SML channel, where I_{c0} is the switching threshold [29].

A. Read Signal

To read-out the FM, we inject $i_c < I_{c0}$ only in the $\hat{x}$-direction by applying a read pulse of amplitude $V_{dd}/8$ at the BL while keeping the SL grounded. The read line (RL) senses the FM open circuit voltage (V_{fm}) which is either high or low depending on $m_z = +1$ or -1, as given by [20], [21]

$$V_{fm}(m_z) = V_{ref} + m_z \frac{\xi p_f p_0}{\pi} R_B i_c, \tag{1}$$

where p_f is the FM polarization, $R_B = h/(q^2 M_t)$ is the ballistic resistance, and M_t is the total number of modes in the channel (q : electron charge, h : Planck's constant). Note that Eq. (1) is valid from ballistic to diffusive regime [21]. We used $i_c \approx 0.5 I_{c0}$ for reading in our example and leave read disturbance analysis and optimization for future work.

Here, p_0 is the degree of SML [20], [21], [30] which is 0 for a NM channel and 1 for a perfect TI. However, p_0 in a real TI effectively gets lowered by the presence of parallel channels. $p_0 \approx \alpha_R k_F/(2E_F) \ll 1$ in a Rashba channel with a coupling coefficient α_R (k_F : Fermi wave vector, E_F : Fermi energy) [20]. Effect described by Eq. (1) has been confirmed and quantified with p_0 by a number of experiments on TI (see [23], [31]–[33]). Such effect has been observed recently on HM [22], [34] and can be quantified with p_0 although the underlying mechanism is subject to debate and could involve either surface [35]–[37] or bulk [12], [38]. Note that the discussions in this letter hold irrespective of the mechanism.

$0 \le \xi \le 1$ takes into account the current shunting in the FM contact where 0 and 1 correspond to high and low shunting respectively [21]. ξ depends on the FM resistance relative to the SML channel resistance and can be estimated experimentally by grounding the FM contact and observing how much of the channel current flows out, as described previously in [21]. Current shunting in metallic FM is high when in direct contact with a high resistive TI and usually a thin oxide is inserted at the interface [23], [31]–[33] to enhance ξ for spin voltage measurement. However, such barrier degrades the spin injection into the FM during the write operation. On the other hand, such shunting is less severe for metallic channels like Pt, Ta and W and the voltage is measurable at room temperature even without any tunnel barrier [22]. This implies efficient read and write in the same structure.

B. Signal Strength

The relative change in V_{fm}/i_c from $m_z = +1$ to -1 is given by $\Delta R_s = 2\xi p_0 p_f R_B/\pi$ from Eq. (1). For 2D channels, $M_t = k_F w/\pi$ (w : channel width) which gives

$$\Delta R_s \cdot w = \frac{\xi p_0 p_f}{k_F} \times 51.8 \text{ k}\Omega, \tag{2}$$

indicating that the signal is higher in a material with lower k_F. For Bi_2Se_3 and Pt, $k_F \approx 1.5$ nm^{-1} [31] and 6.7 nm^{-1} (estimated using $k_F = \sqrt[3]{3\pi^2 n}$ with electron density $n \approx 10^{22}$ cm^{-3} [39]) respectively and $\xi p_0 \approx 0.6$ (estimated from [23]) and 0.05 (estimated from [22]) respectively. With $p_f = 0.58$ [22] we estimate $\Delta R_s \cdot w$ product to be $\sim$12 kΩ-nm and $\sim$0.23 kΩ-nm for Bi_2Se_3 and Pt respectively, which corresponds to $V_{fm}(m_z) - V_{fm}(-m_z) \approx 12$ mV and 0.23 mV respectively for $w = 100$ nm and $i_c = 100$ μA. Roughly we expect the signal in Ta and W to be $\sim$5 and $\sim$10 times higher than Pt respectively, based on experimentally estimated charge to spin conversion efficiency [12], [13]. The signal may require multi-stage amplification and differential sensing similar to static random access memory [40], but we leave such consideration for future work. The noise should also be significantly lower than MTJ based designs [41], [42] since our device is metallic and does not include a high resistance tunnel barrier.

C. On-Cell Self-Referencing

The output (V_{out}) of the sense amplifier is $+V_{dd}$ ($-V_{dd}$) when $V_{fm} > V_{ref}$ ($V_{fm} < V_{ref}$). $V_{ref} = (V_{fm}(m_z) + V_{fm}(-m_z))/2$ which is the voltage measured with a NM contact (NM3) at the same position along the channel as

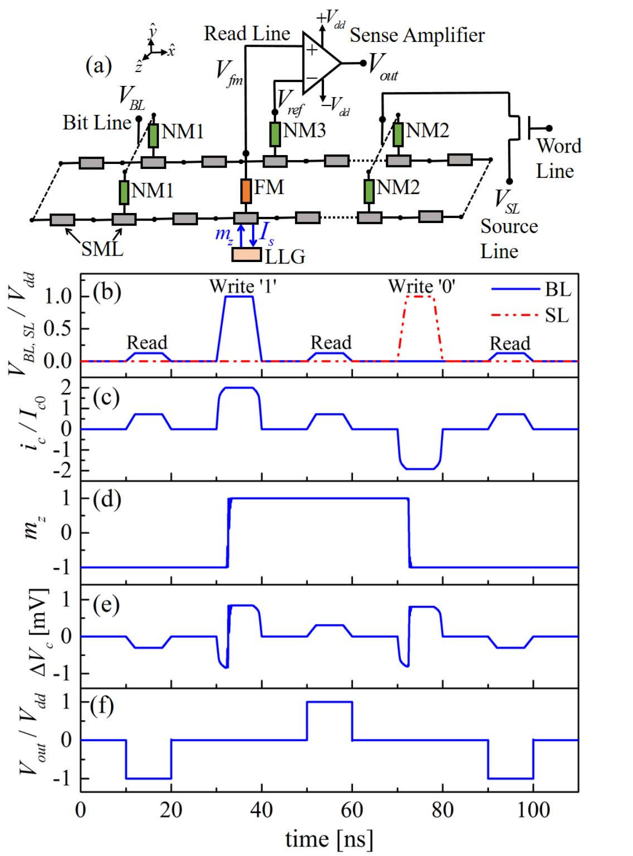

Fig. 2. **Simulation.** (a) SPICE setup for structure in Fig. 1 with 20 discretized blocks. (b) Control voltages V_{BL} and V_{SL} at bit line (BL) and source line (SL) respectively. (c) Channel current i_c due to $V_{BL,SL}$. (d) Magnetization m_z of the ferromagnet (FM). (e) Spin voltage $\Delta V_c = V_{fm}(m_z) - V_{ref}$ induced by i_c. (f) Output of the the sense amplifier. Parameters: $p_f = 0.58$, $M_t = 1050$, scattering rate $= 0.1$ per unit mode per lattice point.

the FM. Note that the spatial separation between FM and NM3 along $\hat{z}$-direction is irrelevant for device operation as long as they do not overlap. However, spatial separation of L_{os} along $\hat{x}$-direction will create a read offset $R_{os} = R_B L_{os}/\lambda$ (λ : channel mean free path) which may cause a read failure if $R_{os} \geq \Delta R_S$ i.e. $L_{os} \geq (2\xi p_0 p_f \lambda)/\pi$. The reference can be a FM as well but with larger length compared to the storage FM so that it does not switch during write operations. This may achieve good alignment i.e. $L_{os} \approx 0$ as material will be deposited at the same time using same mask.

III. Simulation

We have simulated the device using our experimentally benchmarked multi-physics framework [43], [44], which has been previously used to explain a number of experiments and propose new devices [44]. The SPICE setup for the structure in Fig. 1 is shown in Fig. 2(a). The SML channel is constructed using a distributed connection of our two component (charge and spin) model [30] which can have a NM or a FM or no external contact. We have used two of such distributed chains to take into account the channel area under FM and NM3 respectively (along $\hat{z}$-direction). The SML block with FM contact is coupled to a LLG module [43] which solves the Landau-Lifshitz-Gilbert (LLG) equation self-consistently and provides an instantaneous feedback on m_z to the corresponding SML block. Boundaries of both chains are charge open and spin grounded, which is also the boundary conditions for all external contacts. Charge terminals of NM2 in both chains are connected to a 14 nm n-FinFET model [45] with 6 fins, which is kept on by the WL. Charge terminals of NM3 and FM are connected to a differential sense amplifier which is nearly ideal and is active only during read operations. Proper design of such sense amplifiers is left for future assessment.

We assume a $200 \times 100 \times 1.6$ nm^3 CoFeB FM (saturation magnetization $M_S \approx 10^3$ Oe, uniaxial anisotropy field $H_K \approx 10^2$ Oe) with $\Delta_B \approx 40 k_B T$ stability [29] (k_B : Boltzmann constant, T : temperature) on Ta channel. The spin current required to switch is $(8q\pi/h)\Delta_B \alpha_g (1 + 2\pi M_s/H_K) \approx 0.5$ mA [29] with Gilbert damping $\alpha_g \approx 0.008$ [12]. Ratio of spin to charge current densities in Ta is ~ 0.15 [12], which gives a switching threshold of $I_{c0} \approx 0.25$ mA in Ta channel with 500×3 nm^2 cross-section. We assume $\xi p_0 \approx 0.25$ to achieve $\sim$5 times higher spin voltage than estimated for Pt, however, proper extraction of material parameters we leave for future.

The pulse widths are 10 ns with 2 ns of rise and fall time and $V_{dd} = 0.8$ V. We start from an initial condition '0' ($m_z = -1$) of the FM with an initial angle of 5° due to the thermal noise. We apply a read pulse at $t = 10$ ns to the BL which yields i_c induced spin voltage $\Delta V_c = V_{fm}(m_z) - V_{ref} \approx -0.3$ mV and gives $V_{out} = -V_{dd}$ when applied to the sense amplifier (see Fig. 2(b)-(f)). At $t = 30$ ns we apply a write '1' pulse at BL and keep SL at circuit ground, which injects $i_c = 2I_{c0}$ and switches the FM to $m_z = +1$. We apply a second read pulse at $t = 50$ ns which yields $\Delta V_c \approx +0.3$ mV and $V_{out} = +V_{dd}$ indicating $m_z = +1$. At $t = 70$ ns we apply a write '0' pulse to the SL and keep BL at circuit ground, which injects $-1.9I_{c0}$ to switch the FM back to $m_z = -1$. The asymmetry in write current is due to source degeneration similar to STT MRAM [7]. We apply a third read pulse at $t = 90$ ns which yields $\Delta V_c \approx -0.3$ mV and $V_{out} = -V_{dd}$ indicating $m_z = -1$.

IV. Summary

We have proposed a memory device similar to the well-known SOT driven MRAM, except that our new read mechanism based on current induced spin voltage replaces the MTJ and associated material layers with a single FM contact. Simpler interconnects and control circuits can be used since read and write currents share the same metallic path. The proposal enables very simple on-cell self-referencing which is expected to improve the read performance in a large array. The read signal is small compared to MTJ based devices, but the noise is also expected to be smaller in our metallic device as compared to devices with tunnel barriers.

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