Demonstration of 4H-SiC Digital Integrated Circuits Above 800 °C

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***Abstract*— Short-term demonstrations of packaged 4H–SiC junction field-effect transistor (JFET) logic integrated circuits (ICs) at temperatures exceeding 800 °C in air are reported, including a 26-transistor 11-stage ring oscillator that functioned at 961 °C ambient temperature believed unprecedented for electrical operation of a semiconductor IC. The expanded temperature range should assist temperature acceleration testing/qualification of such ICs intended for long-term use in applications near 500 °C ambient, and perhaps spawn new applications. Ceramic package assembly leakage currents inhibited the determination of some intrinsic SiC device/circuit performance properties at these extreme temperatures, so it is conceivable that even higher operating temperatures might be obtained from SiC JFET ICs by employing packaging and circuit design intended/optimized for T $\geq$ 800 °C.**

***Index Terms*— JFET integrated circuits, high-temperature techniques.**

I. Introduction

WIDE bandgap semiconductors theoretically enable hundreds of degrees centigrade (°C) increase in envisioned semiconductor integrated circuit (IC) ambient operating temperature (T) over silicon, and developmental SiC and III-N ICs for T $\geq$ 500 °C have been reported [1]–[18]. Recently, 4H-SiC junction field effect transistor (JFET) ICs with two levels of interconnect have started to consistently demonstrate substantially longer (>1000 hours) operating times at 500 °C [13]–[17], which is a significant step towards beneficial insertion into new applications, including jet engine ground test and Venus surface exploration [18]–[21].

The ability to operationally stress semiconductor devices at temperatures higher than the intended application has proven crucial to reliability assessment and qualification of ICs [22]. Furthermore, expansion of IC operating temperatures can be expected to spawn new applications not presently envisioned. We previously reported shorter-term (< 150 hours) operation of 4H-SiC JFET logic ICs up to 727 °C ambient temperature [13], [16]. Here we report operational testing of similar 4H-SiC JFET ICs at ambient temperatures up to 961 °C.

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TABLE I
T > 800 °C 4H-SiC JFET IC Oven Tests

Test	T Profile	Devices/Circuits
Test #1 Die (12,20) *r*=21mm	Heat to 500°C. 144 hour burn-in. Heat to 966°C. Oven power off. Cool to 25°C.	Metal1 resistor/isolation HF inverting amplifier NOT gate 11-stage inverting amp. ring osc. 11-stage current source ring osc.
Test #2 Die (20,15) *r*=22mm	Heat to 500°C. 116 hour burn-in. Heat to 953°C. Oven power off. Cool to 25 °C.	48μm / 6 μm JFET Inverting amplifier NOT gate Current source NOT gate Inverting amplifier D Flip-Flop
Test #3 Die (16,09) *r*=15mm	Heat to 500°C. 118 hour burn-in. Cool to 25°C Heat to 851°C. Cool to 25°C.	Package isolation/leakage Package conductors 40-square SiC n-resistors Current source NOT, NOR, NAND, and XOR gates

Heating and cooling with oven power on are $\leq$ 3°C/minute.

II. Experimental

A. Procedures

The fabrication process for the 4H-SiC JFET ICs with two levels of interconnect is reported in [14]–[17], except that another wafer (from the same epi-growth run) was processed with modified mask layout (but same 6 μm feature size), the 1360 °C activation anneal was 100 hours duration instead of 4 hours (aimed at improved implant activation), and the contact to SiC was a 50 nm titanuim layer instead of hafnium. It should be noted that parallel fabrication of a wafer with Hf contacts was also attempted, but this wafer suffered a significant processing non-ideality that excluded its use in this study. Therefore, well-controlled comparison of Ti-contact vs. Hf-contact ICs for the extreme T range covered in this report remains to be accomplished.

Three chips, each with a unique set of devices/circuits, were bonded into three custom 32-lead Al_2O_3 ceramic package assemblies originally designed for T $\leq$ 500 °C [23] and wired for extreme T tests conducted in air-atmosphere ovens. The

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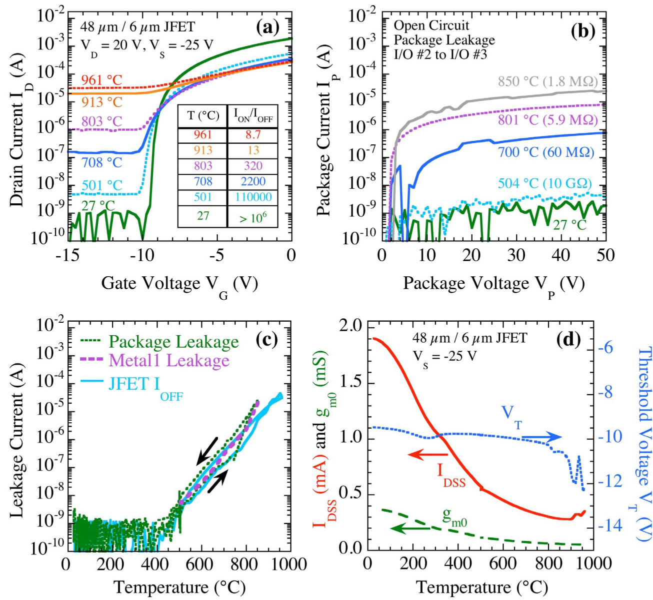

Fig. 1. Measured JFET and 32-pin package/board electrical properties as a function of T. (a) Test #2 JFET turn-off I-V characteristics. (b) Test #3 package/board open circuit leakage I-Vs. (c) Same-plot comparison of leakages of JFET I_{OFF} at $V_D = 20$V and $V_G = -15$V, Metal 1 isolation test device at 35 V, and package/board leakage at 35 V. The fact that all three follow the same behavior indicates that on-chip device leakage data for T > 500 °C are actually package/board shunt leakage currents. (d) Test #2 JFET I_{DSS}, V_T, and g_{m0} vs. T.

test devices and thermal conditions are briefly summarized in Table I. These tests were first attempts at electrically testing ICs with gold-paste die attach introduced in [16] beyond 700 °C. The oven testing setup is not optimized for low noise or high frequency measurements due to large wiring/cabling capacitances and substantial electromagnetic coupling (EMC) of oven heating elements to unshielded gold wires inside the oven [5]. In two tests, ovens were powered off for cool-down to facilitate some measurements without oven EMC.

As we have previously described in [15], circuit "burn-in" effects take place within the first 100 hours of initial chip heating to 500 °C. Therefore, T ≥ 500 °C data reported herein is after more than 100 hours of 500 °C packaged IC burn-in, with the burn-in time variation due to scheduling/logistical issues.

B. JFET, Package and Board, and Resistors

Pre-dicing electrical probe testing of this wafer at 25 °C revealed the same systematic dependence of threshold voltage (V_T) on radial distance *r* from the wafer center as for our prior IC wafer (see [24] for details about this dependence). Fig. 1a shows measured turn-off current vs. voltage (I-V) characteristics of the Test #2 JFET ($r = 22$ mm) at selected temperatures. The approximate ratios of on-state current I_{ON} to off state current I_{OFF} are listed in the Fig. 1a inset. Excellent I_{ON}/I_{OFF} ratio in excess of 2000 is demonstrated through 700 °C, and even above 900 °C the ratio remains viable for implementation of leakage-tolerant circuits.

Fig. 1b shows "open-circuit" leakage currents measured between two adjacent package assembly leads with no bond

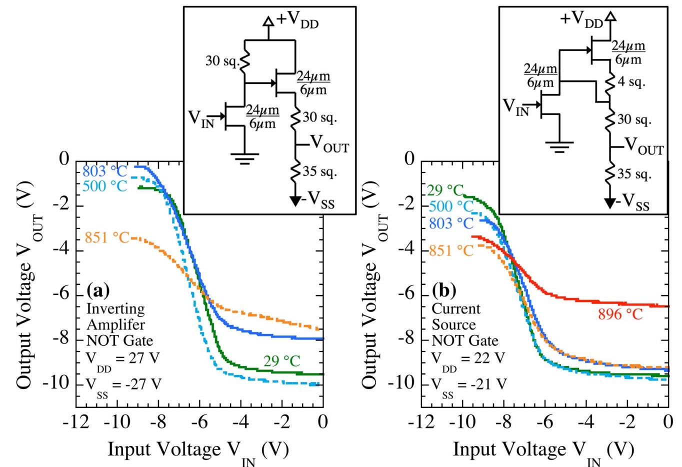

Fig. 2. Low-frequency NOT gate voltage transfer characteristics measured at selected temperatures in Test #2 for the two logic circuit designs shown in the insets. (a) Inverting amplifier design, and (b) current source design. Both logic designs function from room temperature through 800 °C without change to power supply or input signal voltages.

wire connections during last cooling of Test #3. Above measurement setup noise floor, open-circuit I-V's are roughly linear with resistance values listed in Fig. 1b. The fact that Fig. 1a JFET I_{OFF} values fall close to Fig. 1b package/board leakages indicates that measured JFET I_{OFF} data for T > 500 °C may actually be package assembly leakage. This hypothesis is supported by Fig. 1c that directly compares measured T-dependence of JFET I_{OFF} at $V_D = 20$ V and $V_G = -15$ V (35 V bias difference), package assembly leakage and a Metal 1 isolation diagnostic device [24] at comparable adjacent lead bias of 35 V. Above 500 °C, the measured leakages are comparable and exponential in temperature ($I \sim 2 \times 10^{-16} e^{0.022T}$ A). However, the Fig. 1c data (except Metal 1 isolation measured during heating only) exhibit hysteresis between heating and cooling, with an average T-down sweep/T-up sweep current ratio of ~3.

Fig. 1d plots measured T dependence of JFET saturation current I_{DSS}, V_T and tranconductance g_{m0} across more than 900 °C temperature spread. The behavior prior to package assembly leakage interference (i.e., leakages that interfere with JFET parameter extractions from measured I-V data) arising near 900 °C is quantitatively consistent with expected behavior [24], [25]. 4H-SiC n-type resistor measurements likewise extend T ≤ 500 °C trends [24], with sheet resistance increasing from 3.8 kΩ/square at 25 °C to 24 kΩ/sq. at 700 °C. Above 300 °C, T^2 (T in Kelvin) power law resistance behavior is followed until package assembly leakages begin shunting 40-square IC resistances approaching 750 °C.

C. Logic Circuits

Two different SiC JFET logic circuit approaches were tested [26], [27], the schematics of which are shown in Fig. 2 along with NOT logic gate low-frequency voltage transfer characteristics at selected temperatures during Test #2. As shown in Fig. 2, these logic circuits function from room temperature to T > 800 °C without adjustment to power supply and/or signal input voltages. Measured gate power under 50%

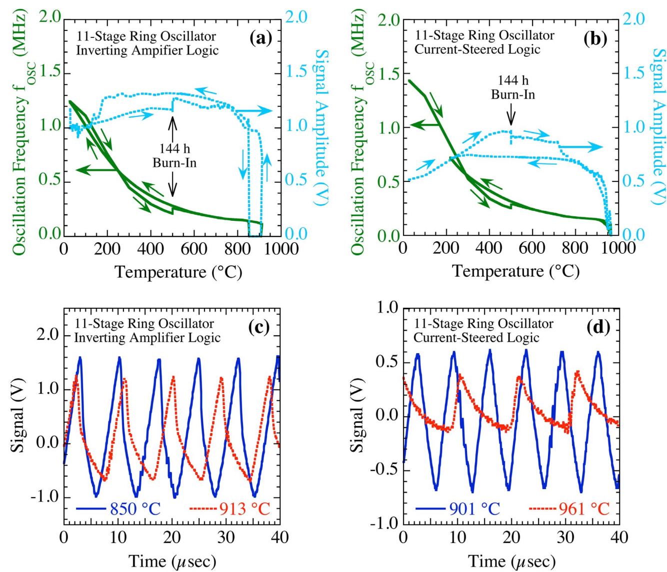

Fig. 3. 11-stage ring oscillator data from Test #1. (a) Inverting amplifier design and (b) current source design signal frequency (solid green) and amplitude (dashed blue) measured in Test #1. (c) & (d) Waveforms recorded at (dashed red) and near (solid blue) peak observed oscillation temperature. Loading effects distort/reduce measured oscillator signals (see text).

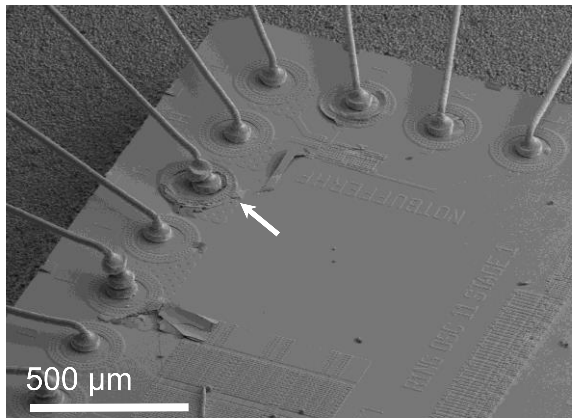

Fig. 4. Electron micrograph of Test #1 chip section tested up to 966 °C. Almost all wires remained functionally intact along with bonds, die attach, and package. The damage to metal traces seen in the above image was correlated to oxide damage that initiated during wire bonding to the pad denoted by the arrow.

cycle 0 V to -10 V square wave input wave declined from 20 mW at 29 °C to 11 mW at 804 °C for the Fig. 2a inverting amplifier circuit, while the Fig. 2b current source circuit dropped from 14 mW to 8 mW. Above 800 °C, package assembly leakage and 10 MΩ oscilloscope probe loading (i.e., connections external to the chip) contribute to reduction in measured logic output swing and increase in power dissipation. It should be noted that there is an extra diagnostic package connection to the inverting amplifier circuit (i.e, extra package assembly leakage source) that degrades its high temperature characteristics.

Two 11-stage ring oscillator circuits (each with 26 JFETs including two output buffer gates) were implemented based on the NOT gate designs of Fig. 2. For output buffers, JFETs were 192 μm / 6 μm and resistors were 6.4, and 7.5 squares for the Fig. 2a inverting amplifier version and 1, 6.4, and 7.5 squares for the Fig. 2b current source version. Figs. 3a and 3b show measured frequency (solid green) and amplitude (dashed blue) of these ring oscillators recorded during Test #1. Waveforms recorded at/near peak circuit oscillation temperature are shown in Figs. 3c and 3d. Given circuit output resistance and frequency, waveforms are substantially affected by capacitive loading from the setup wiring and oscilloscope probes [21], [28]. However, as the output buffer stages effectively isolate the 11 gates in the feedback loop from external circuit leakages, the propagation of internal ring signal is much less affected by packaging/wiring leakage/loading. Therefore, ring oscillators function at higher T and are a better indicator of intrinsic (internal) IC signal propagation than discrete logic gate tests.

Additional circuits listed in Table I demonstrated T > 800 °C operation. It is worth noting that some tested devices suffered electrical failure during cooldown at temperatures well below peak demonstrated operating temperature. For example, the Fig. 3b ring oscillator failed at 203 °C during cooldown.

D. Microscopy

Fig. 4 shows a post-test electron micrograph of part of the chip in Test #1, including circular gold-capped "IrIS" bond pads [29], gold bond wires, and a logic gate in the chip corner that experienced sudden electrical failure between 847 °C and 850 °C during heating to 966 °C peak T. Despite gold bond wire "bamboo" re-structuring [30], all but one studied post-test bond wires were functionally intact without physical opens or sag-induced shorts. Fig. 4 also shows examples of substantial damage to metal traces that were correlated to oxide damage initiated at a non-ideal wire bond (to the pad denoted by the arrow). However, microscopic evidence of degradation was not ascertained in some failed circuits, such as the Fig. 3b oscillator.

III. Conclusion

While 4H-SiC properties enable 961 °C JFET operation, a packaged 961 °C oscillator IC demonstration is not possible without all links in the "back end" technology chain (e.g., contacts, interconnect dielectrics and metals, bonding pads and wires, die attach, and ceramic packaging) performing their desired function (at least briefly and adequately) at this extreme temperature. It is conceivable that higher temperature operation of 4H-SiC ICs from this wafer might be attained if packaging intended for T > 800 °C is developed and employed. Also, circuits designed to withstand larger package assembly leakages could be implemented.

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