200 V Enhancement-Mode p-GaN HEMTs Fabricated on 200 mm GaN-on-SOI With Trench Isolation for Monolithic Integration

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***Abstract*— Monolithic integration of a half bridge on the same GaN-on-Si wafer is very challenging because the devices share a common conductive Si substrate. In this letter, we propose to use GaN-on-SOI (silicon-on-insulator) to isolate the devices by trench etching through the GaN/Si(111) layers and stopping in the SiO_2 buried layer. By well-controlled epitaxy and device fabrication, high-performance 200 V enhancement-mode (e-mode) p-GaN high electron mobility transistors with a gate width of 36 mm are achieved. This letter demonstrates that by using GaN-on-SOI in combination with trench isolation, it is very promising to monolithically integrate GaN power systems on the same wafer to reduce the parasitic inductance and die size.**

***Index Terms*— p-GaN, AlGaN/GaN HEMTs, GaN-on-SOI, 200V, trench isolation, monolithic integration.**

I. Introduction

MONOLITHIC integration of GaN power systems on a single chip is very promising due to its advantages of suppressing parasitic inductance, decreasing die size, and increasing the flexibility for design [1]. For monolithic integration of a half bridge, one of the most important requirements is to isolate the substrates of the high-side and low-side devices because they need to be connected to the respective sources of the devices and biased differently (Fig. 1(a)). Therefore, it's very challenging to achieve monolithic integration of HEMTs on GaN-on-Si, because those HEMTs share a common conductive Si substrate. Without isolating the substrates, the HEMT cannot function properly while biasing the common Si substrate (Fig. 1(b)). Presently, most GaN power systems are fabricated based on a multi-chip solution, which results in high complexity and high cost [2]–[4]. This problem can be solved with GaN-on-SOI (silicon-on-insulator) using a trench isolation process, i.e. etching through the GaN/Si(111) to the SiO_2 buried layer to fully isolate the devices. As a new technique, GaN-on-SOI was first reported for a higher crystal quality related with the compliant effect of the SOI wafer [5]. Next, the first on-wafer integration of Si MOSFETs (metal-oxide-semiconductor field-effect transistors) and GaN HEMTs was demonstrated by bonding [6]. Later, a current mirror circuit was successfully fabricated [7]. Recently, high-voltage GaN HEMTs have also been reported on this platform [8], [9].

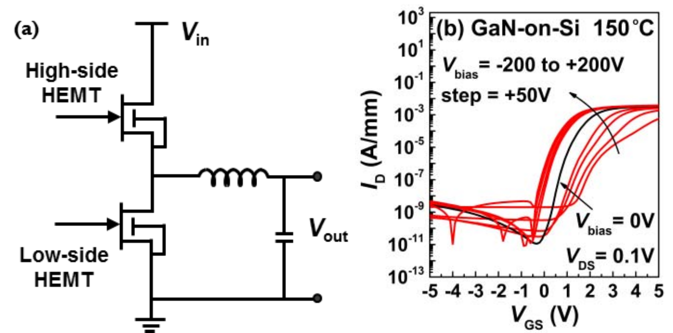

Fig. 1. (a) Simplified circuit of a half bridge and (b) transfer characteristics of a HEMT on GaN-on-Si with the common Si substrate biased from −200 to 200 V at 150 °C. Both serious shifts of threshold voltage (V_{th}) and drive current are observed while biasing the Si substrate negatively.

In this letter, we present 200 V e-mode p-GaN HEMTs fabricated on 200 mm GaN-on-SOI for monolithic integration. The full isolation of the devices was achieved by trench etching, and the normal functioning of the devices was verified when the neighboring substrate was biased from −200 to 200 V. In addition, the DC performance of the devices is also comparable with that of GaN-on-Si. This work demonstrates the possibility of monolithic integration of GaN power systems on the same GaN-on-SOI wafer.

II. Epitaxy and Device Fabrication

The SOI substrate used in this work consists of a 1070 μm Si(100) handling wafer, a 1 μm SiO_2 buried layer,

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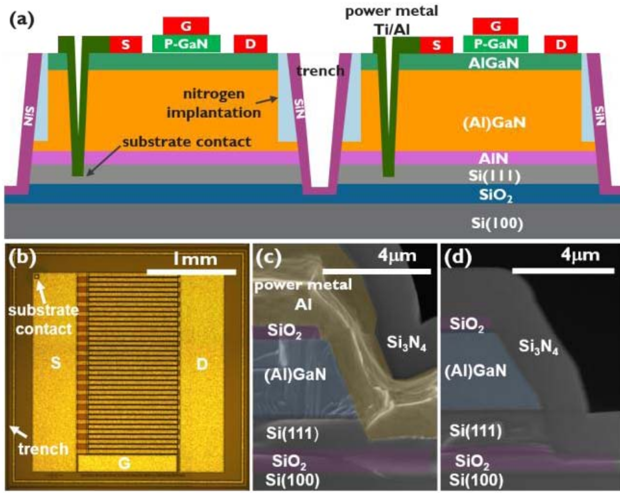

Fig. 2. (a) Schematic cross-section of the e-mode p-GaN HEMT, (b) the top view of the fabricated device, and cross-section Secondary Electron Microscopy (SEM) micrographs of (c) the substrate contact and (d) the trench isolation fabricated on 200 mm GaN-on-SOI.

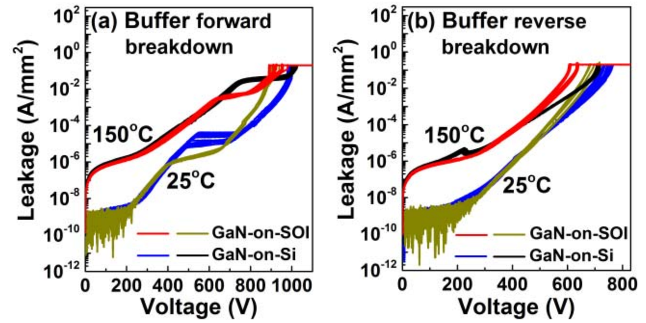

Fig. 3. Distribution of the (a) forward and (b) reverse bias vertical buffer leakage characteristics of the 200 mm GaN-on-SOI and GaN-on-Si at 25 °C and 150 °C.

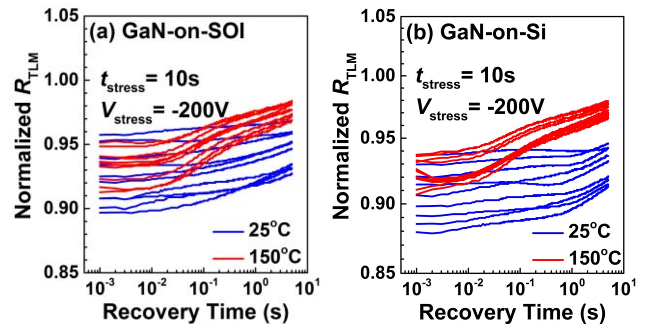

Fig. 4. Distribution of the buffer dispersion over the 200 mm (a) GaN-on-SOI and (b) GaN-on-Si wafers at 25 °C and 150 °C after applying a substrate stress voltage of −200 V and a stress time of 10 s.

and a 1.5 μm Si(111) device layer. The thickness of SiO_2 is determined by considering both breakdown voltage and thermal resistance of the wafer. The device stack was epitaxially grown on the 200 mm SOI wafer using metalorganic chemical vapor deposition (MOCVD). The growth and characterization details were as described in previous publications [10], [11]. The epi stack consists of (from bottom to top) a 200 nm AlN nucleation layer, a 2.6 μm (Al)GaN buffer layer, a 300 nm GaN channel layer, a 12.5 nm $Al_{0.25}Ga_{0.75}$ N barrier layer, and an 80 nm Mg-doped p-GaN layer. An in-situ annealing of the p-GaN layer was conducted in N_2 ambient after the epitaxy to result in a hole concentration of around 1×10^{18} cm^{-3}. The detailed (Al)GaN superlattice buffer has also been discussed in a previous publication [12]. Delicate strain engineering was carried out in order to control the stress during the epitaxy and to avoid excessive wafer warp. The optimized epi stack showed a high structural quality with wafer warpage well below 50 μm and a smooth surface with a root-mean-square (RMS) roughness of 1.4 nm ($5\times5\mu$m^2) measured with Atomic Force Microscopy. The (Al)GaN buffer thickness of the GaN-on-Si reference wafer was adjusted to 2.69 μm in order to keep the wafer warp within specification.

The e-mode p-GaN HEMTs were processed using Au-free process modules for ohmic contacts and metal interconnects [13]. A TiN/p-GaN stack was used for the gate [14]. Nitrogen implantation was used for horizontal isolation. After the fabrication of devices, the substrate contact (50μm $\times$ 50μm) was processed by etching through the (Al)GaN to the Si(111) device layer, followed by Ti/Al sputtering for the power metal to connect the Si(111) with the source. Next, the trench isolation (20 μm width) was processed by etching through the (Al)GaN/Si(111) to the SiO_2 buried layer. Finally, a back-end passivation layer was deposited. The device processing of GaN-on-Si and GaN-on-SOI is identical, except no trench or substrate contact was processed on GaN-on-Si. Fig. 2 shows the schematic of the device, substrate contact, and trench isolation. The power devices have a gate width W_G of 36 mm, a gate length L_G of 0.8 μm, a gate-source distance L_{GS} of 0.75 μm, and a gate-drain distance L_{GD} of 6 μm.

III. Results and Discussion

The buffer quality of GaN-on-SOI was first evaluated. Fig. 3 shows similar forward and reverse vertical buffer leakage for GaN-on-SOI in comparison with GaN-on-Si at 25 °C and 150 °C. During the measurement, the Si(111) device layer, instead of the Si(100) handling layer, was grounded. Furthermore, the buffer dispersion of both GaN-on-SOI and GaN-on-Si is limited to $\sim$ 10% as shown in Fig. 4. A TLM (transfer length method) structure with a spacing of 10 μm between the cathode and anode terminals was used to measure the buffer dispersion. During the measurement, the Si(111) device layer was first stressed at −200 V for 10 s and then a voltage of 1 V was applied on the anode to monitor the recovery of the TLM resistance over time. The buffer dispersion might be related to the ionization of donor traps in the buffer [15].

Fig. 5 summarizes the transfer characteristics of the devices at 25 °C and 150 °C. Both wafers show fully e-mode devices with a threshold voltage of around 1.6 V. Further measurements (Fig. 6) also show that the HEMTs on GaN-on-SOI feature a low ON-resistance R_{on} around 10.8 Ω·mm (@V_{DS} = 0.1 V and V_{GS} = 7 V) which is comparable with the value of 10.6 Ω·mm of the HEMTs on GaN-on-Si. On both substrates, the maximum drain current at V_{GS} = 7 V of 36 mm-wide power devices reach 9 A.

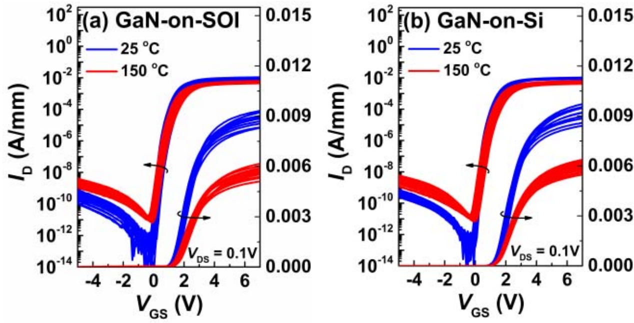

Fig. 5. Distribution of the transfer characteristics of the 36 mm-wide e-mode p-GaN power HEMTs on 200 mm (a) GaN-on-SOI and (b) GaN-on-Si at 25 °C and 150 °C.

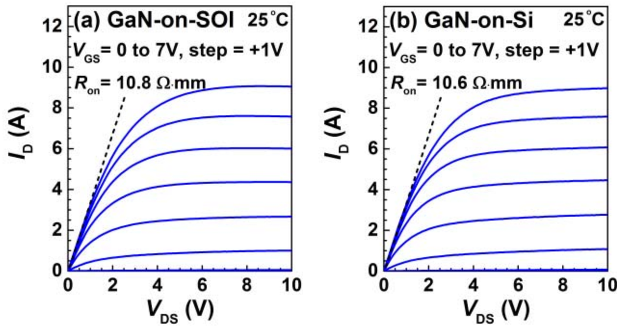

Fig. 6. Output characteristics of the 36 mm-wide e-mode p-GaN power HEMTs on 200 mm (a) GaN-on-SOI and (b) GaN-on-Si at 25 °C.

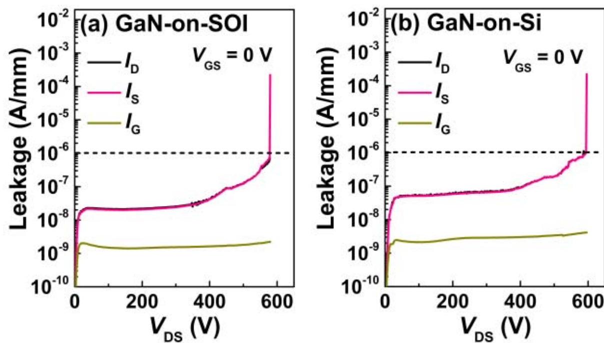

Fig. 7. OFF-state breakdown characteristics (V_{GS} = 0 V) of the 36 mm-wide e-mode p-GaN power HEMTs on 200 mm (a) GaN-on-SOI and (b) GaN-on-Si at 25 °C with the substrate grounded.

The OFF-state ($V_{GS} = 0$ V) breakdown characteristics of the devices ($L_{GD} = 6\mu$m) at 25 °C are shown in Fig. 7. At the leakage current criterion of 1 μA/mm, the 36 mm-wide power devices on GaN-on-SOI and GaN-on-Si both have a breakdown voltage of around 600V, which is able to satisfy the requirements for 200 V switching applications with sufficient margin.

The stability of the device isolation by the surrounding trench on GaN-on-SOI was further verified as shown in Fig. 8. It shows that the horizontal breakdown voltage of the trench isolation reaches ~700 V at 150 °C (Fig. 8(a)), and both the forward and reverse vertical breakdown voltage of the SiO_2 buried layer exceeds ~ 500 V at 150 °C (Fig. 8(b)).

Finally, the effectiveness of device isolation by trench etching on GaN-on-SOI was evaluated. Fig. 9(a) and (b) show

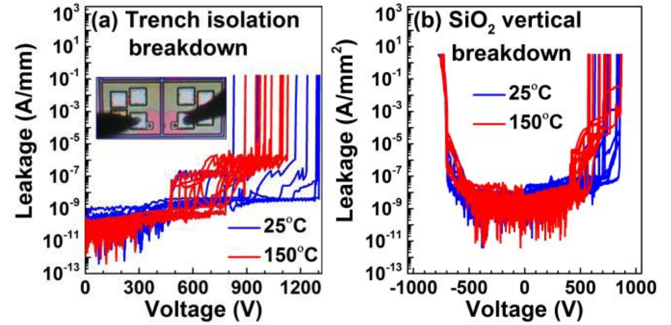

Fig. 8. Distribution of the (a) horizontal leakage of the trench isolation and (b) vertical leakage of the SiO_2 buried layer over the 200 mm GaN-on-SOI at 25 °C and 150 °C.

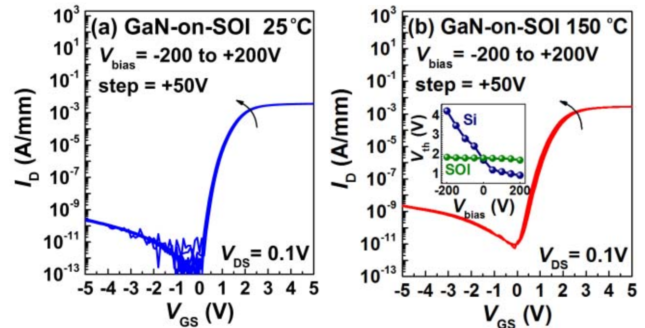

Fig. 9. Evaluation of the device isolation on GaN-on-SOI by measuring the transfer characteristics of a device while simultaneously biasing the neighboring Si(111) device layer at different voltages at (a) 25 °C and (b) 150 °C. The inset shows the V_{th} as a function of different substrate bias for GaN-on-SOI and GaN-on-Si at 150 °C.

that the transfer characteristics of a device on GaN-on-SOI, fully isolated by the trench isolation, are very robust when the substrate of the neighbouring device is biased between −200 and 200 V. This is in clear contrast to the performance degradation of the device on GaN-on-Si as shown in the inset of Fig. 9(b). With the demonstrated high-quality device isolation, it is very promising to achieve monolithic integration of GaN power system on GaN-on-SOI, and further explore the potentials of GaN in the field of high power applications.

IV. Conclusion

High-performance 200 V e-mode p-GaN HEMTs were successfully fabricated on 200 mm GaN-on-SOI substrates. Full device isolation by trench etching on GaN-on-SOI for monolithic integration was proposed and verified in this letter. Our work demonstrates that HEMTs on GaN-on-SOI combined with trench isolation is promising for monolithically integrating GaN power systems on the same wafer to reduce parasitic inductance and die size.

References

[1] D. Reusch, J. Strydom, and J. Glaser, "Improving high frequency DC-DC converter performance with monolithic half bridge GaN ICs," in *Proc. IEEE Energy Convers. Congr. Expo. (ECCE)*, Sep. 2015, pp. 381–387, doi: 10.1109/ECCE.2015.7309713.

[2] T. Nomura, M. Masuda, N. Ikeda, and S. Yoshida, "Switching characteristics of GaN HFETs in a half bridge package for high temperature applications," *IEEE Trans. Power Electron.*, vol. 23, no. 2, pp. 692–697, Mar. 2008, doi: 10.1109/TPEL.2007.915671.

[3] T. Morita, S. Tamura, Y. Anda, M. Ishida, Y. Uemoto, T. Ueda, T. Tanaka, and D. Ueda, "99.3% efficiency of three-phase inverter for motor drive using GaN-based gate injection transistors," in *Proc. IEEE Appl. Power Electron. Conf.*, Mar. 2011, pp. 481–484, doi: 10.1109/APEC.2011.5744640.

[4] M. Ishida, T. Ueda, T. Tanaka, and D. Ueda, "GaN on Si technologies for power switching devices," *IEEE Trans. Electron Devices*, vol. 60, no. 10, pp. 3053–3059, Oct. 2013, doi: 10.1109/TED.2013.2268577.

[5] J. Cao, D. Pavlidis, Y. Park, J. Singh, and A. Eisenbach, "Improved quality GaN by growth on compliant silicon-on-insulator substrates using metal organic chemical vapor deposition," *J. Appl. Phys.*, vol. 83, no. 7, pp. 3829–3834, Apr. 1998, doi: 10.1063/1.366613.

[6] J. W. Chung, J. Lee, E. L. Piner, and T. Palacios, "Seamless on-wafer integration of GaN HEMTs and Si(100) MOSFETs," *IEEE Electron Device Lett.*, vol. 30, no. 10, pp. 1015–1017, Oct. 2009, doi: 10.1109/LED.2009.2027914.

[7] W. Hoke, R. V. Chelakara, J. P. Bettencourt, T. E. Kazior, J. R. LaRoche, T. D. Kennedy, J. J. Mosca, A. Torabi, A. J. Kerr, H.-S. Lee, and T. Palacios, "Monolithic integration of silicon CMOS and GaN transistors in a current mirror circuit," *J. Vac. Sci. Technol. B, Microelectron., Nanom. Struct.*, vol. 30, no. 2, pp. 02B101-1–02B101-6, Mar. 2011, doi: 10.1116/1.3665220.

[8] Q. Jiang, C. Liu, Y. Lu, and K. J. Chen, "1.4-kV AlGaN/GaN HEMTs on a GaN-on-SOI platform," *IEEE Electron Device Lett.*, vol. 34, no. 3, pp. 357–359, Mar. 2013, doi: 10.1109/LED.2012.2236637.

[9] Q. Jiang, C. Liu, Y. Lu, and K. J. Chen, "High-voltage enhancement/depletion-mode AlGaN/GaN HEMTs on modified SOI substrates," in *Proc. 25th ISPSD*, May 2013, pp. 407–410, doi: 10.1109/ISPSD.2013.6694431.

[10] M. Zhao, Y. Saripalli, P. K. Kandaswamy, H. Liang, A. Firrincieli, S. Decoutere, and E. Vancoille, "Growth and characterization of DH-HEMT structures with various AlGaN barriers and AlN interlayers on 200 mm Si(111) substrates," *Phys. State Solid C*, vol. 11, nos. 3–4, pp. 446–449, Apr. 2014, doi: 10.1002/pssc.201300478.

[11] M. Zhao, H. Liang, P. K. Kandaswamy, M. Van Hove, R. Venegas, E. Vranken, P. Favia, A. Vanderheyden, D. Vanhaeren, Y. N. Saripalli, S. Decoutere, and R. Langer, "MOCVD growth of DH-HEMT buffers with low-temperature AlN interlayer on 200 mm Si (111) substrate for breakdown voltage enhancement," *Phys. State Solid C*, vol. 13, nos. 5–6, pp. 311–316, May 2016, doi: 10.1002/pssc.201510280.

[12] D. Marcon, Y. N. Saripalli, and S. Decoutere, "200mm GaN-on-Si epitaxy and e-mode device technology," in *Proc. IEEE Int. Electron Devices Meeting*, Washington, DC, USA, Dec. 2015, pp. 16.2.1–16.2.4, doi: 10.1109/IEDM.2015.7409709.

[13] M. Van Hove, S. Boulay, S. R. Bahl, S. Stoffels, X. Kang, D. Wellekens, K. Geens, A. Delabie, and S. Decoutere, "CMOS process-compatible high-power low-leakage AlGaN/GaN MISHEMT on silicon," *IEEE Electron Device Lett.*, vol. 33, no. 5, pp. 667–669, May 2012. DOI: 10.1109/LED.2012.2188016

[14] T.-L. Wu, D. Marcon, S. You, N. Posthuma, B. Bakeroot, S. Stoffels, M. Van Hove, G. Groeseneken, and S. Decoutere, "Forward bias gate breakdown mechanism in enhancement-mode p-GaN gate AlGaN/GaN high-electron mobility transistors," *IEEE Electron Device Lett.*, vol. 36, no. 10, pp. 1001–1003, Aug. 2015, doi: 10.1109/LED.2015.2465137.

[15] C. Zhou, Q. Jiang, S. Huang, and K. J. Chen, "Vertical leakage/breakdown mechanisms in AlGaN/GaN-on-Si devices," *IEEE Electron Device Lett.*, vol. 33, no. 8, pp. 1132–1134, Aug. 2012. DOI: 10.1109/LED.2012.2200874