600 V/1.7 Ω Normally-Off GaN Vertical Trench Metal–Oxide–Semiconductor Field-Effect Transistor

Ray Li, Yu Cao, Mary Chen, and Rongming Chu

***Abstract*— This letter reports a GaN vertical trench metal–oxide–semiconductor field-effect transistor (MOSFET) with normally-off operation. Selective area regrowth of n^+-GaN source layer was performed to avoid plasma etch damage to the p-GaN body contact region. A metal-organic-chemical-vapor-deposition (MOCVD) grown AlN/SiN dielectric stack was employed as the gate "oxide". This unique process yielded a 0.5-mm^2-active-area transistor with threshold voltage of 4.8 V, blocking voltage of 600 V at gate bias of 0 V, and on-resistance of 1.7 Ω at gate bias of 10 V.**

***Index Terms*— GaN, vertical transistor, MOSFET, power semiconductor devices.**

I. Introduction

DUE to the high electron mobility and the high breakdown strength of GaN, there has been significant interest in developing GaN transistors for power electronics applications [1]. Conventional GaN transistors have a lateral device structure. With excellent performance in high-speed and high-voltage power switching [2]–[4], GaN lateral transistors are strong competitors for voltage/current ratings below 600V/100A. For higher voltage/current ratings, vertical devices are preferred because: (1) chip area utilization is more efficient; (2) device operation is less sensitive to surface trapping.

There have been reports on pioneering work in the area of GaN vertical transistors [5]–[12]. Two kinds of gate structure have been reported. One is the current-aperture-vertical-electron-transistor (CAVET) structure [5]–[7], which is similar to the Si vertical-double-diffused-metal-oxide-semiconductor (V-DMOS) structure. The other one is the vertical trench MOSFET structure [8]–[12]. The CAVET structure has the gate placed on the semiconductor surface. Gate structures developed for lateral GaN transistors can be readily utilized by the CAVET structure. State-of-the-art GaN CAVET has a breakdown voltage of 1.5 kV, an on-resistance (R_{ON}) of 1.5 Ω, and a threshold voltage (V_{th}) of 0.5 V [7]. A negative gate bias (V_{GS}) of −5 V was applied to completely pinch-off the channel for high voltage blocking; and a positive gate bias of 4 V was applied to measure the on-resistance. Trench MOSFET has the advantage of high packing density, and therefore low on-resistance. State-of-the-art GaN trench MOSFET has a breakdown voltage of 1.3 kV, a R_{ON} of 0.19 Ω, and a V_{th} of 3.5V [11]. A negative V_{GS} of −10 V was applied to measure the blocking voltage; and a positive gate bias of +40V was applied to measure the on-resistance.

In this letter, we report a GaN trench MOSFET with a blocking voltage of 600 V, and a R_{ON} of 1.7 Ω. 600V blocking was achieved when the V_{GS} was 0 V; and the transistor was fully turned on at the V_{GS} of 10 V. The V_{th} of this transistor is 4.8 V. A gate bias swing of 0∼10 V is preferable for most gate driver circuits. A V_{th} of 4.8V provides desirable noise immunity to prevent false turn-on. These device characteristics were enabled by an AlN/SiN gate dielectric process, and a source regrowth process to allow proper body contact.

II. Device Fabrication

Fig. 1 shows major process steps for fabricating the GaN vertical trench MOSFET. The process started with metal-organic-chemical-vapor-deposition (MOCVD) growth of n^--GaN drift layer and p-GaN base layer on a bulk GaN substrate. The drift layer is about 8 μm thick. Growth condition for the drift layer has been described in Ref. 13 and 14. It has a Si doping concentration of $1\sim2\times10^{16}$ cm^{-3}, as determined by secondary-ion-mass-spectroscopy (SIMS). Capacitance-voltage (CV) measurements yielded a net electron concentration of $\sim5\times10^{15}$ cm^{-3}. Discrepancy between Si concentration and net electron concentration can be attributed to compensation centers such as carbon impurities [13]. The base layer is about 800 nm thick. It has a Mg concentration of $\sim2\times10^{18}$, as determined by SIMS.

On top of the base layer, a selective area regrowth of n^+-GaN was performed, using patterned SiO_2 as the regrowth mask. The n^+-GaN is 200∼400 nm thick, with the Si concentration of $\sim5\times10^{18}$ cm^{-3}. After that, 2-μm-wide gate trenches were formed by Cl-based ICP etch, using another layer of patterned SiO_2 as the etch mask. The wafer was then subject to a Tetra-Methyl-Ammonium-Hydroxide (TMAH) wet etching treatment to clean etched surface and to smooth gate trench sidewall surface [15]. Region outside of the device active area received the same etch as the gate trench etch, plus an additional implantation step to reduce the surface leakage. After that, an AlN/SiN dielectric stack, similar to what we used for our GaN lateral transistor [3], [16], [17], was grown by MOCVD. The dielectric growth conditions were adjusted to improve step coverage over the gate trench. On the planar surface, the AlN/SiN stack has a thickness of 20/50 nm, as calibrated by ellipsometer measurement and confirmed by TEM. On the lower portion of the gate trench

Manuscript received August 24, 2016; revised September 20, 2016; accepted September 21, 2016. Date of current version October 21, 2016. The information, data, and work were supported in part by the ARPA-E SWITCHES Program under contract DE-AR000450, managed by Dr. Tim Heidel and Dr. Isik Kizilyalli. The review of this letter was arranged by Editor T. Egawa.

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Digital Object Identifier 10.1109/LED.2016.2614515

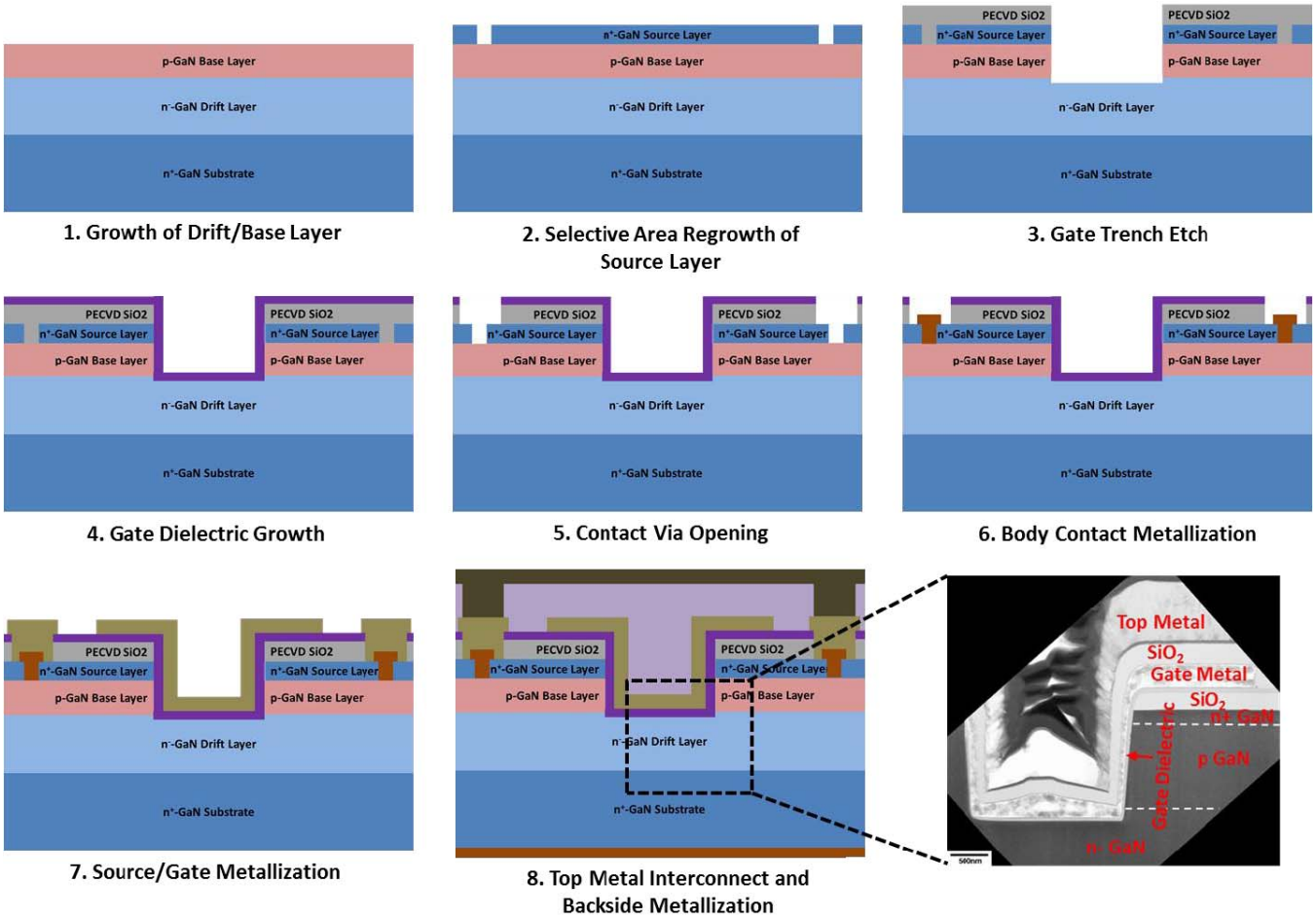

Fig. 1. Major process steps of fabricating the GaN vertical trench MOSFET; TEM cross-sectional image of the gate region of a fabricated device.

sidewall, the total thickness of the AlN/SiN stack is 50 nm, according to the TEM. TEM didn't provide enough contrast to determine the thicknesses of the individual layers. Activation annealing of p-GaN layer at 850 °C in N_2 ambient was performed after each MOCVD step.

After the gate dielectric deposition, contact via were opened by dry etching through the gate dielectric, then Buffered-oxide-etchant (BOE) wet etching through the underlying SiO_2. This process avoids the exposure of the p-GaN surface to plasma dry etching, which is often detrimental to the formation of p-GaN ohmic contact [18]. Body contact to the p-GaN base layer was formed by alloying Ni/Au. Using this method, we achieved a contact resistance of around 1 mΩ-cm^2 to the p-GaN base layer, as measured by TLM. After the body contact metallization, Ti/Al metal stack was deposited and patterned to form both the source and the gate electrodes, with the source electrode overlaying the body contact.

After the source/gate metallization, a Ti/Ni/Au stack was deposited on the backside of the wafer as the drain electrode. Ti/Au source metal interconnect was formed on the front side, using another SiO_2 layer as the inter-metal dielectric. Cross-sectional transmission-electron-microscope (TEM) image of the gate structure is shown in Fig. 1. The dashed blue lines denote the source/base and base/drain junctions, which are not clearly visible in this TEM.

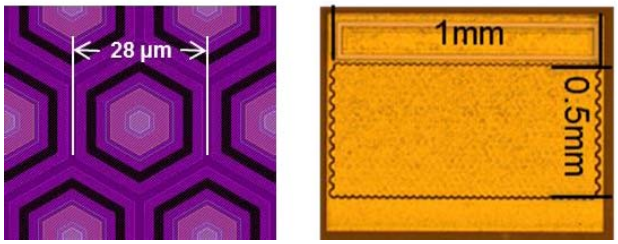

Fig. 2. Top view schematic of the hexagonal layout design; microscopic photograph of a fabricated devices.

Hexagonal cell structure was adopted to maximize the packing density. The cell pitch size is 28 μm. The device discussed in this letter has an active area of 0.5 mm^2, which includes the source/gate electrode area but excludes the bond pad area. The total gate width of the 0.5 mm^2 device is about 71 mm. Top view schematic of the layout design, and microscopic photograph of a fabricated device are shown in Fig. 2.

III. Device Characterization and Discussion

On-wafer direct-current (DC) current-voltage (IV) characterization was performed using an Agilent B1505A power device analyzer. The output and transfer current-voltage (IV)

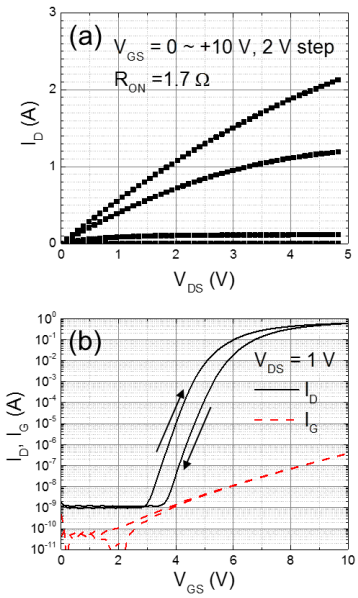

Fig. 3. Output (a) and transfer (b) IV characteristics of the fabricated GaN vertical trench MOSFET. The cell pitch size is 28 μm; and the active area is 0.5 mm^2.

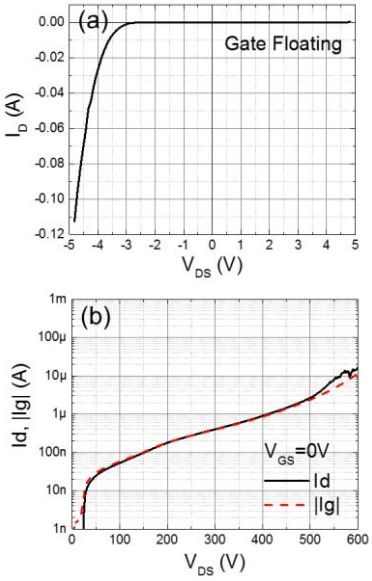

Fig. 4. Body diode IV characteristics (a) and off-state leakage characteristics (b) of the fabricated GaN vertical trench MOSFET. The cell pitch size is 28 μm; and the active area is 0.5 mm^2.

characteristics are plotted in Fig. 3 (a) and (b). From the output IV curves, one can extract an R_{ON} of 1.7 Ω at a gate bias of 10 V, for the 0.5 mm^2 area device. This translates to a specific on-resistance ($R_{ON} \times A$) of 8.5 mΩ-cm^2. Schottky diodes made with the same drift layer has a specific R_{ON} of 2∼3 mΩ-cm^2, suggesting that the large cell pitch size and/or the channel resistance are limiting factors of the total on-resistance. Improvement of total on-resistance can be achieved by: (1) reducing the cell pitch size; (2) improving the dielectric/semiconductor interface quality; (3) optimizing the drift layer growth condition for better electron mobility.

The transfer IV curves show a current ON/OFF ratio close to 10^9. The low off-sate leakage indicates effective current blocking of the p-GaN base layer. The gate leakage increased from 0.1 nA at $V_{GS} = 0$ V to 1 μA at $V_{GS} = 10$ V. We expect that the gate leakage can be further reduced by improving conformity of gate dielectric deposition. A hysteresis of 0.6 V can be observed between up and down gate bias sweeps. The hysteresis indicates trap states within the gate dielectric and/or at the interface between the gate dielectric and the p-GaN sidewall. Further process optimization for gate dielectric deposition is needed to reduce the trapping. This GaN vertical trench MOSFET has a V_{th} of 4.8±0.3V. The V_{th} is defined as the V_{GS} at which the drain current is 1000 times lower than the drain current when the V_{GS} is fully turned on. The high V_{th} is desirable for high power applications due to the noise immunity.

Fig. 4 (a) shows the drain-to-source body diode IV characteristics, with the gate electrode floating. There was no current conduction under positive drain-to-source bias, because the base/drain pn junction was reverse biased. Under negative drain-to-source bias, current conduction starts at around −3 V, which is the turn-on voltage of the base/drain pn junction. The well-behaved pn junction IV characteristics suggest success in forming body contact to the p-GaN base layer. Proper body contact is necessary for maintaining the p-GaN base layer at zero potential during transistor operation. Without the body contact, a positive drain-to-source bias can result in a positive body bias. The positive body bias shifts the threshold voltage toward negative, causing increased off-state leakage current and false turn-on. Fig. 4 (b) shows off-state drain and gate leakage characteristics. At V_{GS} of 0 V, 600 V blocking was achieved with the drain/gate leakage at around 10 μA. The off-state leakage is dominated by the gate-to-drain leakage. Suppression of the gate-to-drain leakage requires: 1. optimization gate trench etch process to achieve rounded corners; 2. further improvement of gate dielectric conformity; 3. improvement of edge termination structure.

IV. Summary

We have developed a GaN vertical trench MOSFET with two major process innovations: (1) an AlN/SiN dielectric process for the trench gate structure; (2) selective area regrowth of n$^+$-GaN source layer allowing body contact formation. The fabricated 0.5-mm^2-active-area transistor showed a threshold voltage of 4.8 V, a blocking voltage of 600 V at gate bias of 0 V, and on-resistance of 1.7 Ω at gate bias of 10 V.

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