Fabrication of Thin-Film Silicon Membranes With Phononic Crystals for Thermal Conductivity Measurements

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***Abstract*— Thermoelectricity struggles with the lack of cheap, abundant, and environmentally friendly materials. Silicon could overcome this deficiency by proposing high harvested power density, simplicity, availability, harmlessness, CMOS compatibility, and cost reduction. However, despite its high Seebeck coefficient and electrical conductivity, silicon is an inefficient thermoelectric material due to a high thermal conductivity (κ). Modern nanofabrication techniques enable reduction of κ in silicon through attenuation of thermal phonons. In this letter, the design and the fabrication of nanostructured material onto κ measurement platforms are presented. The proposed fabrication process is versatile and ensures compatibility with CMOS technologies. The proposed devices enable precise κ measurement owing to a careful management of thermal losses. Characterization resulted in a two-fold ($\kappa = 59 \pm 10$ W/m/K) reduction below bulk value for a 54-nm-thick plain silicon membranes. Further reduction is measured at $\kappa = 34.5 \pm 7.5$ W/m/K for membranes with phononic crystals.**

***Index Terms*— Thermoelectricity, silicon, phonons, thin film devices, semiconductor materials measurements, fabrication.**

I. Introduction

URGED by the worldwide increasing demand in energy [1], constrained by the limited reserves of fossil fuel [2] and faced by the problem of global climate change [3], [4], all innovative solutions contributing to improve the renewable production of energy are playing a strategic role. Among all energies produced worldwide, heat represents the highest wastes, in global scale around half of input energy being lost as a waste heat [5], [6]. In this context, harvesting of heat losses is extremely important and contributes to wiser, durable, economic usage of fossil fuels. Energy production from waste is also spurred by continually rising popularity of network-connected, mobile and energetically autonomous devices contributing in growth of the so-called *Internet-of-Things* [7].

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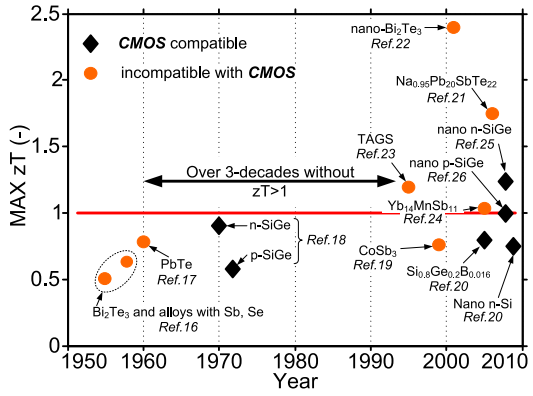

Fig. 1. Historical evolution of non-dimensional-figure-of-merit zT for chosen thermoelectric materials, based on [16]–[26].

Despite the omnipresence of waste heat, its conversion into electric energy is challenging and thus restricts thermoelectricity only to niche applications *e.g.* medical [8], spatial [9], automotive [10] or advanced industrial [11]. The main reason for such a situation is the lack of cheap thermoelectrically efficient materials. The evaluation of material's thermoelectric performance relies on maximizing the non-dimensional figure of merit ($zT = S^2\sigma T/\kappa$) [12]. Where S is the thermopower, T the temperature, σ the electrical conductivity and ($\kappa = \kappa_e + \kappa_{ph}$) the thermal conductivity. In semiconductors, thermal conductivity is a sum of two contributions: dominating lattice κ_{ph} and negligible electronic κ_e [13]. Ideal thermoelectric material should exhibit antagonistic high crystal-like σ and low glass-like κ [14]. Optimizing zT is very challenging because κ; σ and S are interdependent. As depicted in FIG. 1 it took over 30-years to develop a material exhibiting zT higher than one. FIG. 1 also reveals that a vast majority of thermoelectrics are harmful, complex, expensive, incompatible with ***CMOS*** fabrication technologies and toxic. ***CMOS*** compatible materials namely Silicon (***Si***), Germanium (***Ge***) or Silicon-Germanium (Si_xGe_{1-x}) are not marked with the aforementioned disadvantages but due to high bulk κ their usage in thermoelectricity is limited only to Si_xGe_{1-x}. Interestingly from the electrical standpoint ***Si***, ***Ge*** and Si_xGe_{1-x} are offering comparable harvesting capabilities to conventional Bismuth-Telluride Bi_2Te_3 [15].

II. Fabrication and Characterization

New fabrication techniques enabled to boost zT by suppression of κ_{ph} with minor impact on electric transport [27], [28]. This reduction is observed in low-dimensional materials

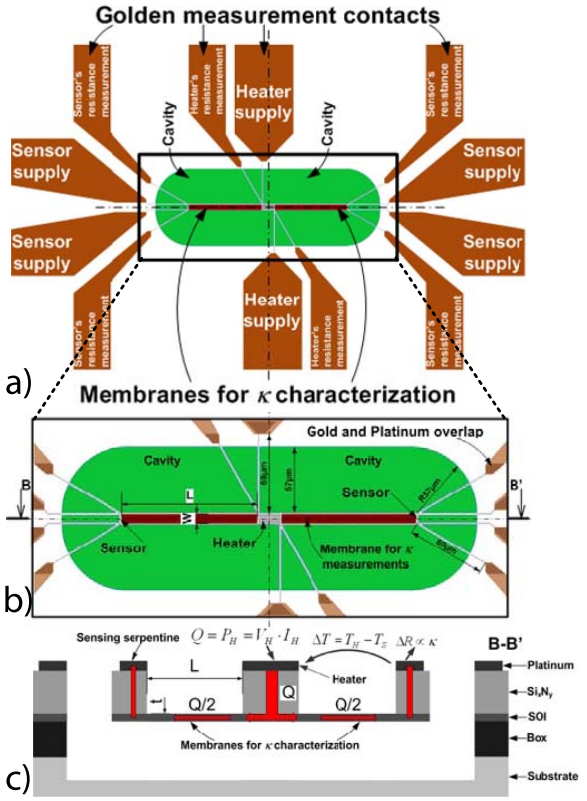

Fig. 2. Layout of measurement platform for thermal conductivity characterization in thin-film materials with phononic-crystals; a) full top-view on device; b) zooming on the membrane; c) cross-sectional view along the B-B' cutline.

e.g. quantum-dots [29], nano-wires [30], thin-films [27], [28], [31], [33]–[41], phononic crystals [27], [32], [42] or superlattices [22], [43]. This is an opportunity to improve thermoelectric efficiency for ***CMOS*** compatible materials [44] contributing to ***CMOS***-based thermoelectric generators commercialization through mass production and cost reduction.

To experimentally reveal $\boldsymbol{\kappa}$ reduction in nanostructured ***Si*** a measurement platform based on Silicon-on-Insulator (***SOI***) technology has been designed, fabricated and characterized. Thermal characterization of thin-film materials is challenging due to the high influence of heat leakages. In the literature, four main techniques able to measure $\boldsymbol{\kappa}$ in nanostructured materials are reported (FIG. 5): Raman thermometry [31], thermoreflectance [32], [33], 3-ω method [34] and electro-thermal [27], [28], [35]–[41]. This device uses the electro-thermal method owing to its simplicity and, more important, the similarity between this configuration and an actual thermopile. Measurement platforms are designed to thermally insulate the characterized membrane from the surroundings and to privilege one-dimensional heat flow ($\boldsymbol{Q}$) through the membrane. FIG. 2a) and b) depicts the top view on the device.

Design integrates two main aims: (i) the management of thermal insulation and (ii) as high as possible electrical and thermal symmetry of the device. Merging those two goals crucially improves the precision of the measurements. Thermal insulation of the membrane is achieved through the suspension of the membrane from the substrate and by applying a sensor/heater voltage via long thermally resistive arms. Moreover, the $\boldsymbol{Q}$ flow through the membrane is maximized thanks to thermal conductance matching between the membrane and the arms. The thermal conductances of the arms and membranes

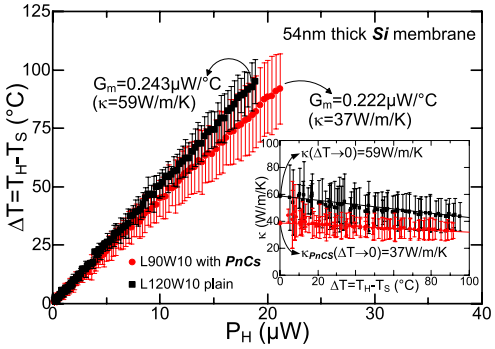

Fig. 3. Heater-sensor temperature difference versus heater's power for plain and phononic membranes. Inset plot presents $\boldsymbol{\kappa}$ versus $\boldsymbol{\Delta T}$ for same membranes. Results based on four separate measurements for each of the devices.

are almost equal making the $\boldsymbol{Q}$ as high as possible. For further improvement of measurement precision the reduction of heat convection losses is achieved by performing the measurement in vacuum allowing to assume that heat generated in the heater equals to applied Joule power ($\boldsymbol{Q = P_H}$). Thermal insulation limits the heat propagation paths privileging the heat generated in centrally situated heater to flow through the two identical suspended membranes towards sensors FIG. 2c). Heat flowing in each of the membranes ($\boldsymbol{Q}/2$) rises sensor temperature shifting its resistance. Finally, $\boldsymbol{\kappa}$ is retrieved using Eq. 1:

$$\kappa = G_m \cdot \frac{L}{W \cdot t} \tag{1}$$

where $\boldsymbol{L}$, $\boldsymbol{W}$ and $\boldsymbol{t}$ are membrane length, width and thickness respectively, $\boldsymbol{G_m}$ is membrane thermal conductance. FIG. 3 depicts the heater-sensor temperature difference ($\boldsymbol{\Delta T}$) versus $\boldsymbol{P_H}$ used to determine $\boldsymbol{G_m}$. Fabrication of membranes with $\boldsymbol{L} = \{30; 60; 90; 120\}\mu$m and $\boldsymbol{W} = \{5; 10\}\mu$m enabled statistical treatment of measured $\boldsymbol{\kappa}$.

Inset plot in FIG. 3 show that $\boldsymbol{\kappa}$ value is found at $\boldsymbol{\Delta T} \rightarrow 0$ corresponding to theoretic condition for $\boldsymbol{\kappa}$ determination.

In this topology two identical membranes are exposed to equal thermal conditions. This particularity allows performing comparative $\boldsymbol{\kappa}$ measurements upon two membranes exposed to the same fabrication and measurement conditions.

The fabrication process flow is depicted in FIG. 4. Departure point is ***SOI*** wafer with 70nm thick active layer upon which high resolution lithographically defined phononic crystals (***PnCs***) patterns are etched using chlorine-based ***R***eactive ***I***on ***E***tching (***RIE***) [45] (***STEP: 1***). Thanks to highly selective chlorine-based ***RIE*** the ***PnCs*** hole diameter is typically 20nm with a pitch of 60nm, which is so far the lowest reported dimensionality in a ***CMOS*** compatible process. In the FIG. 4 it is visible that the ***PnCs*** feature regular pitch and diameters and are defect free. Afterwards, a 12nm thick stop etch layer of thermal oxide ($\boldsymbol{SiO_2}$) is grown followed by 100nm thick low stress silicon nitride ($\boldsymbol{Si_xN_y}$) deposition (***STEP: 2***). Openings of cavities are subsequently etched down to the substrate using ***RIE*** under SF_6/Ar atmosphere (***STEP: 3***). In ***STEP: 4*** the sidewalls of the ***SOI*** are protected using $\boldsymbol{SiO_2}$. The $\boldsymbol{Si_xN_y}$ overlayer is selectively removed from the top of the membrane to avoid parasitic thermal conduction using SF_6/Ar-based ***RIE*** (***STEP: 5***). $\boldsymbol{Si_xN_y}$ is etched till $\boldsymbol{SiO_2}$ sacrificial layer grown in ***STEP: 2***. Subsequently, two metallization are performed. Firstly a 30nm thick platinum layer (***Pt***) to form heater and sensor (***STEP: 6***). Secondly, a 250nm thick gold layer (***Au***)

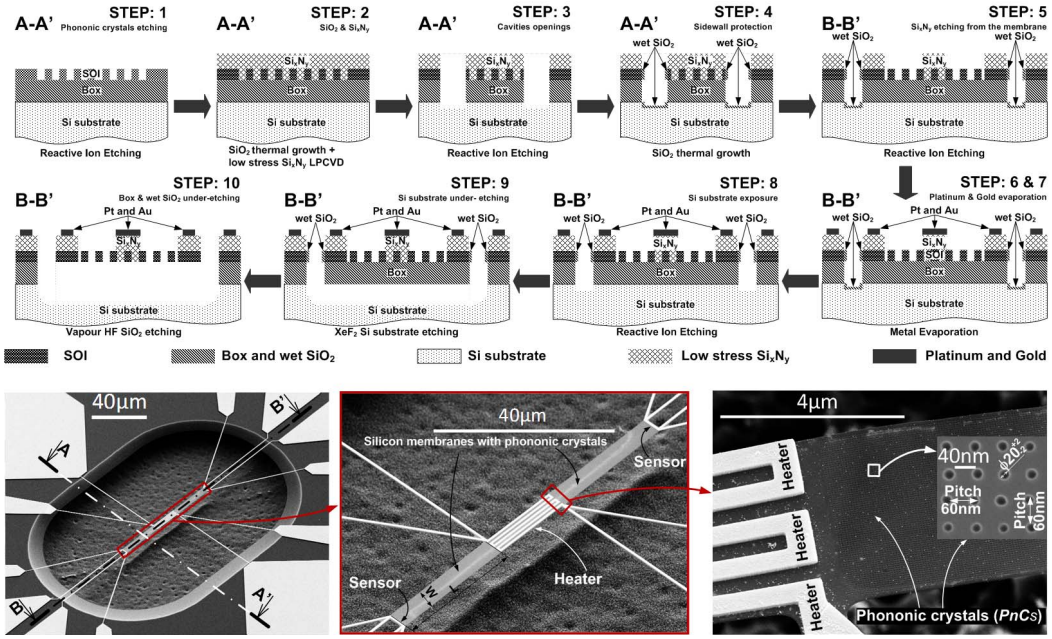

Fig. 4. Fabrication sequence of thermal conductivity measurement platform in suspended thin-film silicon membranes with integrated phononic crystals. Process flow showed after each inner step of fabrication using cross-sectional view along A-A' and B-B' cutlines presented in the photo. Pictures show the view on whole device, zoom on the membrane, finally the phononic crystals are showed highlighting their dimensionality.

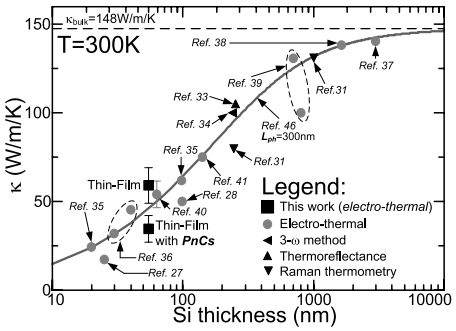

Fig. 5. Silicon thermal conductivity versus thickness. κ values related to this work includes measurements for all membranes with different L and W.

to structure measurement pads (***STEP: 7***). Consequently, to expose the substrate, SiO_2 grown in ***STEP: 4*** is selectively removed from the cavities bottoms using CH_4, N_2, O_2 based ***RIE*** (***STEP: 8***). The two final ***STEP***s consist in releasing the membrane from the substrate. The silicon handler is under-etched by XeF_2 in gaseous phase (***STEP: 9***). Finally, the buried oxide (***Box***) layer is removed by vapor phase hydrofluoric etching (***STEP: 10***). Pictures in FIG. 4 depict the final device. The membrane is insulated from the substrate relying only on the 60 μm long arms.

III. Results

We report $\kappa = 59 \pm 10$W/m/K for a plain membrane and $\kappa = 34.5 \pm 7.5$W/m/K for membrane with integrated ***PnCs***, both membranes being 54nm thick. Comparing measured κ with the theoretical model [46], using dominant mean free path for phonons $L_{ph} = 300$nm, it can be remarked that the characterized κ for thin-film ***Si*** is slightly higher than theoretical value. The reason is the imprecise estimation of heater's and sensor's temperatures due to the thin spacer layer of SiO_2 placed between Si_xN_y and ***SOI***. The heat losses in SiO_2 spacer were neglected during the analysis. The maximal temperature drop over the spacer is estimated to be $\Delta T_{SiO2} = 0.04$°C which is incomparably small comparing with ΔT along the membrane. Secondly, the accuracy of this method relies also on the precision of measurement equipment which is limited especially for at ΔT. For membranes with ***PnCs*** patterning the κ value may be higher than the expected one owing to not controlled etching depth of ***PnCs***, which may result in situation that thin-film ***SOI*** membrane is not completely etched through and κ reduction is lower. Analyzing FIG. 5 it can be remarked that the obtained measurements confirm κ reduction in thin-film ***Si***. The plain 54nm thick membrane exhibits around 2-fold reduction of κ below bulk value. Further reduction of κ is observed for membranes with ***PnCs***.

IV. Conclusions

This work has presented the design and fabrication of thin-film ***Si*** membranes with integrated phononic crystals (***PnCs***) for κ characterization Proposed device incorporates (i) high thermal insulation of the characterized membrane, (ii) high symmetry and (iii) thermal conductance matching to achieve good precision. Characterized ***Si*** membranes are integrated with ***PnCs*** patterning with ultra low diameter (20nm) and pitch (60nm) constituting the lowest reported dimensionality in ***CMOS*** compatible process. Thermal coupling between heating and sensing serpentine is used to determine κ. We report $\kappa = 59 \pm 10$W/m/K in 54nm thick ***Si*** plain membrane and $\kappa = 34.5 \pm 7.5$W/m/K in the membrane with integrated ***PnCs***. The reduction of κ in ***Si*** opens the way for cheap, environmentally friendly, industrially compatible thermoelectric devices.

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