

# A $0.27\text{e}^-_{\text{rms}}$ Read Noise $220\text{-}\mu\text{V/e}^-$ Conversion Gain Reset-Gate-Less CMOS Image Sensor With $0.11\text{-}\mu\text{m}$ CIS Process

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**Abstract**—A low temporal read noise and high conversion gain reset-gate-less CMOS image sensor (CIS) has been developed and demonstrated for the first time at photoelectron-counting-level imaging. To achieve a high pixel conversion gain without fine or special processes, the proposed pixel has two unique structures: 1) coupling capacitance between the transfer gate and floating diffusion (FD) and 2) coupling capacitance between the reset gate and FD, for removing parasitic capacitances around the FD node. As a result, a CIS with the proposed pixels is able to achieve a high pixel conversion gain of  $220\text{ }\mu\text{V/e}^-$  and a low read noise of  $0.27\text{e}^-_{\text{rms}}$  using correlated multiple-sampling-based readout circuitry.

**Index Terms**—CMOS image sensors (CISs), low read noise, high conversion gain, photon counting, photoelectron counting histogram (PCH).

## I. INTRODUCTION

LOW LIGHT-LEVEL imaging techniques with single-photon sensitivity have applications in many diverse scientific and industrial fields [1]. A single-photon avalanche diode (SPAD) [2] is one type of detector for photon-counting imaging. Using the avalanche operation, SPAD-based imagers achieve very high gain. Consequently, a single photon can be detected by the imaging devices using a SPAD array. However, they need large in-pixel circuitry for photon detection, which results in a reduction in the spatial resolution and a relatively small fill factor. In addition, the high dark count rate limits the sensor noise performance.

Recently, low-noise CMOS imagers with sub-single-electron noise level have been reported [3]–[5]. Specifically, a quanta image sensor (QIS) exhibits very impressive photon-counting capability. Using the pump-gate junction [6], a high conversion gain of  $403\text{ }\mu\text{V/e}^-$  is achieved, and consequently, a low read noise of  $0.28\text{ e}^-_{\text{rms}}$  is obtained. A photoelectron

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counting histogram (PCH) was also shown. However, a fine CIS process is essential for QIS to reduce a floating diffusion capacitance. Furthermore, because the QIS is an imager with junction devices, it has a small full well capacity (FWC) of approximately  $200\text{ e}^-$  compared with the general CMOS imagers, and no image was presented.

In this letter, a CMOS image sensor with low read noise and high pixel conversion gain, implemented through a  $0.11\text{-}\mu\text{m}$  CIS process, is introduced. Its performance is recognized through image outputs from an area image sensor, confirming its capability of photoelectron-counting-level imaging. To achieve high pixel conversion gain, the proposed pixel has two special in-pixel structures: 1) between the TG and FD node and 2) between the RG and FD node. The first method was already introduced in our previous work [7], and the second method is a new approach to eliminate the parasitic capacitance between the RG and FD node. The excellent noise level with very high, but relatively smaller conversion gain compared to [3], is attained by the FD node, which is less sensitive to noises from power lines, and the powerful 1/f noise reduction capability of readout circuitry [8].

## II. PIXEL DESIGN AND OPERATION

A high pixel conversion gain is one of the most essential performance parameters of CISs for achieving low-noise imaging. To achieve low noise, the parasitic FD node capacitance should be minimized. Fig. 1 shows the high conversion gain (HCG) pixel structure with a new approach for reducing parasitic capacitance. A cross-sectional view of the HCG pixel is shown in Fig. 1(a). Two techniques are used for achieving the high pixel conversion gain. The first method helps to reduce the parasitic capacitance between the TG and FD node [7]. As placing a fully depleted diode structure between the TG and FD nodes, the coupling capacitance, which is generated between the TG and FD nodes, can be minimized. This helps eliminate the coupling capacitance between the FD node and common power lines, which becomes noise sources.

The second method perfectly removes the parasitic capacitance between the RG and FD nodes because a reset transistor is not used, as shown in Fig. 1(a). The pixel reset operation is implemented by an implanted  $n^+$  layer located close to the FD node. This  $n^+$  implant is termed a “Reset-Generating Implant (RGI)”. As can be seen from Fig. 1(b), the FD reset

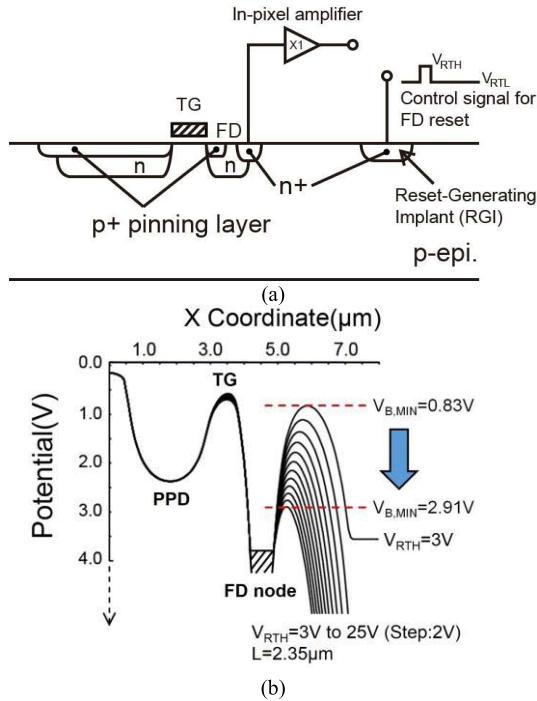


Fig. 1. Proposed HCG pixel. (a) Cross-section of the proposed pixel for reducing the parasitic capacitance of floating diffusion. (b) Potential diagram as a function of the voltage level of  $V_{RTH}$ .

level is set by a high level voltage ( $V_{RTH}$ ) of 25 V. During the readout, a low level voltage ( $V_{RTL}$ ) of 3 V is supplied to RGI. When a high voltage is applied, a barrier between the FD node and RGI is lowered by punch-through between them. The FD node is reset by this operation. These simulations are implemented by a device simulator SPECTRA. As a result, the pixel conversion gain is increased due to the minimized FD node capacitance, and the noise performance is also improved by removing two noise sources from power supplies for charge transfer and FD reset operations. To implement the FD reset, on-board clock driver is used because the high voltage over 20 V is required. The global FD resetting is applied to each line of the proposed imager to prevent the FD leakages. The pixel uniformity problem such as a pixel fixed pattern noise (FPN) may be occurred by the global reset because of the parasitic RC components, but these noise components can be removed by an analog correlated double sampling (CDS) operation.

The detected pixel signals are read out by a column-parallel analog-to-digital converter (ADC), which is capable of reducing noise effectively based on correlated multiple sampling (CMS), so-called folding-integration/cyclic ADC [8], [9]. CMS has relatively better 1/f noise reduction capability than high-gain CDS [10]. The combination of high conversion gain, less power-line noise coupling, and the CMS-based readout circuitry makes it possible to achieve the extremely low read noise level, below 0.3 e<sub>rms</sub>.

### III. MEASUREMENT RESULTS

Fig. 2 shows a temporal read noise histograms of the developed CMOS imager and a conventional low-noise

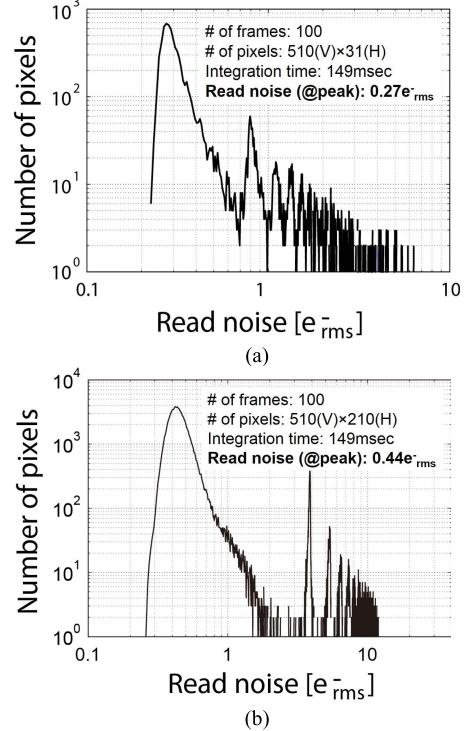


Fig. 2. Read noise histograms (@ Temp. =  $-10^{\circ}\text{C}$ ). (a) A developed HCG CMOS image sensor. (b) A conventional low-noise CMOS image sensor which uses the same column CMS readout circuitry as the HCG CMOS imager.

CMOS imager, which uses the same column CMS readout circuitry as the developed imager. In the measurement for an HCG pixel imager, a hundred frames, each comprising 15,810 pixels, are captured. A low noise level, 0.27 e<sub>rms</sub> at peak value of the distribution, is confirmed from the measured read noise histogram. Fig. 2(b) shows the read noise distribution of the conventional low-noise CMOS imager. The read noise level of the conventional imager is approximately 0.44 e<sub>rms</sub>, and the pixel conversion gain is 135  $\mu$ V/e<sup>-</sup>. In case of the HCG pixel imager, the conversion gain of 220  $\mu$ V/e<sup>-</sup> is used for converting the signal from voltage to electron, and this conversion gain is obtained from the photoelectron-counting histogram (PCH) result, as shown in Fig. 3.

To attain PCHs, a particular pixel is saved several times (100,000 points) with the 19-bit column ADC. Fig. 3(a) and Fig. 3(b) are the measured results when  $\lambda$  is 2.05 and 4.0, respectively, where  $\lambda$  means an average signal level. These results are almost the same as the theoretical Poisson distributions with a Gaussian noise distribution, which are expressed as

$$h(y) = \sum_{x=0}^{\infty} \frac{\lambda^x}{x!} \cdot e^{-\lambda} \cdot \frac{1}{\sqrt{2\pi\sigma}} e^{-\frac{(y-x)^2}{2\sigma^2}} \quad (1)$$

where,  $\sigma$  is a read noise level. The valley-to-peak modulations of PCHs indicate the CMOS imager's read noise levels [11], which are 0.26 e<sub>rms</sub> and 0.27 e<sub>rms</sub>, respectively.

Fig. 4 shows the captured images with the United States Air Force (USAF) test chart for demonstrating the photoelectron-counting capability of the newly developed CMOS imager.

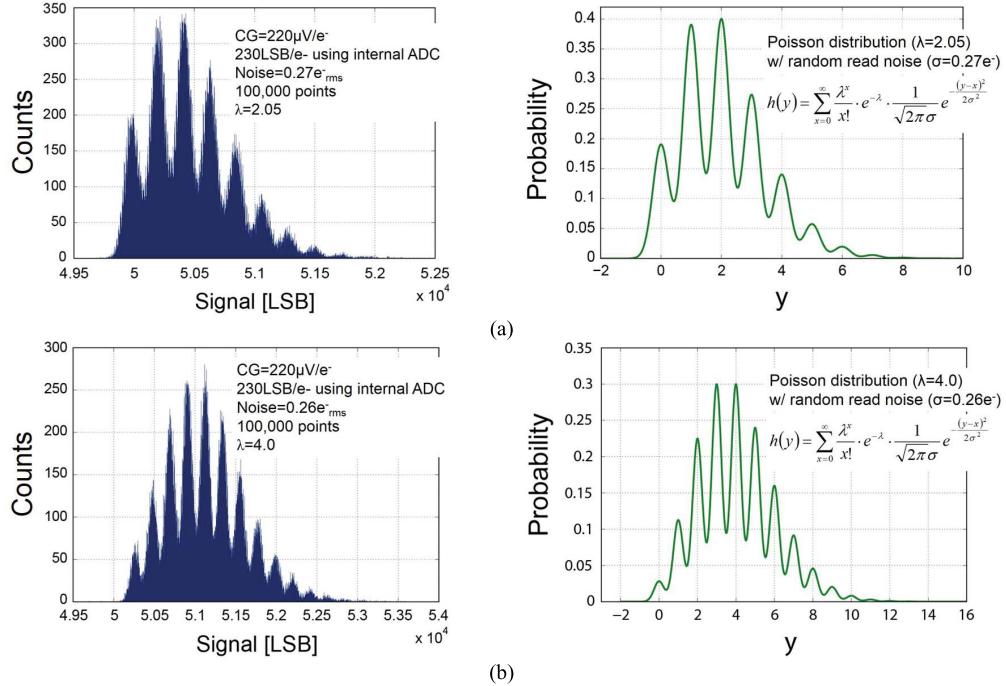


Fig. 3. Photoelectron-counting histograms with a theoretical Poisson distribution of the developed CMOS imager (@ 100,000 points, 230 LSB/e<sup>-</sup> using internal ADC). (a)  $\lambda = 2.05$ . (b)  $\lambda = 4.0$ .

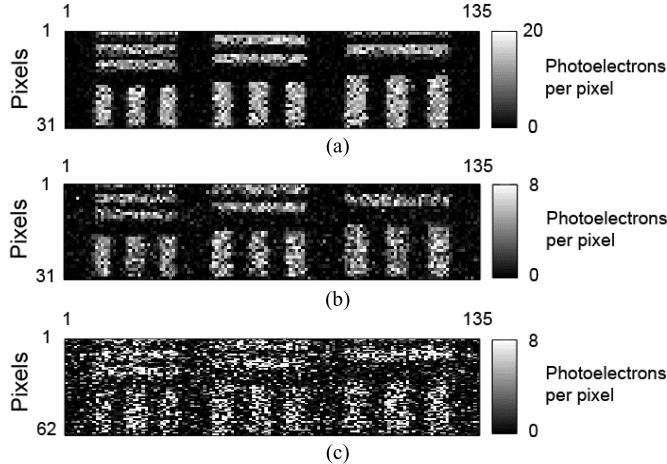


Fig. 4. Captured images with the USAF test chart for demonstrating a photon-counting-level imaging capability (@ single frame, analog gain = 128). (a) Signal range from 0 to 20 electrons (captured by proposed imager). (b) 0 to 8 electrons. (c) 0 to 8 electrons (captured by conventional low-noise imager).

This is the first proof of the photoelectron-counting-level images using the low-noise CMOS image sensor without avalanche gain. Photon-counting-level imaging means that the photon shot noise only is observed in the image and particularly the very dark region of the image becomes very black because of the lack of incident photons. The images are formed from single frames, each 142 msec of exposure, and the signal (photoelectron) per pixel is calculated from PCH of each pixel. The captured images from Fig. 4(a) to (c) have a different signal ranges adjusted by a neutral density (ND) filter with a fixed light intensity (Fig. 4(b) and (c) are captured under the same conditions). The sensor chip is air cooled to  $-10^{\circ}\text{C}$  in order to minimize the influence of dark current, and we

TABLE I  
SENSOR PERFORMANCE

Parameter	Value
Technology	$0.11\ \mu\text{m}$ 1P4M CIS process
# of pixels	Total number: $312(\text{H}) \times 512(\text{V})$ Effective number: $35(\text{H}) \times 512(\text{V})$
Pixel size	$11.2\ \mu\text{m}(\text{H}) \times 5.6\ \mu\text{m}(\text{V})$
ADC resolution	19 bits
Full well capacity (FWC)	1,500 electrons
Pixel conversion gain	220 $\mu\text{V/e}^{-}$
Read noise (@peak)	$0.27\ \text{e}_{\text{rms}}$

work with a region of interest of  $35(\text{H}) \times 512(\text{V})$  pixels. Fig. 4(c) is captured by a conventional low-noise CMOS imager (see Fig. 2(b)). As shown in Fig. 4, the image contrast of the pixels with  $0.27\ \text{e}_{\text{rms}}$  (Fig. 4(b)) is much better than that of conventional pixels, which is with  $0.44\ \text{e}_{\text{rms}}$  (Fig. 4(c)).

Table I shows a brief summary of the prototype CMOS imager performance.

#### IV. CONCLUSION

In this letter, an extremely-low-noise CMOS image sensor with reset-gate-less high conversion-gain pixels using a standard  $0.11\ \mu\text{m}$  process is presented. For the first time, high contrast images from the CMOS image sensor, with less than  $0.3\ \text{e}_{\text{rms}}$  noise level, have been generated at an extremely low light level of less than eight electrons per pixel. This suggests that photoelectron-counting-level imaging is possible. The extremely low noise level with very high, but relatively small conversion gain, and large full well capacity, when compared with the quanta image sensor [3], are suitable for many scientific cameras and applications that require

both photon-counting- level sensitivity and sufficient dynamic range.

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