A Dual-Pass High Current Density Resonant Tunneling Diode for Terahertz Wave Applications

K. J. P. Jacobs, B. J. Stevens, O. Wada, T. Mukai, D. Ohnishi, and R. A. Hogg

***Abstract*— We report on a dual-pass high current density resonant tunneling diode (RTD) for terahertz wave applications. This technique reduces the overall fabrication complexity and improves the reproducibility for creating low resistance ohmic contacts. With our dual-pass technique, we demonstrate accurate control over the final device area by measuring the RTD current–voltage characteristic during the fabrication process and guiding the emitter current through the full RTD structure with a second contact electrode on the collector side. We go on to show how we may extract important information about the RTD performance using this method.**

***Index Terms*— Resonant tunnelling diode, terahertz, manufacturability.**

I. Introduction

THERE is currently a high demand for ultra-fast wireless communications due to the explosive growth in mobile data [1]. To satisfy future data usage needs, higher operating frequencies are required to make better use of the available spectral resources. The spectral region between 0.1-10 terahertz (THz) in the electromagnetic spectrum, also known as the "terahertz gap", offers ultra-fast wireless communications [2]. The lower frequency band of 275 GHz $\sim$ 3000 GHz has not been allocated yet for specific uses, and offers high wireless data rates which match the current bandwidths of fibre optic communications [3]. In 2011, Mukai *et al.* demonstrated wireless data transmission at 1.5 Gbit/s in the 300 GHz band using a resonant tunnelling diode (RTD) coupled to an antenna [4].

The RTD is recognised as the fastest electronic device with a fundamental oscillation of 1.55 THz reported [5]. Small device dimensions are required to minimise the parasitic capacitance of the device for high speed operation, which results in very high current densities being required.

A high operating current density places significant emphasis on the final device area and the manufacturability of low resistance ohmic contacts, meaning that process variability is critical to the final device characteristics.

In this letter, we propose and demonstrate a dual-pass high current density RTD for THz wave applications. This fabrication technique allows accurate control over the final device area (and hence characteristics), and the formation of reproducible low resistance ohmic contacts to both the collector and emitter. This has been made possible by guiding the emitter current through the full RTD structure with a large second contact electrode on the collector side. Full control over the RTD mesa area is achieved by evaporating the emitter and collector electrodes *before* the RTD mesa area is defined. Fabricating both contact electrodes in a single metal evaporation process at the start of the fabrication process not only ensures that the emitter and collector semiconductor-metal interfaces are identical and of low resistance, but also simplifies the fabrication process, and improves reproducibility as damage to the surface from future processing is minimised. We developed an all-wet etch process as dry etching plasma damage to the surface may severely degrade the device characteristics. Whereas a combination of dry and wet etching can reduce surface damage, this comes at the expense of uniformity and reproducibility due to the increased complexity of the fabrication process. Our technique builds up on work recently reported by Jin *et al.* on the fabrication of a Si/SiGe resonant interband tunnelling diode (RITD) using a 1-metal fabrication process and self-aligned Ni silicidation process [6] and by Romanczyk *et al.* on the realisation of submicron III-V Esaki diodes using a subtractive mesa etch [7]. Large parasitic tunnel diodes were used as a virtual ground. We apply a similar technique to the RTD and are able to accurately control the mesa area of the RTD, whilst minimising fabrication complexity, and extracting important information about the RTD characteristics, such as RTD peak voltage and contact resistance, through in-line I-V characterisation. Extracting these characteristics in-line with the fabrication process without the need of additional complex test structures is advantageous from a manufacturing point of view, and provides a route for further device optimisation.

II. Device Structure & Fabrication

Fig. 1(a) shows a schematic of the RTD structure and (b) the fabrication process flow of the RTD. Details of the growth process are discussed elsewhere [8]. Initially, a Ti/Au (20 nm/1000 nm) metallisation layer is deposited using a standard thermal evaporation and lift-off process to define

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K. J. P. Jacobs, B. J. Stevens, O. Wada, and R. A. Hogg are with the Department of Electronic and Electrical Engineering, The University of Sheffield, Sheffield S3 7HQ, U.K. (e-mail: elp11kjj@gmail.com).

T. Mukai and D. Ohnishi are with the Optical Device Research and Development Division, Sensor Business Strategy, Rohm Company, Ltd., Ukyō-ku 615-8585, Japan.

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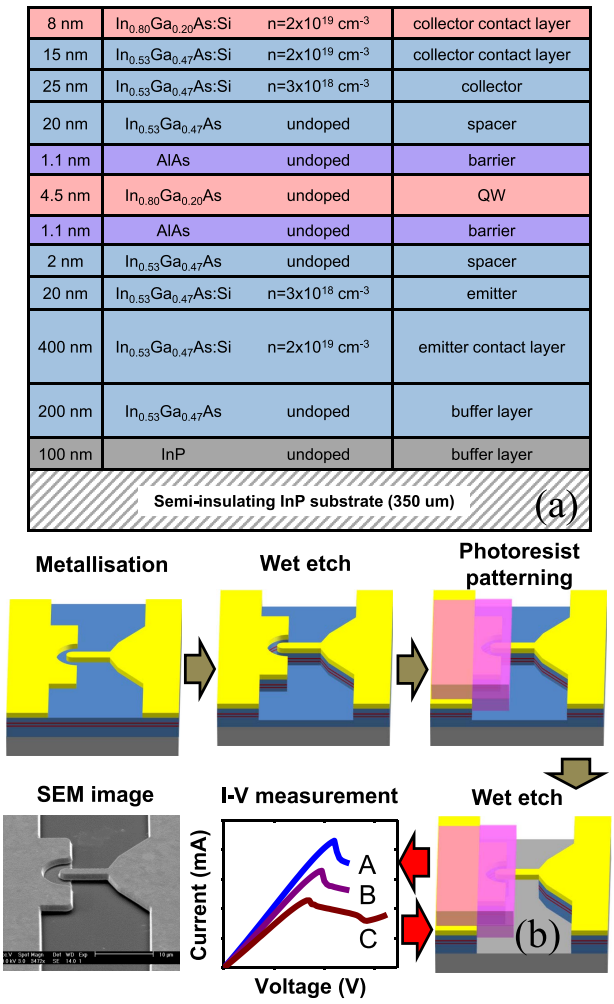

Fig. 1. (a) Schematic of the RTD layer structure. (b) Process flow of the dual-pass high current density RTD.

both contact electrodes. With this contacting arrangement, both contact interfaces benefit from the narrow band-gap $In_{0.8}Ga_{0.2}As$ surface layer, as a nearly zero Schottky barrier height can be produced for InGaAs with an indium mole fraction greater than 0.8 for a non-alloyed contact [9].

The contact metallisation stage is followed by a controlled shallow wet etch (H_3PO_4:H_2O_2:H_2O = 1:1:38) of 150 nm down to the highly doped emitter layer located below the double-barrier heterostructure. A Au air-bridge contact is subsequently fabricated by photoresist patterning the RTD and wet etching to produce a "tunnel" below the exposed Au stripe as shown schematically in Fig. 1(b) [10], [11]. The RTD devices are fabricated with the air-bridge aligned along the [001] direction to enhance the lateral etch rate underneath the air-bridge in the [010] direction whilst creating nearly vertical etch profiles along [001]. V-shaped and dovetail etch profiles are obtained for the mask patterns aligned in the [01-1] and [011] directions, respectively. The InP layer underneath the highly doped emitter contact layers acts as an etch-stop layer which also enhances the lateral etching underneath the air-bridge due to the selectivity of the selected wet etch. Test-structures of standalone metal bridges of various widths are fabricated along the direction of the air-bridge on the wafer to monitor the formation of the air-bridge during the

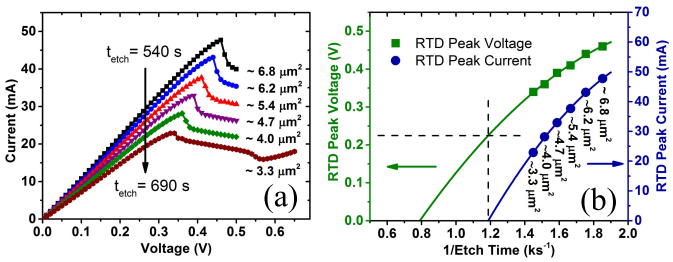

Fig. 2. (a) I-V characteristics of the RTD measured in-line with the fabrication process. The device area shown in μm^2 represents the total RTD area and is calculated from the peak current density measured from a second sample. (b) RTD peak voltage and peak current as a function of etch time. The black dotted lines guide the eye to the intercept point on the curve of the extrapolated quadratic fit to the RTD peak voltage for a zero peak current.

etch process. These test structures with increasing width are sequentially etched off due to undercutting.

III. Results and Discussion

Eliminating the second contact metallisation to the emitter layer by guiding the emitter current through the full RTD structure also allows the I-V characteristic of the RTD to be measured during the fabrication to accurately control the final RTD area. Fig. 2(a) shows a graph of such RTD I-V characteristics for etch durations of 540 seconds to 690 seconds with 30 second steps from a single device. The I-V measurements are carried out in third quadrant operation (negative bias applied to the collector), as the peak current density and peak voltage are lower in this mode of operation (thicker undoped spacer layer on the emitter side). Operating in this safe operation mode reduces the risk for catastrophic failure due to self-heating during the etch process. From the measured I-V characteristic shown in Fig. 2(a), a peak-to-valley current ratio (PVCR) of 1.5 is obtained, which is in good agreement with the literature for similar high current density RTDs [12], [13]. A value of 0.7 MA/cm^2 is also a similar performance to previously reported values for similar devices [14]. A peak current density of 1.7 MA/cm^2 and a PVCR of 2.5 were measured in the forward bias condition.

The observed reduction in peak current with increasing etch time is associated with a reduction in mesa size, as the total tunnelling current is proportional to the mesa area. The corresponding mesa area for each I-V characteristic is deduced from the current density through the RTD as indicated in Fig. 2(a). The current density was measured from a different fabrication based on e-beam lithography (EBL), which allowed for an estimation of the mesa area through I-V characterisation. This test-structure was fabricated without an air-bridge structure by applying a two-stage metal deposition with a separate contact electrode on the highly doped emitter contact layer. The active area tunnelling area was defined using a shallow wet etch of ~150 nm to the emitter. We note that the current density (and hence area) is an estimated value as we neglect the undercut of the mesa electrode. Measurement of our dual-pass device under repeated wet etch processes showed constant PVCR with increasing etch time, indicating that surface leakage currents are minimal lending further confidence to this estimation of area.

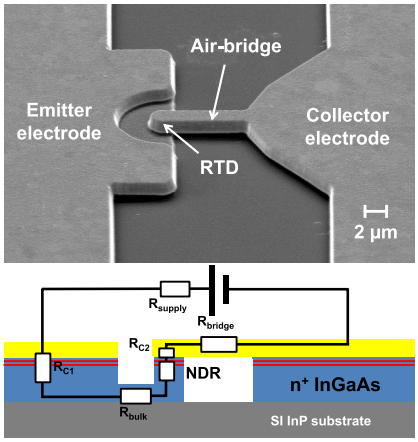

Fig. 3. Annotated SEM image of a 3.3 μm^2 RTD with a schematic profile showing contact resistances (R_{C1}, R_{C2}), bulk resistance (R_{bulk}), negative differential resistance (NDR), bridge resistance (R_{bridge}), and supply resistance (R_{supply}).

Based on an etch time resolution of 1 second, an areal etch accuracy of less than 1 % is achieved for a single device with a final area of 3.3 μm^2. It is also noted that the peak current is not linear with time which illustrates the encroachment of the undercut process.

The avoidance of plasma processes, and associated sidewall damage, is also seen as a benefit. Whereas dry etch damage might be less significant for devices with a large diameter, the damage (up to 100 nm deep [15]) can have a large impact on the performance of micron and sub-micron scale devices, as the size of the device approaches the dimension to the damaged region.

Fig. 2(b) shows the RTD peak voltage and peak current as a function of etch time. The reducing RTD peak voltage with increasing etch time is associated with the voltage drop across parasitic resistance in the circuit. Extrapolating the peak voltage as a function of mesa area provides information on the RTD characteristics. A peak voltage of ~225 mV is determined in the limit of zero peak current by extrapolating the quadratic fit to the peak voltage as a function of etch time. This minimum peak voltage consists of the voltage drops across the collector contact (R_{C2}), and between the emitter and collector layers of the RTD at resonance. Fig. 3 shows an annotated SEM image of the RTD and a circuit diagram of the resistive elements of the device and the measurement circuit. The voltage drops across the emitter contact (R_{C1}+R_{bulk}), the supply resistance (R_{supply}), and air-bridge (R_{bridge}) are excluded in the limit zero current, as these resistive elements do not change in size during the etch process. For a total series resistance of 5 ohms, 2 ohms is assigned to R_{C1}+R_{bulk}+R_{bridge} and 3 ohms to R_{supply}.

The bias voltage between the emitter and collector layers of the RTD at resonance are extracted by a subtraction of the collector contact voltage drop from the extrapolated minimum peak voltage of the RTD. The voltage drop across the collector contact is deduced from linear transfer length method (LTLM) measurements performed on devices fabricated alongside the RTDs. Using LTLM, a specific contact resistivity of 8 $\Omega.\mu$m^2 is measured for the collector contact, allowing a peak forward voltage of 168 mV to be deduced between the emitter and collector layers of the RTD. Our fabrication method therefore not only allows accurate control over the final device area (and hence characteristics) by measuring the RTD I-V characteristic during the fabrication process, but also allows the contact resistance of the RTD to be measured without LTLM structures, if the peak voltage between the emitter to the collector layers of the RTD is known, or vice versa.

By using a large emitter contact, a low resistive path of 2 Ω is created between the collector and emitter. For a measured sheet resistivity of 5 Ω/square using LTLM, 1 Ω is estimated for R_{bulk} of the n^+ InGaAs layer and 1 Ω for the large parasitic tunnel diode. R_{bulk} can be further reduced by minimising the distance between the RTD and the emitter electrode, whilst R_{C1} and R_{C2} can be further reduced by optimising the ohmic contacts (e.g. Mo based metal contact [16]). We note that our contacting arrangement is not only attractive from being simple and reproducible, but future devices will benefit from this arrangement as the emitter contact resistance will continue to reduce by increasing the current density to access the higher oscillation frequencies. Using our fabrication technique, we recently demonstrated fundamental emission at 0.35 THz with the RTD monolithically integrated to a slot antenna on the InP substrate [17], To further reduce the mesa area to <1 μm^2 for >1 THz operation, we propose the introduction of an InP etch stop layer in the highly doped emitter layer to perform additional lateral etching to reduce the RTD mesa area to sub-μm^2 dimensions.

IV. Conclusions

In this letter, we proposed and demonstrated the fabrication and characterisation of a dual-pass high current density RTD for THz wave applications using a novel emitter contact. Accurate control over the final mesa area (and hence device performance) was achieved by in-line I-V characterisation and guiding the emitter current through the full RTD structure with a second contact electrode on the collector side. Our contacting arrangement reduces fabrication complexity and improves the reproducibility of creating low resistance ohmic contacts for these high speed devices. We extracted the RTD peak voltage from the measured I-V characteristics of the RTD, and demonstrated a low resistance emitter contact using a dual-pass technique.

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