Implementation of High-Power-Density *X*-Band AlGaN/GaN High Electron Mobility Transistors in a Millimeter-Wave Monolithic Microwave Integrated Circuit Process

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***Abstract*— A GaN high electron mobility transistor monolithic microwave integrated circuit (MMIC) designer typically has to choose a device design either for high-gain millimeter-wave operation with a short gate length, or for high-power-density *X*-band operation with a much larger gate/field-plate structure. We provide the designer the option of incorporating two different devices by implementing a 0.14-μm gate length GaN MMIC process capable of high-efficiency Ka-band operation while simultaneously achieving high power density in the same process flow. The key process enabler simply uses the capacitor top plate in the MMIC process as a field plate on the passivation layer. On two separate devices on the same chip using the same MMIC process flow, we demonstrate 7.7 W/mm at 35 GHz and V_{DS} = 30 V on a standard 4 × 65-μm T-gated FET and then 12.5 W/mm at 10 GHz and V_{DS} = 60 V on a 4 × 75-μm T-gated FET by adding a field plate. These are the highest reported power densities achieved simultaneously at *X*-band and Ka-band in a single wideband GaN MMIC process.**

***Index Terms*— GaN, AlGaN, SiC, high electron mobility transistor, X-band, Ka-band, field-plate.**

I. Introduction

GaN monolithic microwave integrated circuit (MMIC) technology performance continues to advance for dual-use applications including narrow-band, high-power amplifiers for transmitters, broadband amplifiers for receivers, as well as higher frequency applications such as communication [1]–[5]. Device level improvements from major government investments have resulted in impressive performance gains over the years. In 2005, Palacios *et al.* demonstrated 10.5 W/mm with 34% power added efficiency (PAE) at 40 GHz [6]. In 2006, Wu *et al.* demonstrated 40 W/mm with 60% PAE at 4 GHz, using double field-plated (FP) technology [7]. Rosker *et al.* reported results in 2009 for X-band and Q-band which achieved 6.5 W/mm with 62% PAE and 3.6 W/mm with 36% PAE, respectively [8]. Presently, performers have reported self-assessed manufacturing readiness level (MRL) 9 for 0.25 μm GaN MMIC processes [9], [10].

In parallel with these efforts, the Air Force Research Laboratory (AFRL) demonstrated a 0.14 μm GaN high-electron mobility transistor (HEMT) process optimized for high gain and efficiency using a simple gate-first process with silicon nitride passivation layer on 0.14-μm gate length HEMTs [11]. This process was further used to define the tradespace for short-channel effect and breakdown limitations in T-gated AlGaN/GaN HEMTs as a function of aspect ratio for gate length values ranging from 90 nm – 500 nm [12]. The AFRL GaN MMIC process developed from the previous device level efforts supports high efficiency and broadband operation from 0 – 40 GHz [13], [14]. Many known manufacturing processes to date use some form of dielectric etch to define gate openings [15], [16]. The process reported here uses a gate-first process to avoid dry-etch damage under the gate which can alter threshold voltage and impact frequency dispersion [17].

In this letter, we demonstrate simultaneous high power operation at 10 GHz and high power and efficiency operation at 35 GHz in one MMIC process flow on separate devices using a single 0.14 μm T-gate process. High-power device operation is achieved at 10 GHz by adding a source-connected field plate (FP), through layout changes, over the T-gate on top of the device passivation layer formed from the top metal layer of the capacitor. As shown in Fig. 1, the FP used in conjunction with the common T-gate allows both high-power and high-efficiency operation at X-band without trading off high efficiency or power at Ka-band. Since the FP is deposited on thick silicon nitride device passivation, parasitic capacitance is reduced. The resulting power performance is the highest reported simultaneously at X-band and Ka-band on the same wafer in a single wideband GaN MMIC process.

II. Device Structure and Fabrication

The wafers and epitaxy were purchased from IQE and grown by metal organic chemical vapor deposition (MOCVD) on 4″ 6H-SiC substrates with the following structure: AlN nucleation/ 1.8 μm Fe-doped GaN buffer/

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TABLE I
DC/RF WAFER LEVEL PARAMETERS FOR 4 × 75 μm fp AND NON-FP DEVICE

Device		V_{th} (V)	$G_{m,peak}$ (mS/mm)	I_{dss} (mA/mm)	I_{max} (mA/mm)	V_{knee} (V)	I_{gl} (mA/mm)	V_{BK-3T} (V)	Gate Lag (%)	Drain Lag (%)	f_T (GHz)	f_{max} (GHz)
No FP	Mean	-3.2	421	1117	1294	1.8	-0.03	34	4	10	65	100
	Std. Dev.	±0.05	±21	±50	±58	±0.06	±0.029	±3	N/A	N/A	±0.8	±0.99
FP	Mean	-3.2	383	997	1158	2.1	-0.03	> 50	4	10	63	80
	Std. Dev.	±0.05	±20	±50	±60	±0.05	±0.027	N/A	N/A	N/A	±0.7	±1.2

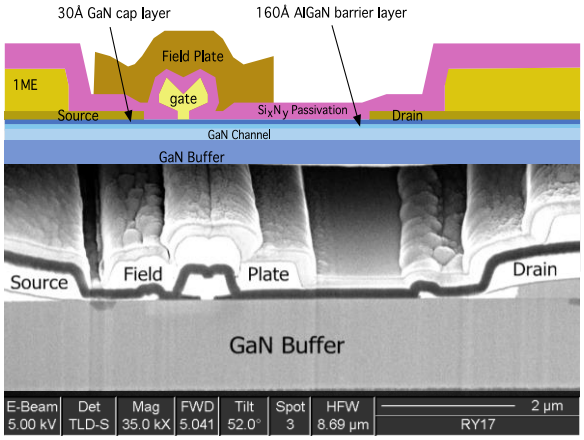

Fig. 1. Illustration and SEM cross-section of the device topology for source-connected FP HEMTs from AFRL 0.14 μm GaN MMIC process.

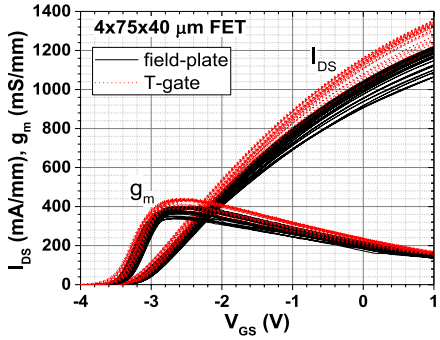

Fig. 2. Wafer scale data showing I_{DS} and g_m for all 4×75 μm FETs passing breakdown screen.

GaN channel/ 1 nm AlN/ 16 nm $Al_{0.28}Ga_{0.72}N$/ 3 nm GaN cap (Part Number F46080P1ECR2223C). Pre-process screening of the wafers was performed using a Lehighton 1610 contactless Hall mapping system. The sheet resistance (R_{sh}) of the wafers was 328 ± 4 Ω/sq.

Device fabrication began with mesa isolation of the active field-effect transistor (FET) areas using a Plasma-Therm 770 and $BCl_3/Cl_2/Ar$ with inductively coupled plasma and reactive ion etching. Excellent isolation characteristics of the GaN buffer were measured using process control monitor (PCM) structures with less than ~75 nA/mm leakage with 60 V bias between ~5-μm separated mesas. Ohmic contact metal (Ti 200 nm/Al 100 nm/Ni 50 nm/Au 50 nm) was evaporated and alloyed in a Steag SHS100 rapid thermal anneal tool in nitrogen at 850 °C for 30 sec. Schottky T-gates (Ni 20 nm/Au 380 nm) were formed using a PMMA/MMA tri-layer stack and patterned in a JEOL 6300 electron beam lithography system. After T-gate formation, interconnect metal pads and transmission lines were defined with evaporated metallization (Ti 20 nm/Au 480 nm). The devices were passivated with 200-nm silicon nitride deposited by plasma enhanced chemical vapor deposition. As previously reported [18], the silicon-rich nitride, with refractive index of 2.2, serves as an excellent, low RF dispersion passivation layer on the AlGaN/GaN epitaxy. A second interconnect metal (Ti 20 nm/Au 480 nm) was then evaporated and serves as both the capacitor top plate and FET FP. Finally, ~6-μm thick source-connected posts with Au air bridges were electroplated. An FEI Dual Beam 235 was used to generate a SEM cross-section of a representative FP GaN HEMT as shown in Fig. 1. All device topologies presented in this letter are either (1) T-gated FETs with source-drain spacing of 3.0 μm and gate-drain spacing of 2.0 μm or (2) FP T-gate FETs with source drain spacing of 4.5 μm and gate-drain spacing of 3.5 μm with nominal FP extension of 1.5 μm from gate center toward the drain. Device peripheries were (1) 4×65 μm and (2) 4×75 μm with 40 μm gate pitch.

III. TEST RESULTS

In-line PCM testing was performed with a Keithley 450 automated parametric test system on-wafer to measure sheet resistance (R_{sh} = 300 ± 4.3 Ω/sq) and contact resistance (R_C = 0.31 ± 0.04 Ω·mm) from over 50 sites. DC/RF measurements were performed on-wafer using an automated Cascade probe station with HP4142 parameter analyzer, bias tees and HP8510 network analyzer. Standard DC measurements included transconductance (g_m), *I-V* family of curves, gate leakage (I_{gl}) and three-terminal breakdown (V_{BK-3T}). S-parameters were swept from 1-26 GHz to obtain extrinsic (pad parasitics included) cutoff and maximum available gain frequencies (f_T and f_{MAX}, respectively) at peak g_m. Unless otherwise specified, all DC/RF measurements were made at V_{DS} = 10 V. Wafer-scale DC/RF metrics and deviation for each device type across a 4-inch wafer are displayed in Table 1. Devices were screened for V_{BK-3T} by forcing a drain current (I_D) with V_{GS} set to 2 volts below threshold (V_{th}) and recording the resulting V_{DS} at I_D = 1 mA/mm. Gate-terminal current (I_G) was recorded in the same measurement and I_{gl} is recorded for V_{DS} = 10 V. FP devices with V_{BK-3T} < 50 V and standard T-gated devices with V_{BK-3T} < 25 V were excluded from the results. Post-screened transfer characteristics are compiled in Fig. 2

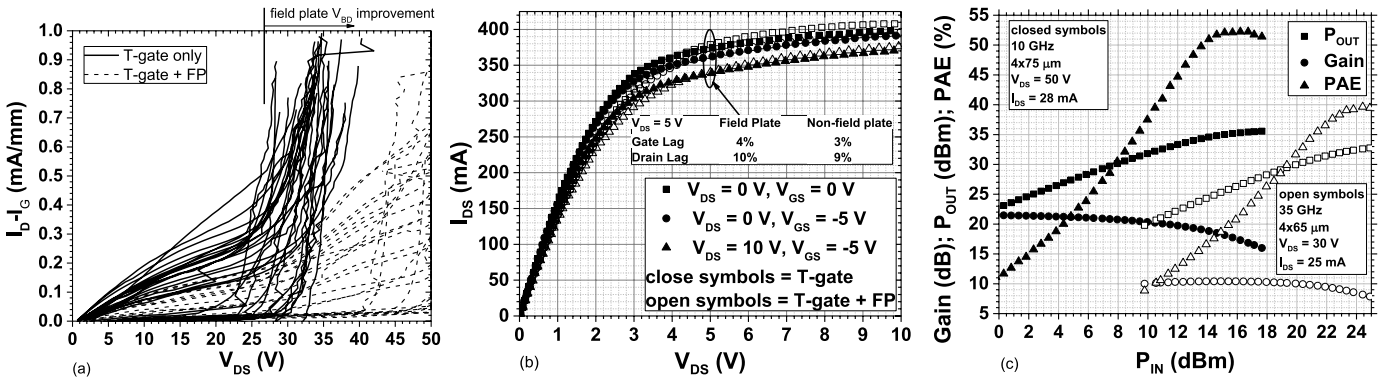

Fig. 3. (a) Aggregate wafer-scale buffer breakdown characteristics. Data shown is $I_D - I_G$ as a function of V_{DS} from V_{BK-3T} extraction on 4×75 μm T-gated FETs with and without FP. (b) Gate and drain-lag measurements for 4×75 μm T-gated FETs with and without FP. Dispersion characteristics are the same for both topologies. (c) Sample X- and Ka-band power performance of T-gated 4×75 μm FP FETs and T-gated 4×65 μm non-FP FETs.

and illustrate the effect of the FP. While f_T remains nearly unchanged, the f_{MAX} is lower as a result of higher gate-source capacitance from the FP.

Fig. 3(a) shows an aggregate plot of breakdown characteristics through the buffer for all FETs that passed screening where gate-terminal current is subtracted from drain-terminal current (I_D - I_G). V_{BK-3T} improved dramatically with the addition of the FP from 34 ± 3 V to greater than 50 V limited by instrument compliance. Dispersion (dc-pulsed I-V current collapse) was characterized on select devices using a D265 Accent DiVA system. Quasi-static, gate lag, and drain lag data were collected for $V_{DS} = 10$ V, $V_{GS} = 1$ V when pulsed from the following respective bias points: $V_{DS}/V_{GS} = 0$ V/0 V; $V_{DS}/V_{GS} = 0$ V/($V_{th} - 2$ V); $V_{DS}/V_{GS} = 10$ V/($V_{th} - 2$ V). Pulse length was 200 ns with 1 ms between pulses. Gate and drain lag were 4% and 10%, respectively, at $V_{DS} = 5$ V. Fig. 3(b) shows representative dispersion characteristics for T-gate devices which reveal negligible difference between both designs. Power load pull measurements at 10 GHz were performed using 1.8 – 18 GHz Maury Microwave Automated Tuners and an Aethercomm 8 – 12 GHz, 10 W solid state power amplifier, and 35 GHz testing using Maury 8.0 – 50 GHz tuners and IFI T3832-40, 32 – 38 GHz, 40 W traveling wave tube wide-band amplifier. In all cases, devices were biased in Class AB with $I_{DQ} = 0.1 \cdot I_{DSS}$ and matched for maximum power. At 10 GHz CW, 4 × 75 μm FP devices achieved 10.8 ± 0.8 W/mm and $PAE = 44 \pm 4\%$ at $V_{DS} = 50$ V for 8 different devices over 4 different wafers with maximum output power observed of 12.5 W/mm for $V_{DS} = 60$ V. At 35 GHz CW, 4 × 65 μm T-gated devices achieved 7.0 ± 0.5 W/mm and $PAE = 39 \pm 1\%$ at $V_{DS} = 30$ V on 5 different devices on 2 different wafers with maximum output power observed of 7.7 W/mm. 35 GHz power measurements were limited by 25 dBm input drive. Representative load-pull curves are shown for devices at 10 GHz and 35 GHz in Fig. 3(c). *PAE* values exceeding 50% were observed at 10 GHz.

IV. Conclusion

We have demonstrated high gain and power density at Ka-band while simultaneously achieving high-power density at X-band on separate devices on the same chip through layout changes to high frequency T-gated devices. The resulting field plates allow high voltage operation at lower frequencies enabling flexible MMIC design with efficient broadband operation and high power density from 0 – 40 GHz.

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References

[1] M. S. Shur, R. Gaska, A. Khan, and G. Simin, "Wide band gap electronic devices," in *Proc. 4th IEEE ICCDCS*, Oranjestad, Aruba, Apr. 2002, pp. D051-1–D051-8. DOI: 10.1109/COMMAD.2002.1237177

[2] R. S. Pengelly, S. M. Wood, J. W. Milligan, S. T. Sheppard, and W. L. Pribble, "A review of GaN on SiC high electron-mobility power transistors and MMICs," *IEEE Trans. Microw. Theory Techn.*, vol. 60, no. 6, pp. 1764–1783, Jun. 2012. DOI: 10.1109/TMTT.2012.2187535

[3] J. S. Moon, D. Wong, M. Antcliffe, P. Hashimoto, M. Hu, P. Willadsen, M. Micovic, H. P. Moyer, A. Kurdoghlian, P. Macdonald, M. Wetzel, and R. Bowen, "High PAE 1 mm AlGaN/GaN HEMTs for 20 W and 43% PAE X-band MMIC amplifiers," in *Proc. IEDM*, San Francisco, CA, USA, Dec. 2006, pp. 1–2. DOI: 10.1109/IEDM.2006.346801

[4] K. Kikuchi, M. Nishihara, H. Yamamoto, T. Yamamoto, S. Mizuno, F. Yamaki, and S. Sano, "An 8.5–10.0 GHz 310 W GaN HEMT for radar applications," in *Proc. IEEE MTT-S IMS*, Tampa, FL, USA, Jun. 2014, pp. 1–4. DOI: 10.1109/MWSYM.2014.6848404

[5] C. F. Campbell, Y. Liu, M.-Y. Kao, and S. Nayak, "High efficiency Ka-band gallium nitride power amplifier MMICs," in *Proc. IEEE Int. Conf. COMCAS*, Tel Aviv, Israel, Oct. 2013, pp. 1–5. DOI: 10.1109/COMCAS.2013.6685246

[6] T. Palacios, A. Chakraborty, S. Rajan, C. Poblenz, S. Keller, S. P. DenBaars, J. S. Speck, and U. K. Mishra, "High-power AlGaN/GaN HEMTs for Ka-band applications," *IEEE Electron Device Lett.*, vol. 26, no. 11, pp. 781–783, Nov. 2005. DOI: 10.1109/LED.2005.857701

[7] Y.-F. Wu, M. Moore, A. Saxler, T. Wisleder, and P. Parikh, "40-W/mm double field-plated GaN HEMTs," in *Proc. 64th Device Res. Conf.*, State College, PA, USA, Jun. 2006, pp. 151–152. DOI: 10.1109/DRC.2006.305162

[8] M. Rosker, C. Bozada, H. Dietrich, A. Hung, D. Via, S. Binari, E. Vivierios, E. Cohen, and J. Hodiak, "The DARPA wide band gap semiconductors for RF applications (WBGS-RF) program: Phase II results," in *Proc. CS MANTECH Conf.*, Tampa, FL, USA, 2009, pp. 1–4.

[9] M. Gordon. (2010). *Manufacturing Readiness Level Definitions*. [Online]. Available: http://www.dodmrl.com

[10] S. Nayak, M.-Y. Kao, H.-T. Chen, T. Smith, P. Goeller, W. Gao, J. Jimenez, S. Chen, C. Campbell, G. Drandova, and R. Kraft, "0.15 μm GaN MMIC manufacturing technology for 2–50 GHz power applications," in *Proc. CS MANTECH Conf.*, Scottsdale, AZ, USA, 2015, pp. 43–46.

[11] G. H. Jessen, R. C. Fitch, J. K. Gillespie, G. D. Via, N. A. Moser, M. J. Yannuzzi, A. Crespo, J. S. Sewell, R. W. Dettmer, T. J. Jenkins, R. F. Davis, J. Yang, M. A. Khan, and S. C. Binari, "High performance 0.14 μm gate-length AlGaN/GaN power HEMTs on SiC," *IEEE Electron Device Lett.*, vol. 24, no. 11, pp. 677–679, Nov. 2003. DOI: 10.1109/GAAS.2003.1252410

[12] G. H. Jessen, R. C. Fitch, J. K. Gillespie, G. Via, A. Crespo, D. Langley, D. J. Denninghoff, M. Trejo, and E. R. Heller, "Short-channel effect limitations on high-frequency operation of AlGaN/GaN HEMTs for T-gate devices," *IEEE Trans. Electron Devices*, vol. 54, no. 10, pp. 2589–2597, Oct. 2007. DOI: 10.1109/TED.2007.904476

[13] K. Skowronski, S. Nelson, R. Mongia, H. Sheehan, and S. Anderson, "An octave bandwidth, high PAE, linear, class J GaN high power amplifier," in *Proc. GOMACTECH*, Las Vegas, NV, USA, 2012, pp. 1–6.

[14] C. Essary, D. Ferwalt, J. Gassmann, D. Y. C. Lie, J. Lopez, R. Mongia, S. Nelson, K. O. S. Shichijo, and M. Walker, "Wideband class J high efficiency envelope tracked power amplifiers," in *Proc. GOMACTECH*, Charleston, SC, USA, 2014, pp. 351–353.

[15] M.-H. Weng, C.-K. Lin, J.-H. Du, W.-C. Wang, W.-K. Wang, and W. Wohlmuth, "Pure play GaN foundry 0.25 μm HEMT technology for RF applications," in *Proc. IEEE CSICS*, Monterey, CA, USA, Oct. 2013, pp. 1–4. DOI: 10.1109/CSICS.2013.6659243

[16] D. Floriot, V. Brunel, M. Camiade, C. Chang, B. Lambert, Z. Ouarch-Provost, H. Blanck, J. Grunenputt, M. Hosch, H. Jung, J. Splettstober, and U. Meiners, "GH25-10: New qualified power GaN HEMT process from technology to product overview," in *Proc. 9th EUMIC*, Rome, Italy, Oct. 2014, pp. 225–228. DOI: 10.1109/EuMIC.2014.6997833

[17] A. Hinoki, K. Hataya, H. Miyamoto, T. Nakayama, Y. Ando, T. Inoue, Y. Okamoto, M. Kuzuhara, T. Araki, A. Suzuki, and Y. Nanishi, "Influence of dry etching on nitride semiconductor Schottky characteristics," in *Proc. Int. Meeting Future Electron Devices*, Kyoto, Japan, Jul. 2004, pp. 71–72. DOI: 10.1109/IMFEDK.2004.1566413

[18] R. Fitch, J. Gillespie, D. Via, D. Agresta, T. Jenkins, G. Jessen, N. Moser, A. Crespo, A. Dabiran, and A. Osinsky, "Effect of silicon nitride PECVD growth on AlGaN/GaN HEMT dispersion and breakdown characteristics," in *Proc. Elect. Chem. Soc. SOTAPOCS*, Honolulu, HI, USA, 2004, pp. 459–464.