Novel Multi-Level Cell TFT Memory With an In–Ga–Zn-O Charge Storage Layer and Channel

Wen-Peng Zhang, Shi-Bing Qian, Wen-Jun Liu, Shi-Jin Ding, and David Wei Zhang

Abstract—Amorphous indium–gallium–zinc oxide (a-IGZO) thin-film transistor nonvolatile memory devices with an IGZO charge storage layer were evaluated for the first time for multi-level cell memory applications. The pristine device was defined as the original state (OS), which can be switched to the programmed state (PS) after a positive gate voltage pulse (for example, 12 V for 10 ms), and to the erased state (ES) after a negative gate voltage pulse (for example, −15 V for 10 ms). The writing mechanism was attributed to Fowler–Nordheim tunneling of electrons from the channel to the charge storage layer under a positive gate bias and inverse tunneling under a negative gate bias. The devices demonstrated superior electrical programmable and erasable characteristics. A memory window of 2.4 V between OS and PS was maintained after 100 programming/erasing cycles, and a memory window of 2.66 V between OS and ES as well. The memory windows relative to OS are equal to 1.91 and 1.30 V for PS and ES, respectively, for a retention time of 10^5 s.

Index Terms—In-Ga-Zn-O, multi-level cell, thin-film transistor, nonvolatile memory.

I. INTRODUCTION

IN RECENT years, amorphous indium-gallium-zinc-oxide (a-IGZO) thin-film transistor (TFT) nonvolatile memories have been widely researched as next-generation memory devices for flexible electronic systems and transparent panel systems [1]–[5]. This is because a-IGZO has many advantages over conventional amorphous or polycrystalline silicon, such as high electron mobility, good uniformity, low processing temperature, and transparency in the visible region of the spectrum [6], [7]. To date, a-IGZO TFT nonvolatile memory devices have been investigated using various charge storage layers [8]–[12], indicating that it is easy to attain a considerable positive threshold voltage shift (ΔV_{th}) through Fowler–Nordheim (F–N) tunneling of electrons when the gate is positively biased. A high program efficiency can be easily achieved. However, because a-IGZO is a natural n-type semiconductor, hole conduction is difficult [13]. This means the a-IGZO TFT memory devices have poor erase efficiencies because of the lack of holes in the channel layer [4], [8].

The programmed device cannot be easily erased through F–N tunneling of holes from the channel into the charge storage layer when the gate is negatively biased. To enhance the erasure efficiency, ultraviolet or other light was used to erase the programmed device [4], [11]; however, this is not compatible with the electrical erasure-based memory technology. Although it was reported that an a-IGZO TFT memory with an a-IGZO charge storage layer could be electrically erased by band-to-band tunneling-induced hot-hole injection, a source-drain bias greater than 9 V was required [5]. This will cause concerns about power consumption.

In this letter, a novel multi-level nonvolatile TFT memory cell was reported for the first time using a-IGZO as the charge storage layer and the channel layer. The program/erase endurance between the programmed state (PS) and the original state (OS), or OS and the erased state (ES) was demonstrated with a large memory window. The memory window between PS and ES is as large as 3.2 V at a retention time of 10^5 s and room temperature.

II. EXPERIMENTAL PROCEDURE

Highly doped n-type Si (100) wafers with a resistivity of 0.001–0.004 $\Omega \cdot$ cm were cleaned using the standard RCA process and were used as the starting substrates for the a-IGZO TFT memory devices. First, a 35-nm Al_2O_3 film was deposited as a blocking layer by atomic layer deposition (ALD). Then, a 20-nm a-IGZO layer was deposited by sputtering, followed by photolithography and wet etching (with diluted HCl acid) to form a charge storage layer. Subsequently, an 8-nm Al_2O_3 film was deposited using ALD, which served as a tunneling layer and surrounded the a-IGZO charge storage layer. A 40-nm a-IGZO film was sputtered, which was followed by the formation of active channels using photolithography and wet etching. The 100-nm-thick Mo source and drain contacts were formed on the a-IGZO channel layer by sputtering a Mo target and using a lift-off technique. Finally, the fabricated devices were annealed in air at 300 °C for 1 h. The ALD Al_2O_3 films were grown at 250 °C using $Al(CH_3)_3$ and H_2O precursors. The IGZO films were deposited by radio frequency (RF) magnetron sputtering at room temperature with a ceramic target of $InGaZnO_4$. During the sputtering, the RF power, working pressure, and Ar flow rate were 110 W, 0.88 Pa, and 50 sccm, respectively. A TFT without a-IGZO charge storage layer was also fabricated for comparison.

Electrical measurements were performed on devices with a channel length of 10 μm and a channel width of 50 μm
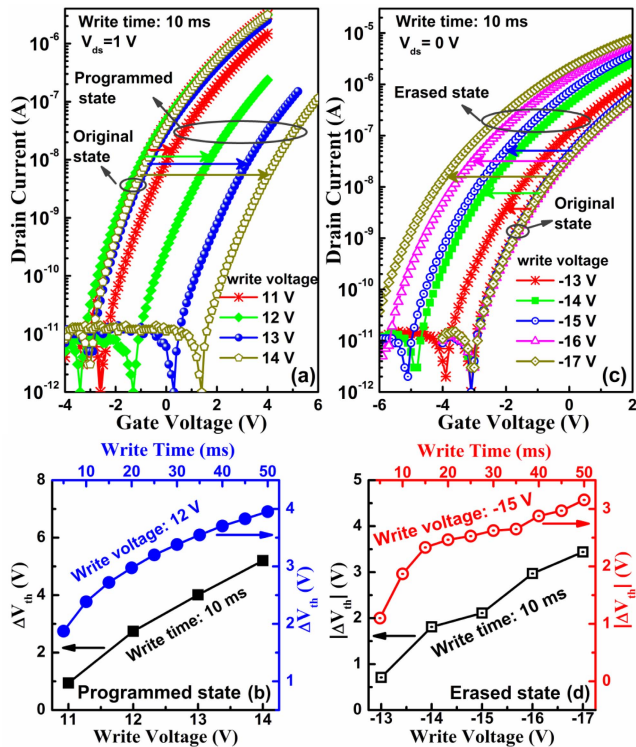
Fig. 1. (a) The transfer curves of the pristine devices and those written at various positive gate biases for a constant time of 10 ms. (b) A plot of ΔV_{th} versus write voltage for a write time of 10 ms and ΔV_{th} versus write time at 12 V. (c) The transfer curves of the pristine devices and those written at various negative gate biases at a constant time of 10 ms. (d) A plot of $|\Delta V_{th}|$ versus write voltage for a write time of 10 ms and $|\Delta V_{th}|$ versus write time at −15 V.
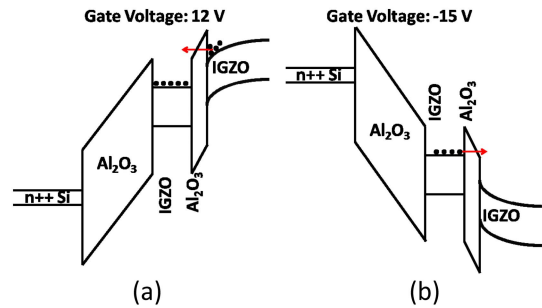

Fig. 2. Energy band diagrams of the device being written (a) at $V_g = 12$ V and $V_{ds} = 1$ V and (b) at $V_g = -15$ V and $V_{ds} = 0$ V.

using a semiconductor device analyzer (Agilent B1500A) at room temperature. The threshold voltage (V_{th}) is defined as the gate voltage where the drain current equals the channel width/length ratio (W/L) $\times 10^{-8}$ A.

III. RESULTS AND DISCUSSION

Figure 1 shows the programming (or writing) characteristics of the fabricated a-IGZO TFT memory devices with a charge storage layer of a-IGZO under positive and negative gate voltages. For each write operation, we used a pristine device to avoid effects from the last write cycle. The effective electron mobility and sub-threshold swing were extracted to be 2.0 cm^2/V·s and 0.84 V/dec, respectively. When a positive bias pulse was applied to the gate, the resulting drain current-gate voltage ($I_d - V_g$) curve shifted to the right of the initial curve and moved towards a positive bias as the write voltage increased, shown in Fig. 1 (a). This is regarded as switching of the device from OS to PS. Also, as shown in Fig. 1(b), the ΔV_{th} increased from 0.94 to 5.20 V as the write voltage increased from 11 to 14 V with a constant write time of 10 ms. When the write voltage was fixed at 12 V, the ΔV_{th} increased from 1.87 to 3.95 V as the write time increased from 5 to 50 ms. These data indicate that the present TFT memory has a high program efficiency under a positive gate bias. However, for the a-IGZO TFT without an IGZO charge storage layer, the device demonstrated a very small ΔV_{th} of 0.16 V

even after 30 min of programming at a high gate bias of +20 V (not shown here). This indicates that the Al$_2$O$_3$ dielectric had a good quality, and the TFT without the charge storage layer of IGZO was unable to capture adequate electrons to satisfy the memory requirements. On the other hand, when a negative bias pulse was applied to the gate, the $I_d - V_g$ curve shifted to the left of the initial curve. This shift became larger with increasing gate bias, shown in Fig. 1(c). This is regarded as switching of the device from OS to ES. As illustrated in Fig. 1(d), the absolute value of ΔV_{th} ($|\Delta V_{th}|$) increased from 0.71 to 3.44 V when the write voltage increased from −13 to −17 V for a constant write time of 10 ms. Additionally, when the write voltage was fixed at −15 V, the $|\Delta V_{th}|$ increased from 1.1 to 3.16 V with an increase in the write time from 5 ms to 50 ms.

The above writing behaviors can be explained with energy band diagrams of the device in Fig. 2. For a positive gate bias of 12 V, electrons in the accumulation layer of the a-IGZO channel can be easily injected into the charge storage layer by F–N tunneling, shown in Fig. 2(a). Under a negative gate bias of −15 V, the channel of a-IGZO was depleted because it is difficult to invert an a-IGZO channel to p-type [13]. Electrons from the a-IGZO charge storage layer, which had a high electron concentration of 3.5×10^{19} cm^{-3} by Hall effect measurement, were injected into the a-IGZO channel through F–N tunneling due to a small barrier height, indicated in Fig. 2(b). Therefore, net positive charges remained in the charge storage layer after this programming. Otherwise, for the memory devices with a charge storage medium of Pt nanocrystals or Zn-doped Al$_2$O$_3$, the light or ultraviolet instead of electrical pulse could be used to effectively erase the programmed devices [4], [11]. This is ascribed to injection of holes generated by photons excitation in the a-IGZO channel.

The programming/erasing (P/E) characteristics of the multi-level TFT memory devices are shown in Fig. 3. When a positive bias pulse of 12 V was applied for 10 ms on the gate, the device was switched from OS to PS, as shown by the black arrow in Fig. 3(a). When a negative gate bias pulse of −12 V was applied for 20 ms, the resulting $I_d - V_g$ curve almost returned to the initial position corresponding to the pristine device, shown by the red arrow. This indicates that the programmed device can be erased to its initial state by an electrical pulse, demonstrating an easy switch between PS and OS. Repeated P/E operations between OS to PS were
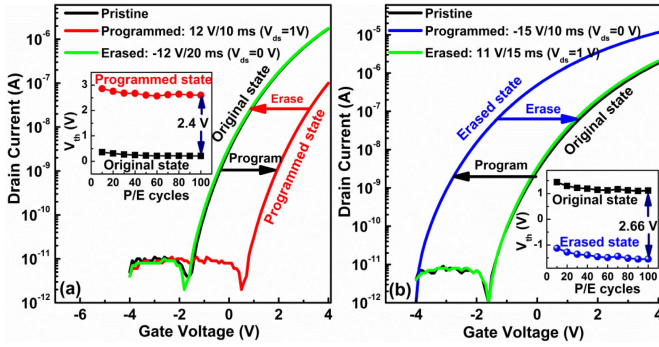
Fig. 3. (a) P/E characteristics related to PS and OS. The inset shows ΔV_{th} as a function of P/E cycles for the two states. (b) P/E characteristics associated with OS and ES. The inset shows the dependence of ΔV_{th} on the number of P/E cycles for the two states.
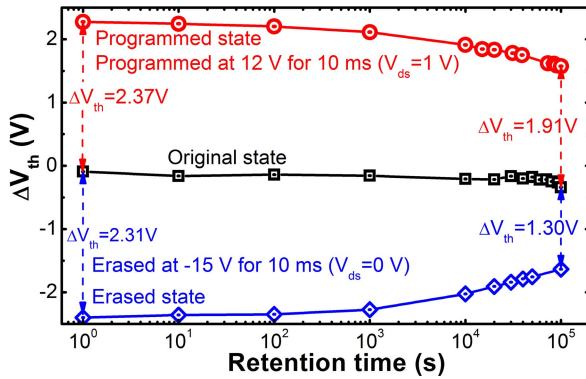

Fig. 4. Data retention characteristics of the memory devices in OS, PS and ES at room temperature, respectively.

successfully demonstrated. The memory window was 2.4 V after 100 P/E cycles, as shown in the inset of Fig. 3 (a). When a negative bias pulse of -15 V for 10 ms was applied to the gate, the device switched from OS to ES, as shown by the black arrow in Fig. 3(b). After a positive bias pulse of 11 V was applied for 10 ms to the gate, the device was restored to its initial state, shown by the blue arrow. This demonstrates good electrical program-erase characteristics between OS and ES. Additionally, a memory window as large as 2.66 V was maintained between OS and ES after 100 P/E cycles, as shown in the inset of Fig. 3 (b).

Figure 4 shows the data retention characteristics of the memory devices in OS, PS and ES, respectively, at room temperature. For the device in OS, the V_{th} exhibited a very small change with retention time, *i.e.*, $\Delta V_{th} = 0.34$ V at 10^5 s. For the device programmed at 12 V for 10 ms (*i.e.*, in PS), the memory window relative to the initial state of a pristine device gradually decreased to 1.91 V with an increase in the retention time of up to 10^5 s. For the device programmed at -15 V for 10 ms (*i.e.*, in ES), the window relative to the

initial state decreased to 1.30 V at a retention time of 10^5 s. The degradation can be attributed to the leakage of charges stored in the a-IGZO charge storage layer. For PS and ES, a memory window as large as 3.2 V can be attained at 10^5 s.

IV. CONCLUSION

An a-IGZO TFT memory device with an a-IGZO charge storage layer was fabricated using a maximum temperature of 300 °C. The fabricated devices displayed stable multi-level states. OS corresponds to the pristine device. PS and ES can be achieved by writing at positive and negative gate biases, respectively. The devices demonstrated electrical programmable and erasable characteristics and good endurance between OS and PS, or OS and ES as well as data retention capability. Therefore, the a-IGZO TFT memory device with the a-IGZO charge storage layer has promising applications in flexible and transparent electronics.

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