Accumulation-Based Computing Using Phase-Change Memories With FET Access Devices

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***Abstract*— Phase-change materials and devices have received much attention as a potential route to the realization of various types of unconventional computing paradigms. In this letter, we present non-von Neumann arithmetic processing that exploits the accumulative property of phase-change memory (PCM) cells. Using PCM cells with integrated FET access devices, we perform a detailed study of accumulation-based computation. We also demonstrate efficient factorization using PCM cells, a technique that could pave the way for massively parallelized computations.**

***Index Terms*— Phase-change materials, non-von Neumann, arithmetic computing, neuromorphic computing.**

I. Introduction

RECENTLY, phase-change materials have been integrated into various types of neuromorphic and biologically-inspired computing architectures [1], [2]. The majority of such work focuses on the use of phase-change materials as tunable, weighting elements to mimic the operation of a synapse [3]–[5]. However, phase-change materials have also been shown to be capable of providing a powerful form of arithmetic, or *accumulation-based*, computing [1], [6], [7]. In the latter scheme, a predetermined number of identical electrical pulses are used to excite, in sequence, an initially amorphous PCM cell. The excitation pulses are configured such that (owing to percolation effects) only after all pulses of the predetermined sequence have been applied does the resistance of the cell fall to that of the SET (low-resistance) state [1]. An accumulation-based scheme does not require separate resistance levels to be recognized with precision; state identification is carried out by counting the pulses needed to switch a cell to the SET state (from any state) [1]. In this letter we demonstrate for the first time how accumulation-based computations can be performed entirely on 'mushroom'-type PCM cells fabricated in the 90-nm technology node and equipped with a FET access device [8]. The purpose of the FET access device is to circumvent the well-known electrical sneak path and to eliminate V_{WL}, V_{BL} voltage disturb issues of standard crossbar architectures [9], as well as to provide better current control capability by regulating the maximum programming current during a RESET/SET event.

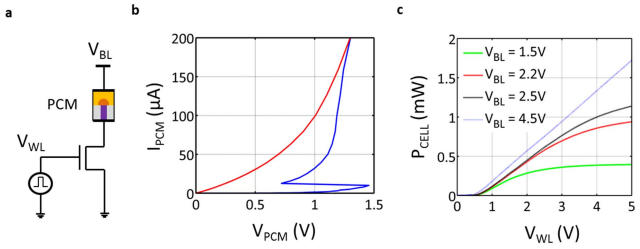

Fig. 1. **a** Schematic of the PCM device used in this work. The subscripts BL and WL refer to the bit line and word line, respectively. **b** Representative *I-V* characteristic of a PCM cell employed in this study. **c** Variation of power dissipated in the PCM cell as a function of V_{WL} and V_{BL}.

II. Experiments and Discussion

A schematic representation of the memory cell used in this work is shown in Figure 1**a**. A representative current-voltage characteristic of a typical cell is shown in Figure 1**b**. A threshold voltage V_{th} of 1.5 V followed by a pronounced voltage 'snap-back' and an increase in conductivity are observed, all well-known characteristics of PCM cells. The variation of power dissipated in the PCM cell versus the word-line and bit-line voltages is shown in Figure 1**c**.

We begin by analyzing the effect of increasing the FET gate voltage, V_{WL}, on the accumulation property of the PCM cell. As the PCM cell is in series with the channel of the FET, controlling the gate voltage is an effective way of controlling the current through the memory cell. In accumulation-based computing using PCM cells, the computational sequence is as follows: a PCM cell is initially RESET using a combination of fast, high-amplitude pulses ($V_{WL\ RESET}$ = 2.2 V, pulse width (PW) = 120 ns, leading edge (LE) = 20 ns, trailing edge (TE) = 3 ns; $V_{BL\ RESET}$ = 2.2 V). The device is then systematically excited with identical pulses, designated $V_{WL\ EXC}$ and $V_{BL\ EXC}$, respectively, until the cell resistance drops below a 'decision-level' value of 3.1 MΩ, an arbitrary resistance value fixed for the experiments reported herein.

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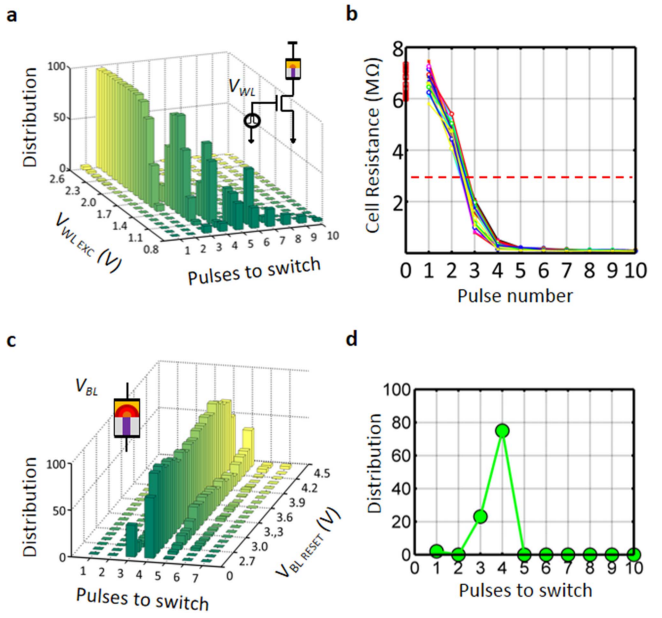

Fig. 2. **a** The effect of $V_{\mathrm{WL\,EXC}}$ on the accumulation properties of PCM cells. **b** The variation of cell resistance versus pulse number for the $V_{\mathrm{WL\,EXC}} = 1.4$ V series (note that data for pulse '0' are the initial reset state resistances). **c** Effect of increasing VBL RESET on the accumulation properties of PCM cells. **d** An extract from c, for $V_{\mathrm{BL\,RESET}} = 2.6$ V.

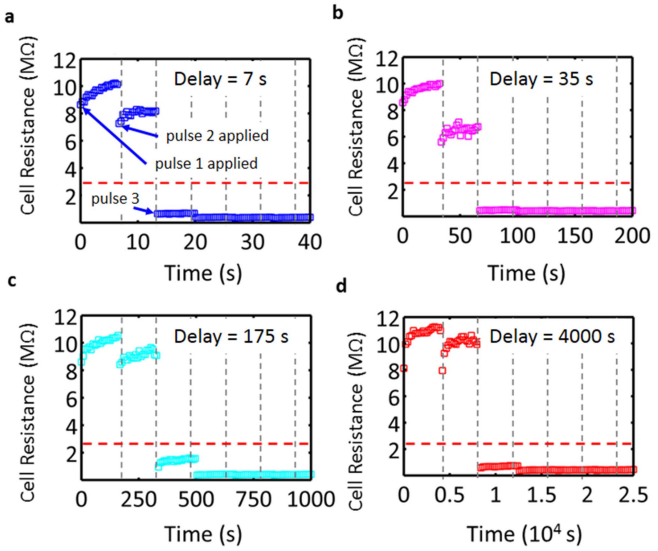

Fig. 3. Accumulation-based computing: a time domain stability study of the intermediate states with a PCM cell. Identical excitation pulses are applied while instructing the control algorithm to wait a specific amount of time (in seconds) between pulses. Increasing time delays of **a** 7 s, **b** 35 s, **c** 175 s and **d** 4000 s are investigated; no substantial difference is observable; the cell switches reliably after 3 pulses.

The number of excitation pulses required to reach this predetermined decision-level resistance (i.e. the result) is stored. To better understand the correlation between excitation current and accumulation properties, we repeat the entire experiment for $V_{\mathrm{WL\,EXC}}$ values ranging from 0.8 V to 2.6 V in 0.1 V steps (with V_{BL} fixed at 1.5 V). Each step is repeated 100 times; an example of this is shown in Figure 2**a**. These results show how increasing the gate pulse amplitude has a direct effect on the accumulation properties of the PCM cells. Lower gate voltage values allow less current to flow through the memory cell, therefore more pulses are needed to reach full crystallization [10]. This can thus be viewed as a change in the arithmetic base of the system (i.e. counting can be performed in base-2, base-3, etc.). More importantly, base-2 and base-3 computations are fairly repeatable, but the reliability of the accumulation scheme decreases for higher bases (as evident in Figure 2**a**). In Figure 2**b**, the variation of cell resistance as a function of the number of applied pulses is shown for the $V_{\mathrm{WL\,EXC}} = 1.4$ V series, where cells mostly switch after three pulses.. In the next set of experiments, we test the impact that the RESET pulse has on the accumulation properties. It is well known that the re-amorphized region in a PCM mushroom cell can be increased in size by increasing the power injected during a RESET pulse [11]. We therefore investigate the number of pulses required to switch a cell for different levels of RESET ($V_{\mathrm{WL\,RESET}} = 3.5$ V, LE = 20 ns, PW = 120 ns, TE = 3 ns; $V_{\mathrm{BL\,RESET}} = 2.5$ V to 4.5 V) while keeping the excitation pulses $V_{\mathrm{WL\,EXC}}$ and $V_{\mathrm{BL\,EXC}}$ fixed. We start by re-amorphizing one cell using increasingly higher values of $V_{\mathrm{BL\,RESET}}$ while keeping all the other parameters fixed. The cell is then pulsed using identical excitation pulses ($V_{\mathrm{WL\,EXC}} = 0.75$ V, LE = 50 ns, PW = 120 ns, TE = 50 ns; $V_{\mathrm{BL\,EXC}} = 2.15$ V) until the cell resistance value drops below the aforementioned decision level of 3.1 MΩ; the number of pulses required is recorded and displayed for each $V_{\mathrm{BL\,RESET}}$ value in Figure 2**c**. As expected, the higher the $V_{\mathrm{BL\,RESET}}$ value, the larger *is* the amorphous region that is formed after the RESET pulse; therefore accumulation requires an increasing number of pulses. Figure 2**d** shows the distribution trend for $V_{\mathrm{BL\,RESET}} = 2.6$ V; we see that the cell required 3 pulses to switch for $< 30\%$ of the time, whereas it needed 4 pulses for $> 70\%$ of the time. These results show how the accumulator response can be tuned by appropriate choices of the excitation and RESET pulse characteristics. Note that no specific steps in terms of the design of the cells, the materials and the shape of excitation pulses were taken to improve the performance of this accumulation-based computational scheme. It is therefore expected that future work might increase the reliability of the scheme by fine-tuning all these aspects.

Accumulation works by increasing, upon the receipt of each excitation pulse, the number and size of crystalline nuclei within the amorphous region of the cell until a percolation path is created and full crystallization is achieved. The stability over time of these intermediate (storage) states is a question of fundamental importance for the realization of phase-change-based computers. We therefore carried out an additional set of experiments in an effort to understand this stability. We started by identifying a combination of pulses that would reliably switch a cell with 3 excitation pulses. We then re-amorphized the cell and applied identical excitation pulses while instructing the control algorithm to wait a specific amount of time (in seconds) between the pulsing sequences. The resistance of the cell was monitored at all times using a low current signal. The results of the experiment with time delays of 7 s, 35 s, 175 s and 4000 s are shown in Figure 3**a**, **b**, **c** and **d**, respectively: The cell reaches the predetermined decision-level resistance after 3 pulses regardless of the time delay between their application (at

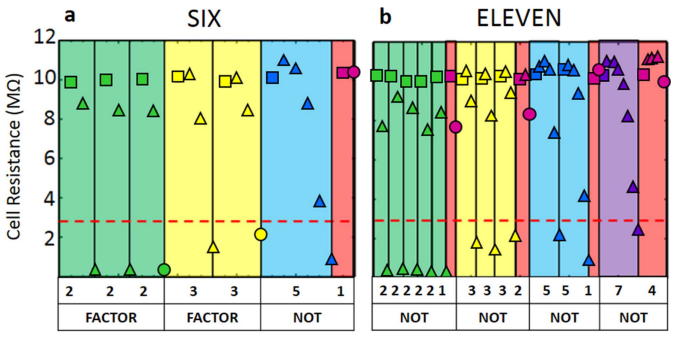

Fig. 4. Finding factors of the numbers 6 and 11, **a** and **b**, respectively, using a single PCM cell. Squares indicate RESET states, triangles intermediate resistance states and circles the end state of a particular factorization test sequence.

least up to 4000 s), and the intermediate states are stable between each pulse. We observe a gradual increase in resistance (resistance drift) between pulses due to structural relaxation of the amorphous phase [12]. However, as we are not sensing the resistance *per se* in the accumulation regime, such drift does not affect our ability to 'compute'. This can be physically explained by considering that the crystallizing pulses applied result in temperatures at which the material is in the super-cooled liquid state and where the crystal growth becomes largely independent of the state of relaxation [10]. Hence, as shown in Figure 3, this implies that structural relaxation does not seem to have a significant effect on the crystallization dynamics, and therefore also has little impact on the relationship between the delay time and the number of pulses subsequently required to reach the decision level resistance. Our results are thus very encouraging in terms of developing a PCM-based non-von Neumann computer that both computes and stores data in the same physical location.

Finally, we demonstrate how a well-characterized phase-change accumulator cell can readily perform advanced arithmetic, such as factorization. Finding the factors of a number is a demanding computational task, but can be carried out by a single PCM cell here. Figure 4 shows two examples of PCM accumulator-based factorization for the numbers 6 and 11. The scheme works by repeatedly exciting a PCM cell 'designed' to switch after Y pulses, with Y being the potential factor of X. As X is always bigger than Y (otherwise it would be impossible for Y to be a factor of X), every time the control algorithm excites the cell Y times, the cell reaches the decision level. At this point, the cell is RESET and the pulsing sequence restarts. The number Y is a factor of X if and only if the PCM cell is below the decision-level after the last pulse (pulse number X) of the sequence. Figure 4**a** shows an example where 2 (Y) is being examined as possible factor of 6 (X). The pulse sequence excites the PCM cell $2 + 2 + 2$ times and the cell falls below the decision level with the last pulse of the last series of 2, therefore 2 is a factor of 6. A similar response is achieved for the number 3 (which of course is also a factor of 6), but not for the number 5, where the cell remains above the decision-level resistance after receipt of the last pulse of the sequence. Similarly, in Figure 4**b** we demonstrate factorization of the number 11 which, being a prime, is not factorable by any of the numbers we tried (i.e. 2, 3, 5 and 7). It is reasonable to expect that future systems could probe in parallel, all the factors possible via multiple PCM cells, a solution that would ultimately reduce the amount of enabling CMOS circuitry required, such as digital counters.

III. Conclusion

In conclusion we have demonstrated how CMOS-integrated PCM memory cells with FET access devices can be used to perform arithmetic operations using an accumulator-based computational scheme. We characterized the effect of the excitation regime on the performance of the cells and demonstrated advanced arithmetic capabilities, such as factorization. We also verified that the intermediate states between pulses are accessible for up to at least an hour. This demonstrates that with a phase-change accumulator, one can realize a form of non-von Neumann computing in which the intermediate states of a particular calculation may be stored simultaneously by the very same cell that carries out the computation itself. Finally, further scaling to smaller devices would substantially reduce the power consumption required by this scheme without affecting its computational properties.

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