Full ALD $Al_2O_3/ZrO_2/SiO_2/ZrO_2/Al_2O_3$ Stacks for High-Performance MIM Capacitors

Qiu-Xiang Zhang, Bao Zhu, Shi-Jin Ding, Hong-Liang Lu, Qing-Qing Sun, Peng Zhou, and Wei Zhang

***Abstract*— Metal–insulator–metal (MIM) capacitors with full atomic-layer-deposition $Al_2O_3/ZrO_2/SiO_2/ZrO_2/Al_2O_3$ stacks were explored for the first time. As the incorporated SiO_2 film thickness increased from 0 to 3 nm, the quadratic and linear voltage coefficients of capacitance (α and β) of the MIM capacitors reduced significantly from positive values to negative ones. For the stack with 3-nm SiO_2 film, a capacitance density of 7.40 fF/μm^2, α of -121 ppm/V^2, and β of -116 ppm/V were achieved, together with very low leakage current densities of 3.08×10^{-8} A/cm^2 at 5 V at room temperature (RT) and 5.89×10^{-8} A/cm^2 at 3.3 V at 125 °C, high breakdown field of 6.05 MV/cm, and high operating voltage of 6.3 V for a 10-year lifetime at RT. Thus, this type of stacks is a very promising candidate for next generation radio frequency and analog/mixed-signal integrated circuits.**

***Index Terms*— Atomic-layer-deposition, voltage coefficients of capacitance, $Al_2O_3/ZrO_2/SiO_2/ZrO_2/Al_2O_3$, metal-insulator-metal.**

I. Introduction

HIGH-κ metal-insulator–metal (MIM) capacitors have recently been studied for radio frequency (RF) and analog/mixed-signal (AMS) integrated circuits (ICs) to meet the requirement of high capacitance density [1]–[4]. However, a high degree of voltage nonlinearity remains a major concern for practical applications while maintaining high enough capacitance density [1], [4]. In particular, quadratic voltage-coefficient-of-capacitance (VCC) is regarded as a critical criterion to judge voltage linearity of MIM capacitor. Recently, it has been reported that satisfying α values can be attained by employing different dielectrics with positive and negative α values [5]–[7]. However, all of these involve multiple instruments and methods to prepare the entire insulating stacks of MIM capacitor. This not only increases fabrication complexity and cost, but also imposes a high risk of contamination and impurity incorporation. Therefore, it is highly desired to assemble the entire insulating stack in the same deposition system. Furthermore, since the atomic-layer- deposition (ALD) technique has various advantages such as low temperature processing, excellent large area uniformity, accurate thickness control etc, high quality dielectrics can be thus obtained by means of ALD [8], ensuring low leakage current and high breakdown field. In a word, to meet the requirements of high performance MIM capacitors, it is indispensable to engineer new insulator configurations with ALD.

In this letter, $Al_2O_3/ZrO_2/SiO_2/ZrO_2/Al_2O_3$ (AZSZA) stacks were assembled by ALD in the same chamber without vacuum interruption. The voltage linearity of MIM capacitor was improved significantly by optimizing the thickness of SiO_2 while maintaining enough high capacitance density. Especially the MIM capacitor exhibits very low leakage current density, high breakdown electric field and robust reliability.

II. Experimental Procedure

By means of ALD in the same deposition chamber without breaking the vacuum, various AZSZA stacks were assembled at 250 °C atop a sputtered TaN (150 nm) bottom electrode, which was deposited on a 500 nm PECVD-SiO_2 film. The thicknesses of individual Al_2O_3 and ZrO_2 layers were optimized at 1 nm and 7 nm, respectively. To study how the SiO_2 layer thickness modulated α value, different thicknesses of SiO_2 (0, 1, 2 and 3 nm) were incorporated, which were grown from $[(CH_3)_2N]_3SiH$ and O_2 by plasma ALD. Al_2O_3 and ZrO_2 were deposited respectively from $Al(CH_3)_3/H_2O$ and $[(CH_3)_2N]_4Zr/H_2O$ by thermal ALD. A sputtered 150 nm TaN layer was used as a top electrode layer. The MIM capacitors were defined by photolithography and dry etching. Finally, the fabricated capacitors were annealed in a rapid thermal annealing (RTA) system at 420 °C for 5 min in forming gas. The dielectric film thickness was measured by ellipsometer and confirmed by transmission electron microscopy (TEM). During assembly of various stacks, the thickness of individual films was controlled through deposition cycles. Capacitance–voltage (C–V) and current-voltage (I–V) measurements were carried out on a precision impedance analyzer (Agilent 4294A) and a semiconductor device analyzer (Agilent B1500A). For the C–V test, the parallel equivalent circuit of a capacitor and a resistor was used, which aimed to extract more precise capacitance from impedance especially for easy leakage dielectrics [9].

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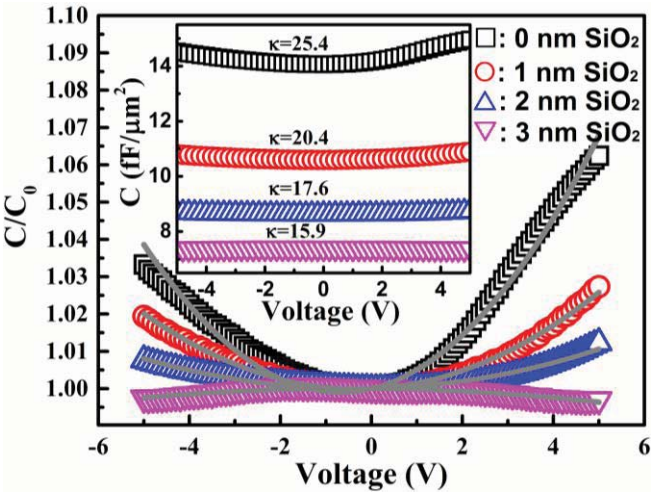

Fig. 1. Typical plotting of C/C_0 versus voltage at 100 kHz together with the fitted curves for various MIM capacitors, and the inset shows corresponding C–V curves at 100 kHz and the extracted κ values.

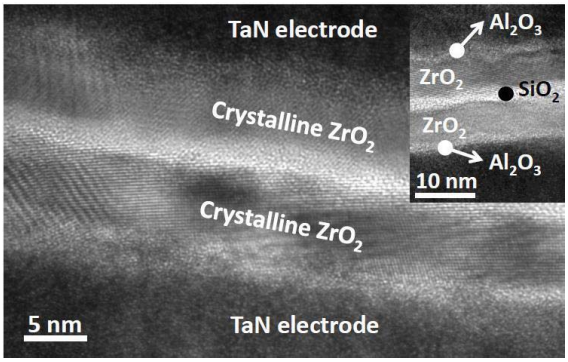

Fig. 2. Cross-section TEM image of the MIM capacitor with 3 nm SiO_2.

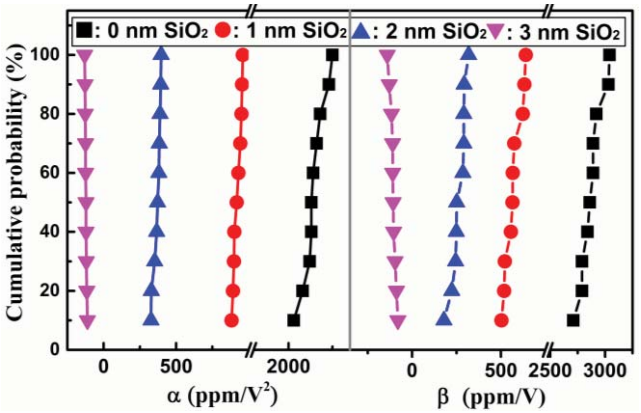

Fig. 3. The cumulative distributions of α and β values for various MIM capacitors at 100 kHz.

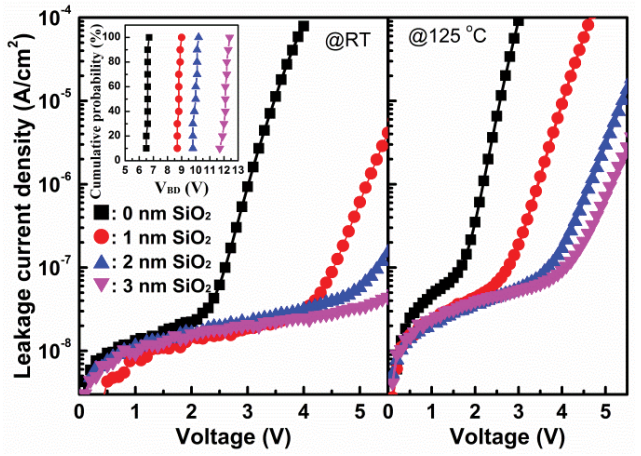

Fig. 4. Dependence of J on V for various MIM capacitors at RT and 125 °C, respectively. The insert illustrates the cumulative probability of breakdown voltage (V_{BD}) for the MIM capacitors (size: 100 × 100 μm^2) at RT.

III. Results and Discussion

VCCs are very important parameters for MIM capacitor applications, and can be obtained by fitting the C–V data with a second order polynomial equation of $C(V) = C_0(\alpha V^2 + \beta V + 1)$, where C_0 is the capacitance at zero-bias. α and β represent the quadratic and linear VCCs, respectively. Fig. 1 shows typical plotting of C/C_0 versus voltage at 100 kHz for the MIM capacitors with different thicknesses of SiO_2, and the inset shows the C-V curves for all the capacitors. In absence of SiO_2, the capacitor shows a sharp upward parabolic curve, which corresponds to a large positive α value. As the thickness of SiO_2 increases from 1 to 2 nm, the upward parabolic curve becomes flatter and flatter, reflecting decreasing α values. When the SiO_2 film is increased to 3 nm, the parabolic curve becomes downward and flat. This indicates an achievement of a small negative α value. In addition, the corresponding capacitance density exhibits a decrease from 14.06 to 7.40 fF/μm^2 (see the inset of Fig. 1), and the extracted dielectric constants (κ) of the overall stacks are 25.4, 20.4, 17.6 and 15.9, respectively. Such high κ values are related to the presence of crystalline ZrO_2 layers, as shown in Fig. 2.

The cumulative distributions of the extracted α and β for different MIM capacitors are illustrated in Fig. 3. As the thickness of SiO_2 increases from 0 to 3 nm, α decreases sharply from 2130 to −121 ppm/V^2 at 50% cumulative probability, and β decreases remarkably from 2920 to −116 ppm/V. It is worthwhile to mention that the α value can be further reduced to near zero if the thickness of SiO_2 decreases to the range of 2 ∼ 3 nm, meanwhile, a capacitance density higher than 7.40 fF/μm^2 is highly anticipated. This can well satisfy the requirements of MIM capacitors by the year 2017 (>7 fF/μm^2, <100 ppm/V^2) [10].

Fig. 4 shows the leakage current density-voltage ($J - V$) characteristics of all the capacitors at room temperature (RT) and 125 °C for electron top injection. Regarding our MIM capacitor with 3 nm SiO_2, J at 3.3 V is equal to 2.19 × 10^{-8} A/cm^2 and 5.89 × 10^{-8} A/cm^2 at RT and 125 °C, respectively. It should be noted that the J exhibits a little increase for electron bottom injection compared with top injection, which is likely due to degraded interface quality caused by exposure of the bottom TaN to the chemicals during ALD and to the atmosphere before dielectric deposition. In addition, the inset in Fig. 4 shows the breakdown voltage distributions of various capacitors. With increasing the thickness of SiO_2 from 0 to 3 nm, the breakdown voltage increases obviously from 6.6 to 12.1 V at 50% breakdown probability. Thus, the breakdown electric field of the whole stack is as large as 6.05 MV/cm for 3 nm SiO_2. Compared to the stacked

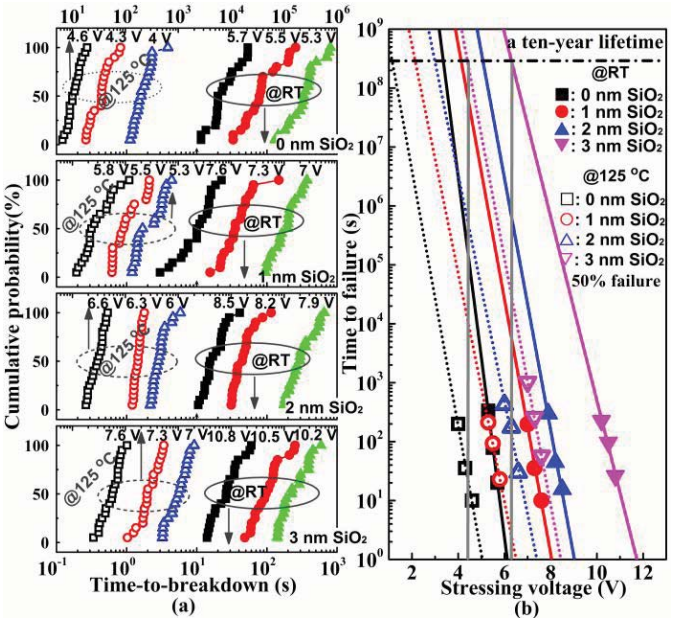

Fig. 5. (a) Cumulative TDDB curves under various constant voltage stressing for all the MIM capacitors (size: 50 × 50 μm^2) at room temperature and 125 °C. (b) Lifetime projection of the MIM capacitors at 50% failure probability.

TABLE I
COMPARISON OF OUR CAPACITOR WITH OTHER MIM CAPACITORS

Dielectric [Ref.]	Preparation method	C (fF/μm^2)	J (A/cm^2) @RT	α (ppm/V^2); β (ppm/V)
AZSZA [our work]	Full ALD	7.40	2.19×10^{-8}@3.3 V 3.08×10^{-8}@5 V	−121; −116
H/S [5]	ALD/PECVD	6	1×10^{-8}@3.3 V	14; 60
S_m/S [6]	Sputter/PECVD	7.2	2×10^{-7}@3.3 V	140; 440
Z/S [7]	—	8.15	5×10^{-5}@2 V	455; 489
E/S [11]	Sputter/ALD	7	2×10^{-7}@3.3 V	−255; —
A/H/A [12]	Full ALD	8.2	2×10^{-8}@2 V	1480; —

Remark: A=Al_2O_3, H=HfO_2, Sm=Sm_2O_3, Z=ZrO_2, S=SiO_2, E=Er_2O_3.

SiO_2/ZrO_2 MIM capacitors [7], such low leakage current density and high breakdown field are due to the incorporation of amorphous Al_2O_3 barriers and an intermediate SiO_2 layer, hence improving the interfacial quality, increasing the barrier height of TaN/insulator, and terminating the grain boundaries extending from the top to the bottom within the crystalline ZrO_2 film [4].

To assess the lifetimes of all the MIM capacitors, the time-to-breakdown characteristics were measured under different constant voltage stress (CVS) at RT and 125 °C, and the operating voltages corresponding to a ten-year lifetime were also projected, see Fig. 5. The operating voltage for a 10-year lifetime increases from 3.1 V to 6.3 V at RT as the thickness of SiO_2 changes from zero to 3 nm for a 50% failure probability. Even at 125 °C, the 10-year operating voltage can be as high as 4.4 V for the capacitor with 3 nm SiO_2, and the deduced activation energy under 8 V CVS is 1.11 eV. Moreover, the traces of leakage current versus stressing time did not show early failure (not shown here). These reflect very good reliability of the ALD AZSZA stacks for practical applications. Finally, we compares our MIM capacitors (SiO = 3 nm) with other reported ones, as shown in Table I. In the case of comparable capacitance density, our capacitors exhibit superior leakage characteristics and VCCs [6], [7], [11], [12]. Kim et al reported very small VCCs of MIM capacitor, but the corresponding capacitance density is distinctly lower than that in our letter [5]. On the other hand, some researchers achieved higher capacitance densities and small VCCs of MIM capacitors by introducing much higher κ materials such as TiO_2 [3], $SrTiO_3$ [13], $BaZr_yTi_{1-y}O_3$ [14], however, the leakage current and breakdown characteristics of these capacitors were quite poor.

IV. CONCLUSION

MIM capacitors with full ALD AZSZA stacks have been fabricated for the first time. By increasing the SiO_2 thickness from 0 to 3 nm, both α and β can be significantly improved. The MIM capacitor with 3 nm SiO_2 displays desirable characteristics such as a capacitance density of 7.40 fF/μm^2, α of −121 ppm/V^2, β of −116 ppm/V, extremely low leakage current of 3.08×10^{-8} A/cm^2 at 5 V, high breakdown field of 6.05 MV/cm and a high operating voltage of 6.3 V for a 10-year lifetime at RT. All of these results indicate that the AZSZA insulator is a very promising candidate for MIM capacitors in RF and AMS ICs.

REFERENCES

[1] T. Ishikawa *et al.*, "High-capacitance Cu/Ta_2O_5/Cu MIM structure for SoC applications featuring a single-mask add-on process," in *IEEE IEDM Tech. Dig.*, Dec. 2002, pp. 940–942.
[2] H. Hu *et al.*, "MIM capacitors using atomic-layer-deposited high-κ $(HfO_2)_{1-x}(Al_2O_3)_x$ dielectrics," *IEEE Electron Device Lett.*, vol. 24, no. 2, pp. 60–62, Feb. 2003.
[3] Y.-H. Wu *et al.*, "MIM capacitors with crystalline-TiO_2/SiO_2 stack featuring high capacitance density and low voltage coefficient," *IEEE Electron Device Lett.*, vol. 33, no. 1, pp. 104–106, Jan. 2012.
[4] S.-J. Ding *et al.*, "High-performance MIM capacitor using ALD high-k HfO_2-Al_2O_3 laminate dielectrics," *IEEE Electron Device Lett.*, vol. 24, no. 12, pp. 730–732, Dec. 2003.
[5] S. J. Kim *et al.*, "Improvement of voltage linearity in high-κ MIM capacitors using HfO_2-SiO_2 stacked dielectric," *IEEE Electron Device Lett.*, vol. 25, no. 8, pp. 538–540, Aug. 2004.
[6] J.-D. Chen *et al.*, "Physical and electrical characterization of metal–insulator–metal capacitors with Sm_2O_3 and Sm_2O_3/SiO_2 laminated dielectrics for analog circuit applications," *IEEE Trans. Electron Devices*, vol. 56, no. 11, pp. 2683–2691, Nov. 2009.
[7] S. D. Park *et al.*, "Bulk and interface effects on voltage linearity of ZrO_2–SiO_2 multilayered metal-insulator-metal capacitors for analog mixed-signal applications," *Appl. Phys. Lett.*, vol. 95, no. 2, p. 022905, 2009.
[8] S.-J. Ding *et al.*, "Metal-insulator-metal capacitors using atomic-layer-deposited $Al_2O_3/HfO_2/Al_2O_3$ sandwiched dielectrics for wireless communications," *J. Vac. Sci. Technol. B*, vol. 24, no. 6, pp. 2518–2522, Nov. 2006.
[9] J. Schmitz *et al.*, "RF capacitance-voltage characterization of MOSFETs with high leakage dielectrics," *IEEE Electron Device Lett.*, vol. 24, no. 1, pp. 37–39, Jan. 2003.
[10] (2012). *The International Technology Roadmap for Semiconductors*. [Online]. Available: http://www.itrs.net/
[11] T. H. Phung *et al.*, "High performance metal-insulator-metal capacitors with Er_2O_3 on ALD SiO_2 for RF applications," *J. Electrochem. Soc.*, vol. 158, no. 12, pp. H1289–H1292, 2011.
[12] I.-S. Park *et al.*, "Dielectric stacking effect of Al_2O_3 and HfO_2 in metal–insulator–metal capacitor," *IEEE Electron Device Lett.*, vol. 34, no. 1, pp. 120–122, Jan. 2013.
[13] C. Jorel *et al.*, "High performance metal-insulator-metal capacitor using a $SrTiO_3/ZrO_2$ bilayer," *Appl. Phys. Lett.*, vol. 94, no. 25, pp. 253502-1–253502-3, 2009.
[14] C.-C. Lin *et al.*, "MIM capacitors based on $ZrTiO_x/BaZr_yTi_{1-y}O_3$ featuring record-low VCC and excellent reliability," *IEEE Electron Device Lett.*, vol. 34, no. 11, pp. 1418–1420, Nov. 2013.