Diamond Metal–Semiconductor Field-Effect Transistor With Breakdown Voltage Over 1.5 kV

Hitoshi Umezawa, Takeshi Matsumoto, and Shin-Ichi Shikata

***Abstract*— A diamond metal–semiconductor field-effect transistor (MESFET) with a Pt Schottky gate was fabricated. The MESFET exhibited clear saturation and pinchoff characteristics. The drain current of the MESFET operated at 300 °C was 20 times higher than that at room temperature due to the activation of acceptors. The breakdown voltage was highly dependent on the gate–drain length and reached 1.5 kV at a gate–drain length of 30 μm, which is the highest reported for a diamond FET.**

***Index Terms*— Diamond, metal-semiconductor field-effect transistor, breakdown voltage.**

I. Introduction

DIAMOND semiconductors are a promising candidate for future electronics devices, due to their superior material properties such as a high breakdown field, high thermal conductivity, low dielectric constant and high bulk carrier mobility. Accordingly, the figures of merits for high-power and low-loss or high-power and high-frequency devices are extremely high [1]. Diamond-based diodes have been reported to realize high-current and low-loss capability [2]–[4], high temperature stability [5], fast switching with low switching losses [6], and high electrical field strength [7]. However, to utilize diamond for inverter/converter applications, not only diodes, but also high-power and high-temperature switching devices are required. Saito et al. have simulated low-loss and high-voltage characteristics for diamond that are better than those GaN or SiC, even though a planar structure was utilized [8]. To date, metal-insulator semiconductor (MIS) or metal-semiconductor (MES) field-effect transistors (FETs) on diamond using hydrogen-terminated surface channels [9]–[11], junction FETs (JFETs) [12], [13] have been reported; however, the breakdown voltages are limited to less than 700 V. In this letter, diamond MESFETs were fabricated by the adoption of a wide gate-drain length device structure and with a lightly doped p-type channel to realize high breakdown voltages.

II. Experimental

Figure 1 shows a top view and the cross-sectional structure of the diamond MESFET. Firstly, the p-type layer was deposited on a high-pressure and high-temperature synthetic Ib (001) semi-insulating single-crystal diamond substrate using microwave plasma assisted chemical vapor deposition (MWCVD). During growth, the methane concentration, plasma power, and chamber pressure were 4%, 3.9 kW and 120 Torr, respectively. In this letter, impurity boron was not introduced intentionally to prevent the degradation of the film quality and Schottky contact. The boron was unintentionally introduced as an order of $10^{15}/cm^3$ during the growth. The growth rate was 1.5 μm/h and the thickness of the deposited p-type layer was 3 μm. A Corbino (circular) type structure, which does not require device isolation, was utilized. Ti/Au ohmic contacts as source and drain electrodes were fabricated using photolithography and lift-off techniques. The surface of the film was exposed to ultraviolet (UV) light under an ozone atmosphere to obtain stable oxygen surface termination [14]. Pt/Au multilayers were fabricated as the Schottky gate. The source-gate length (L_{SG}) was fixed at 5 μm for all the devices fabricated. The gate length (L_G) and the gate-drain length (L_{GD}) were varied as 10 and 20 μm, and as 5, 10, 20, 30 μm, respectively.

The current-voltage (I-V) characteristics of the MESFETs were measured using a parameter analyzer (Agilent 4156C) and a vacuum probe system (Nagase Techno-Engineering) for high-temperature measurement. Breakdown measurements were conducted at room temperature using a power device analyzer (Agilent, B1505A) and a probe system (Vector Semiconductor) in an insulating liquid (3M, Fluorinert™) to prevent surface discharge.

III. Results and Discussion

Figure 2 shows the temperature dependence of the drain current (I_{DS}) and drain bias (V_{DS}) characteristics for a diamond MESFET with $L_G = 20$ μm and $L_{GD} = 30$ μm. The gate bias (V_{GS}) was varied from 0 to 30 V with a voltage step of 6 V. The MESFET shows normally-on characteristics, and the channel is perfectly pinched off at $V_{GS} = 30$ V both at room temperature and at 300 °C. The maximum I_{DS} and transconductance (g_m) are increased from −0.06 mA/mm and 9.7 μS/mm to −1.23 mA/mm and 61 μS/mm, respectively, by increasing the temperature. The specific on-resistance is estimated to be 1.4 kΩ-cm. The current capability is almost comparable to the JFETs ever reported [13] and lower than the MESFET on hydrogen-terminated surface channel [15]. The lower parasitic resistances at high temperature are mainly due to the activation of carriers from the acceptor level ($E_A = 0.36$eV) in the p-type epitaxial film and a decrease in ohmic contact resistance. In order to improve the current capability of the FET the decrease of gate length and parasitic resistances on source-gate spacing and ohmic contact resistances are required. The threshold voltage for the device was confirmed to be $V_{TH} = 27$ V from the

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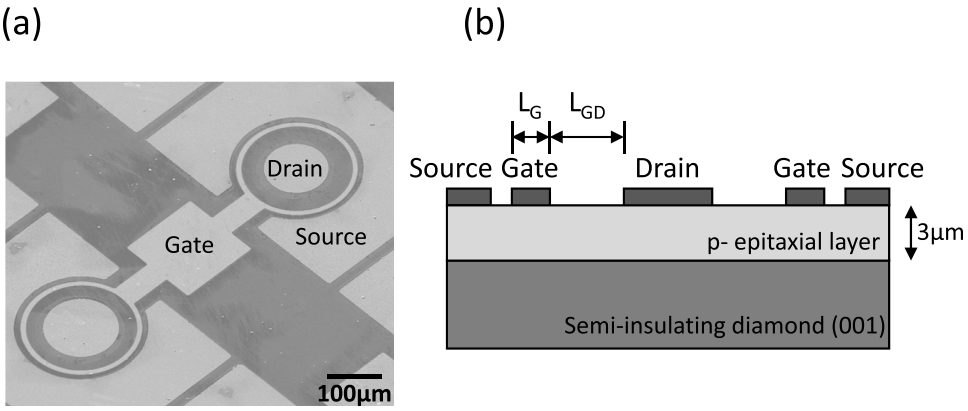

Fig. 1. (a) Top view and (b) cross sectional image of diamond MESFET with Corbino geometry.

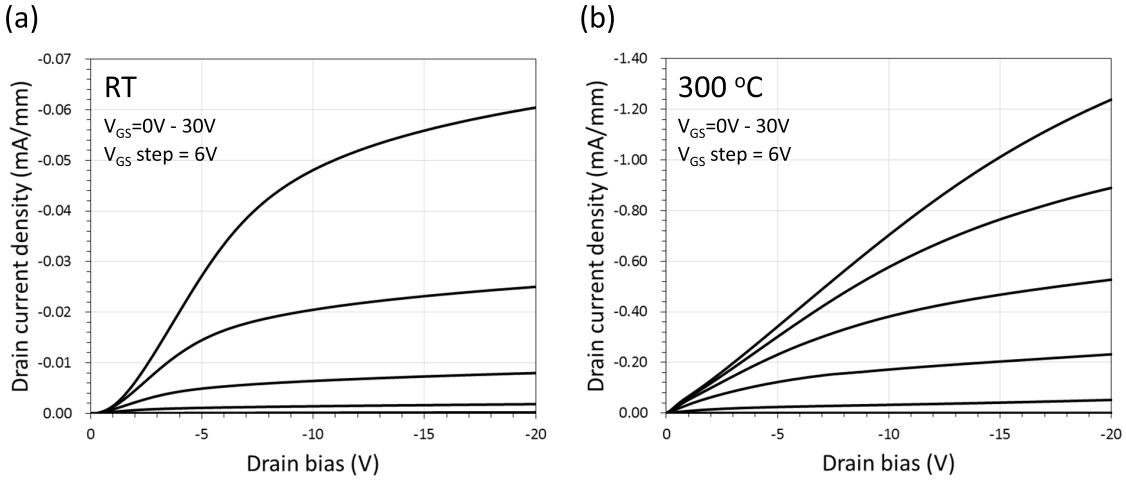

Fig. 2. I_{DS}-V_{DS} characteristics of the diamond MESFET measured at (a) room temperature and (b) 300 °C.

I_{DS}-V_{GS} characteristics. An on/off ratio greater than 7 orders of magnitude was obtained at room temperature, but decreased to 3 orders of magnitude at 300 °C, due to the increase of leakage current through the Schottky interface even though the reverse bias condition. The acceptor concentration (N_A-N_D) was estimated to be $4.7 \times 10^{15}/cm^3$, with considering the depletion of the channel due to the donors in semi-insulating substrate.

Figure 3 shows the breakdown characteristics of diamond MESFETs with $L_G = 20\ \mu m$ as a function of L_{GD}. To decrease the leakage current, a V_{GS} of 50 V was applied. The breakdown voltage of the MESFET was 693 V when L_{GD} was 5μm; however, this was improved to 744, 1218 and 1530 V by increasing L_{GD} to 10, 20 and 30 μm, respectively. The breakdown voltage of 1530 V is 2.5 times higher than that reported [13] and is the highest for a diamond FET reported to date. After the breakdown characterization, the breakdown voltage is degraded more than 30% due to the critical damage on the devices.

Based on the assumptions such as the voltage drop occurs only in the gate-drain spacing without considering field spikes at the drain edge of the gate electrode, the electrical field (E_{max}) and depleted length (wd) at the breakdown voltage can be estimated to be 2.15 MV/cm and 15 μm for $L_{GD} = 30\ \mu m$, and 1.93 MV/cm and 13.1 μm for $L_{GD} = 20\ \mu m$, which indicates that L_{GD} is longer than the depletion length. In contrast, the estimated depletion lengths at the breakdown voltages are longer than L_{GD} for the MESFETs

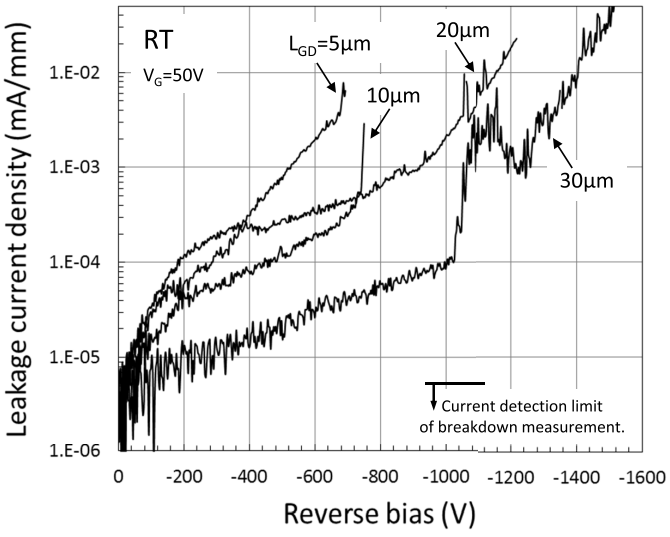

Fig. 3. Reverse characteristics of diamond MESFET with $L_{GD} = 5$, 10, 20 and 30 μm. The gate length of all the devices was 20 μm.

with $L_{GD} = 5$ and 10 μm. Accordingly, the punch-through type potential distribution is expected for these MESFETs. Emax is estimated to be 1.85 and 1.53 MV/cm for the MESFET devices with $L_{GD} = 5$ and 10 μm, respectively. The estimated E_{max} for all of the devices was higher than Si devices but 5-10 times lower than the ideal value for diamond. One of the reasons of this low E_{max} might be due to the field spikes

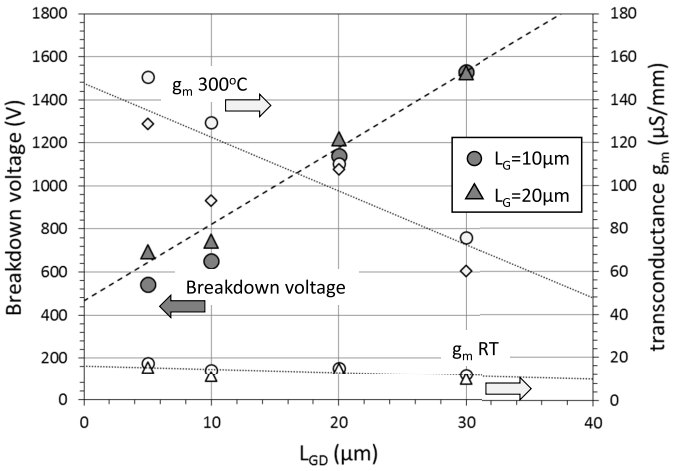

Fig. 4. Breakdown voltage and transconductance of diamond MESFETs as a function of gate-drain length (L_{GD}) for gate lengths of $L_G = 10$ and 20 μm. Transconductance was measured at both room temperature and 300 °C.

at the drain edge of the gate electrode. Field-plate structure are required to alleviate the field at the region.

Figure 4 shows a summary of breakdown voltages and g_m as a function of L_{GD} for $L_G = 10$ and 20 μm. Increasing L_{GD} is effective for improving the breakdown voltage for diamond MESFETs and the performance is almost comparable to GaN HEMT [16]. However, the breakdown voltage is not sensitive to L_G in this case. Similar to the breakdown voltages, a decrease of L_G is not so effective for improving g_m; however, g_m is improved by decreasing L_{GD}, especially at 300 °C. One of the reasons for this is the effect of high parasitic resistances on the gate-drain spacing and also the ohmic contact resistance. The effective g_m is generally decreased from the intrinsic transconductance (g_{mi}) when parasitic resistances such as the source resistance (R_S) and drain resistance (R_D) are present. g_{mi} can be estimated using the following equation [17]:

$$g_{mi} = \frac{g_m^0}{1 - (R_S + R_D) g_d \cdot (1 + R_S \cdot g_m^0)}$$
$$g_m^0 \equiv \frac{g_m}{1 - R_S \cdot g_m} \quad (1)$$

where g_d is the measured drain conductance. When g_d is negligible, R_D has not effect on g_{mi}; however, g_m is degraded by R_D when g_d is high. From the open channel measurement of all of the devices, the parasitic resistances of the device such as R_S and R_D including the ohmic contact resistances were analyzed. Here, the activation energy of p-diamond (0.36eV) and the barrier height of ohmic contact resistance (0.48eV) are considered. R_S and R_D for the device shown in figs. 2 were estimated to be 21 and 85 kΩ from the sheet resistance of the p-type layer (1.4 MΩ/sq) and the ohmic contact resistance. g_d was estimated to be 0.46 μS from the I_{DS}-V_{DS} slope at $V_{GS} = 0$ V and $V_{DS} = -20$ V. Accordingly, g_{mi} can be estimated to be 29 μS/mm at room temperature, which is 3 times higher than the measured g_m. Using the same analysis method, g_{mi} at 300 °C was estimated to be 143 μS/mm using the parameters of $R_S = 1.6$ kΩ, $R_D = 9.2$ kΩ and $g_d = 24$ μS. High g_d of the MESFET is mainly due to the high saturation point. I_{DS} is not fully saturated at $V_{DS} = -20$V even at V_{GS}-V_{TH} is −27V. To realize high current operation on the MESFET, only the multiple figure structure is required without thick epitaxial film.

IV. Conclusions

Diamond MESFETs with a Corbino geometry were fabricated. The MESFETs exhibited normally-on behavior with clear pinched-off characteristics at both room temperature and 300 °C. The estimated intrinsic transconductance at 300 °C was improved to 143 μS/mm, which was 4.9 times higher than that at room temperature, due to activation of acceptors. Improvement of the breakdown voltage was confirmed with increasing gate-drain length and the maximum breakdown voltage reached 1530 V when the gate-drain length was 30 μm. This value was obtained without field-relaxation structures and is the highest reported for a diamond FET to date.

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