# p-GaN Gate HEMTs on 6-Inch Sapphire by CMOS-Compatible Process: A Promising Game Changer for Power Electronics

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***Abstract*— The ≥ 650 V power electronics market penetration by GaN HEMTs on Si has been impeded by the GaN buffer. Recently, GaN-on-sapphire, a promising solution, attracts great attentions. In this work, p-GaN gate HEMTs are successfully manufactured on 6-inch sapphire by CMOS-compatible process in our pilot line. Device process modules of p-GaN selective etching, low-temperature Ohmic contact, and $Al_2O_3/SiO_2$ passivation have all be realized. The fabricated 16 $\mu$m–$L_{GD}$ devices with a simplified epitaxy and device structure, feature a low $R_{ON}$ of 14.8 Ω·mm, a high $V_{TH}$ of 2 V, and a high OFF-state breakdown voltage ($BV$) over 1360 V. Further, the nonuniformity of the $R_{ON}$ and $V_{TH}$ across the 6-inch whole wafer is well controlled. Devices also passed the preliminary reliability assessment of high temperature gate bias (HTGB) stress and high temperature reverse bias (HTRB) stress. The high-reliability, high-uniformity, and low-cost p-GaN gate HEMTs on 6-inch sapphire will probably be a strong driven force for the power electronics market in the near future.**

***Index Terms*— p-GaN gate HEMTs, 6-inch sapphire, CMOS-compatible process, reliability.**

## I. Introduction

GAN HEMTs have opened a new era for solid-state power electronics, which not only improve the energy conversion efficiency but also boost the system's power density [1], [2], [3], [4] [5], [6], [7]. Since 2023, GaN HEMTs are also adopted for other consumer applications such as Class D-Audio, e-tools, and home appliance [8]. Industrial and even vehicle applications are expected to be accelerated since 2024.

At present, the commercialized GaN HEMTS are mostly based on the large-diameter low-cost GaN-on-Si wafers [9], [10]. As two decades passed, other solutions, for instance, 6 and 8-inch sapphire [11], 8-inch SiC [12], 8-inch SOI [13], [14], and 8-inch QST [15] are gradually available. For these novel substrates, sapphire is the most promising game-changing candidate for many factors. Firstly, the substrate cost is limited. Secondly, the high mechanical strength of sapphire helps to fight against stress, avoid crack, so as to simplify the buffer design. The parasitic conductive channel at the AlN/Si interface is significantly suppressed at the AlN/sapphire interface, which enables GaN-on-sapphire to have a much higher lateral blocking capability [16]. Thirdly, they can be manufactured by the existing silicon fabrication facilities.

Moreover, Transphorm has reported the work of 1200 V d-mode GaN switches on sapphire for a 900:450V buck converter [17], [18]. Later, e-mode p-GaN gate HEMTs on sapphire substrate with a high breakdown voltage $V_{BD}$ of 1.4 kV was demonstrated [19]. We have recently shown the 1700 V d-mode GaN HEMTs on sapphire with a 1.5 $\mu$m ultra-thin buffer [16]. Notably, study on the p-GaN gate HEMTs on sapphire is still in its infancy. To verify the possibility for commercialization, various difficulties must be overcome first, for instance, the uniformity and manufacturability of the GaN-on-sapphire epitaxy wafer, the applicability of the existing mass production tools, the portability of the CMOS-compatible process dedicated for GaN-on-Si, the reliability of the fabricated devices, etc.

In this work, the feasibility of fabricating low-cost p-GaN gate HEMTs on 6-inch sapphire for next-generation GaN technique will be comprehensively explored. The epitaxy and CMOS-compatible process in our pilot line will be first introduced. Then, electrical characterization will focus on checking the performance and yield, as well as dynamic $R_{ON}$ and p-GaN gate robustness. Finally, preliminary reliability of high temperature gate bias (HTGB) and high temperature reverse bias test (HTRB) stress will be evaluated in details.

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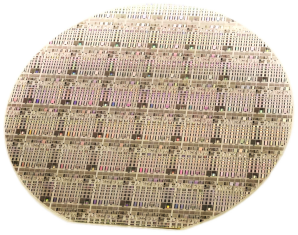

Fig. 1. Photograph of the 6-inch GaN-on-sapphire wafer manufactured by CMOS-compatible process.

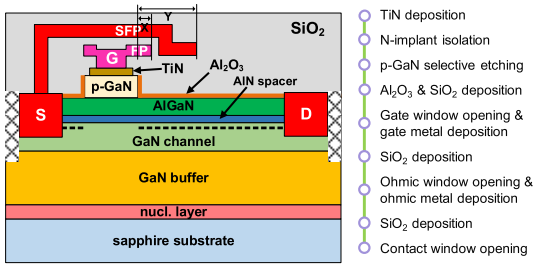


Fig. 2. Cross-sectional schematic and process flow of the p-GaN gate HEMTs on the 6-inch sapphire. [X, Y] denotes the field plate structure.

## II. Epitaxy and Fabrication

The HEMT structure was epitaxially grown on 6-inch sapphire using a Metal Organic Chemical Vapor Deposition (MOCVD) system, as illustrated in Fig. 1. The epitaxial stack consists of a 25 nm AlGaN nucleation layer, a 1.5 $\mu$m ultra-thin GaN buffer layer, a 250 nm GaN channel layer, a 0.5 nm AlN spacer layer, a 15 nm $Al_{0.2}Ga_{0.8}N$ barrier layer, and an 80 nm Mg-doped p-GaN layer with a doping concentration of $4 \times 10^{19}$ cm$^{-3}$, which is depicted in Fig. 2.

As shown in Fig. 2, the CMOS-compatible process in our pilot line starts with the deposition of a 40 nm TiN layer on the p-GaN surface, followed by device isolation through nitrogen implantation [20]. Then, high-selectivity $Cl_2/BCl_3/SF_6$-mixed gas plasma etching of p-GaN was carried out, where a surface root mean square (RMS) roughness of 0.35 nm was achieved, measured by atomic force microscope (AFM). A thin $Al_2O_3$ passivation layer was deposited and a 260 nm $SiO_2$ was deposited using plasma enhanced chemical vapor deposition (PECVD), followed by gate window opening through reactive ion etching (RIE), gate metal TiN/Ti/Al/TiN (40/20/250/30 nm) deposition by physical vapor deposition (PVD) and patterning by inductively coupled plasma (ICP) etching, as shown by the scanning electron microscope (SEM) images in Fig. 3. Further steps include the deposition of a 260 nm $SiO_2$ layer, Ohmic contact window opening, and deposition of Ohmic metal stack Ti/Al (10/200 nm) and rapid thermal annealing at 565 °C for 90 seconds in $N_2$. Finally, a 300 nm $SiO_2$ layer was deposited. The fabricated devices have a gate length $L_G$ of 4 $\mu$m, gate-source distance of 1.5 $\mu$m, and various gate-drain distance from 6 to 30 $\mu$m.

## III. Results and Discussion

In Fig. 4(a) and (b), the output and transfer characteristics of the 650 V HEMTs with $L_{GD}$ of 16 $\mu$m prepared on the 6-inch wafer are presented, where the on-state resistance $R_{ON}$ and threshold voltage $V_{TH}$ reach 14.8 Ω·mm and 2 V, respectively. The current droop in the saturation region of the $I_D$-$V_D$ curves

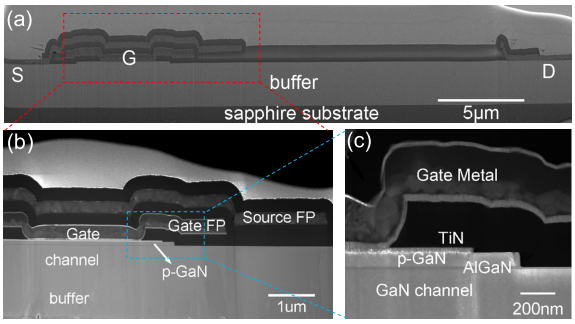


Fig. 3. SEM images of (a) the p-GaN gate HEMT, (b) the gate region, and (c) the p-GaN region on 6-inch sapphire.

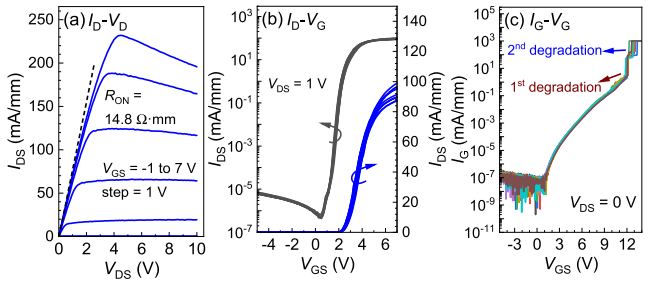


Fig. 4. (a) Output, (b) transfer, and (c) gate forward-bias leakage characteristics of the p-GaN gate HEMTs with $L_{GD}$ of 16 $\mu$m on the 6-inch sapphire.

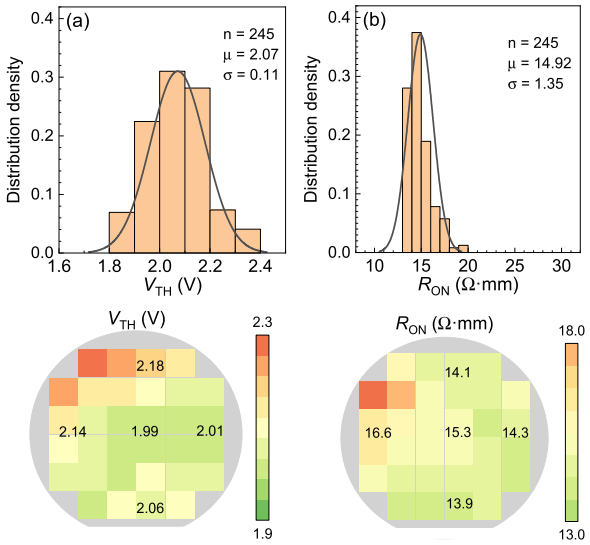


Fig. 5. The statistical distribution and electrical mapping of (a) $V_{TH}$ and (b) RON of 245 devices with $L_{GD}$ = 16 $\mu$m across the 6-inch wafer.

is possibly stemming from trapping effect [21] and self-heating effect [22]. Fig. 4(c) demonstrates the gate forward-bias $BV$ exceeds 12 V, thanks to the TiN retraction process as shown in Fig. 3(c) [23]. The 1st degradation is probably the breakdown of the metal/p-GaN Schottky contact, and the 2nd degradation is probably the p-GaN/AlGaN/GaN PiN junction failure [24], [25].

In Fig. 5, the statistical distribution and electrical mapping of $V_{TH}$ and $R_{ON}$ of the 245 HEMTs across the 6-inch whole wafer are demonstrated. The $V_{TH}$ is concentrated in the range of 2.0 to 2.2 V, and the $R_{ON}$ is predominantly between 14.0 to 16.0 Ω·mm. The statistical results prove the possibility of producing HEMTs on large-scale sapphire.

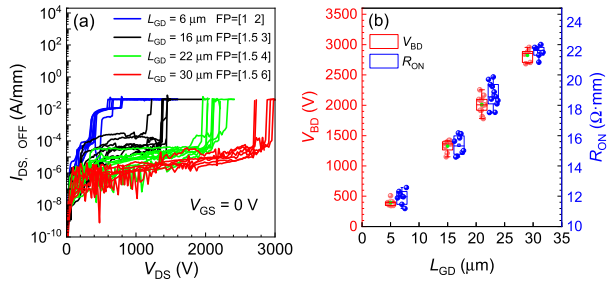


Fig. 6. (a) OFF-state breakdown characteristics and (b) the statistical distribution of $V_{BD}$ and $R_{ON}$ versus $L_{GD}$.

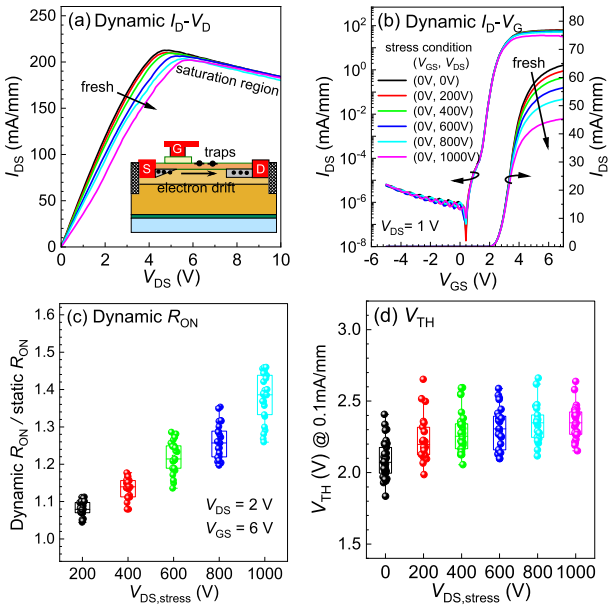


Fig. 7. (a) $I_D$-$V_D$ and (b) $I_D$-$V_G$ curves of p-GaN gate HEMTs on sapphire with $L_{GD}$ of 16 $\mu$m after various OFF-state stress, and the corresponding (c) dynamic RON and (d) $V_{TH}$ versus the stress voltages.

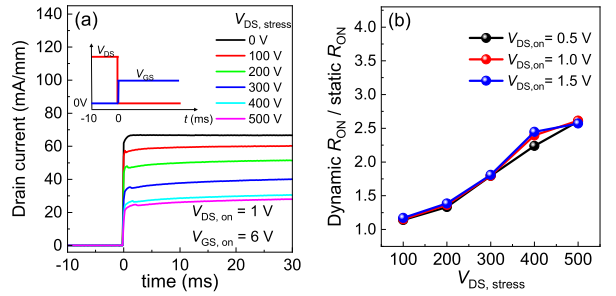


Fig. 8. (a) Transient current curves and (b) dynamic $R_{ON}$ after high-voltage pulse stress by Keysight N1267.

Fig. 6(a) illustrates the breakdown characteristics of HEMTs on sapphire. As shown in Fig. 6(b), the OFF-state $V_{BD}$ and $R_{ON}$ both linearly depends on the $L_{GD}$. In our design, 30 $\mu$m-$L_{GD}$ HEMTs with a simple device structure exhibit an OFF-state $V_{BD}$ of up to 2.9 kV, which demonstrates the potential of GaN-on-sapphire for future 1200 V applications.

Next, to evaluate the dynamic performance of the devices with the advanced $Al_2O_3/SiO_2$ passivation, high-voltage OFF-state stress was applied to the p-GaN gate HEMTs with $L_{GD}$ of 16 $\mu$m. During the measurements, the devices were first stressed for one second in OFF-state. Afterwards, their output

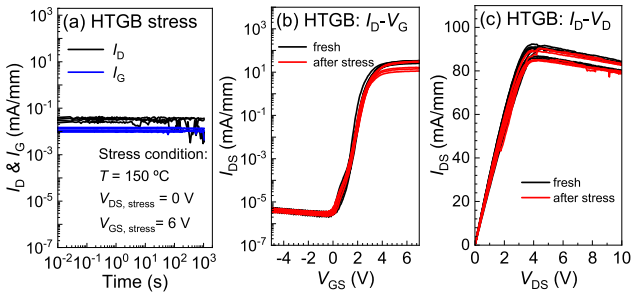


Fig. 9. (a) Gate and drain leakages during the HTGB stress where the temperature is 150 °C and VGS, stress is 6 V, and (b) $I_D$-$V_G$ and (c) $I_D$-$V_G$ curves before and after the 1-ks HTGB stress.

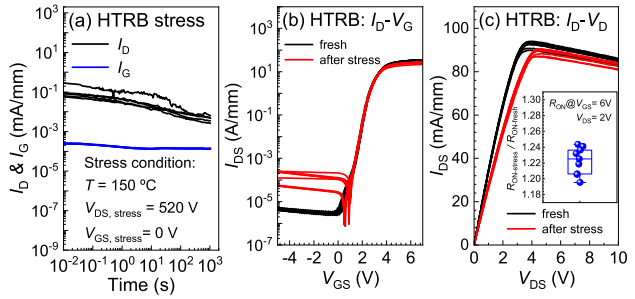


Fig. 10. (a) Gate and drain leakages during the HTRB stress where the temperature is 150 °C and $V_{DS}$, stress is 520 V, and (b) $I_D$-$V_G$ and (c) $I_D$-$V_G$ curves before and after the 1-ks HTRB stress.

and transfer curves were recorded. Fig. 7(a) and (b) both indicate the trapping effect mainly takes place in the gate-to-drain access region. It can be observed that the current collapse does not exist in the saturation region. This is because in the saturation region, the channel is partially pinch-off, as illustrated by the inset of Fig. 7(a), in which case the drifting electrons can hardly be impacted by the charged traps [26]. The boxplots of dynamic $R_{ON}$ and $V_{TH}$ after OFF-state stress are plotted in Fig. 7(c) and (d), respectively. Moreover, current collapse was further assessed by high-voltage pulse stress by Keysight N1267 as shown in Fig. 8, where the overlap time between the $V_{DS}$ falling and $V_{GS}$ rising is about 1.6 $\mu$s.

Furthermore, preliminary long-term reliability was assessed at 150 °C. 1-ks HTGB and HTRB stresses were conducted. During the stress, the gate and drain leakages were monitored. As shown in Fig. 9 and 10, the $V_{TH}$ keeps reliable without significant degradation. A slight current collapse takes place after HTRB stress, consistent with the dynamic $R_{ON}$ in Fig. 7.

## IV. Conclusion

p-GaN gate HEMTs on 6-inch sapphire have been successfully fabricated by CMOS-compatible process in our pilot line. The critical process modules of p-GaN selective etching, $Al_2O_3/SiO_2$ passivation, low-temperature Ohmic contact, and power metal deposition have been fully transferred to the platform of sapphire substrate. The high-uniformity and high-reliability of the fabricated HEMTs, combining the low-cost thin-film epitaxy and extremely simplified device structure and processing flow, make GaN-on-sapphire a promising game-changing technique for the future power electronics market.

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