Realization of a Complementary Full Adder Based on Reconfigurable Transistors

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***Abstract*— Fine grain reconfigurability carried out at the transistor level, i.e. the ability to switch between n- and p-type operation, offers new possibilities for highly efficient logic gates. In particular, XOR- and Majority gate circuit implementations can considerably benefit from reconfigurable transistors, as they require less than half of the transistor count needed in conventional static CMOS technology. Using a total of eight highly on-state symmetric reconfigurable field effect transistors fabricated from monolithic Al-Si heterostructures, we experimentally demonstrate a fully functional full adder, a fundamental circuit for many arithmetic applications. The two slightly adapted reconfigurable XOR gates for sum and carry output provide a full output voltage swing using only a single symmetric supply rail, while achieving very low static power consumption due to complementary circuit design and inherent leakage suppression of the devices. Furthermore, their stable operation against input voltage variations is demonstrated with static and transient measurements.**

***Index Terms*— Full adder, reconfigurable transistor, RFET, silicon on insulator, XOR.**

I. Introduction

EXCLUSIVE-OR (XOR) and Majority (MAJ) logic functions are highly relevant for the realization of arithmetic operations, but their direct implementation with conventional CMOS technology is intricate and demands considerable physical interconnect resources due to the significant number of transistors needed for their synthesis [1]. In this respect, reconfigurable field effect transistors (RFETs) are a promising concept for increasing efficiency in integrated circuits. These doping free, multi-gate transistors are capable of switching between n- and p-type operation during runtime by tuning the charge carrier injection through a gated Schottky junction using a program gate (PG) and one or several channel barriers with a control gate (CG) [2], [3], [4]. This reconfigurability on a transistor level offers high potential for novel, highly efficient logic gates to enhance performance and extend the capabilities of classic CMOS technology [5], [6], [7], [8]. Simulations utilizing this fine-grain reconfigurability on advanced System-on-Chip (SoC) or FPGA architectures predict significant enhancements in path delays, power consumption and even chip area [9], [10], [11]. In particular, RFETs provide intrinsic XOR and MAJ gates with less than half the transistors required in conventional CMOS [12], [13]. Recently, targeting XOR and MAJ logic gate optimizations, Gauchi et. al [14] demonstrated performance improvements on large scale integrated circuits comparing 10 nm RFET with 12 nm FinFET technology.

In this work, we experimentally demonstrate the first complementary 1-bit full adder using only 8 physically identical RFETs, excluding inverters for providing the inverted input signals. These RFETs are based on monolithic Al-Si heterostructures embedded in a three independent top-gated Schottky barrier field effect transistor (SBFET) architecture, exhibiting highly symmetric on-states [15], [16], which is essential for efficiently working logic circuits [2], [17]. Based on a 3-input XOR and MAJ gate with 4 RFETs each, the logic outputs for sum and carry are calculated, as demonstrated with both static and transient measurements.

II. Experimental Results

A. Symmetric On-State Si RFET

For the fabrication of the RFETs, ~300 nm wide nanosheets were patterned from a Si on insulator (SOI) substrate with a 20 nm thick, lightly p-doped (B, $\sim 10^{15}\,cm^{-3}$) device layer on top of 100 nm thick BOX using laser lithography and reactive ion etching. After forming the 10.3 nm thick thermal SiO_2 gate oxide, the Al source/drain (S/D) contacts are defined with laser lithography, followed by a BHF dip, Al sputter deposition and lift-off. Rapid thermal annealing (RTA) at 773 K in forming gas atmosphere is then used to induce lateral intrusion of Al into the nanosheets by an Al-Si exchange reaction, forming shortened Si channels (~2.5 µm) with flat and highly reproducible Al-Si Schottky junctions that exhibit an abruptness down to the atomic level [18]. The Ti top gates with Au bond pads are then structured using electron beam lithography, evaporation and lift-off techniques, with the PG aligned directly atop both Al-Si interfaces, and the CG in between on top of the Si channel, as can be seen in the false-color scanning electron microscopy (SEM) image in Fig. 1a. The single RFET device characteristic is plotted

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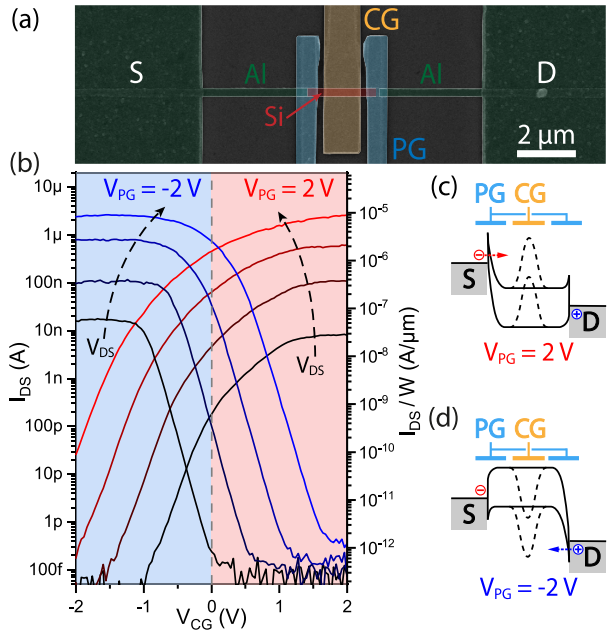
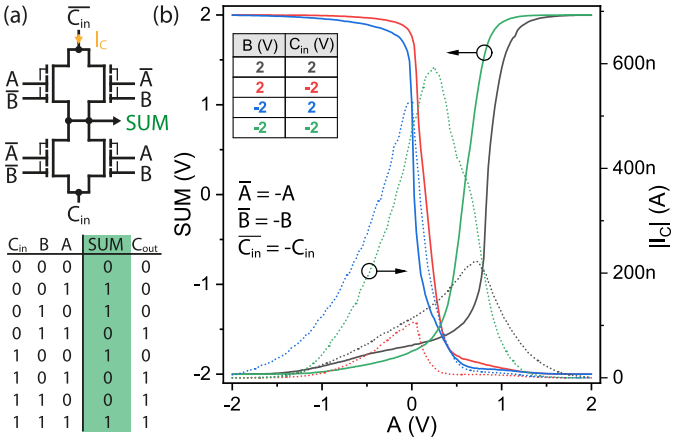


Fig. 1. (a) False-color SEM image of a single Al-Si RFET. (b) Transfer characteristic of the RFET showing symmetric n- and p-type operation at $V_{PG} = 2$ V and -2 V, with V_{DS} increased from 1 V to 4 V in 1 V steps ($V_D = -V_S$). (c,d) Schematic illustration of the energy band landscape for both operation modes.



C_{in}	B	A	SUM	C_{out}
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

Fig. 2. (a) Schematic for the sum operation based on four RFETs and the corresponding truth table. (b) Voltage transfer characteristic for A increased from -2 V to 2 V for all constant logic inputs values B and C_{in}. The dotted lines indicate the current flow $|I_C|$ through the circuit.

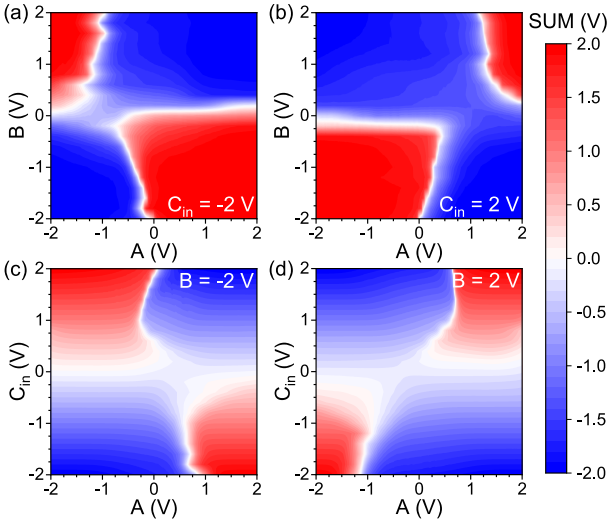


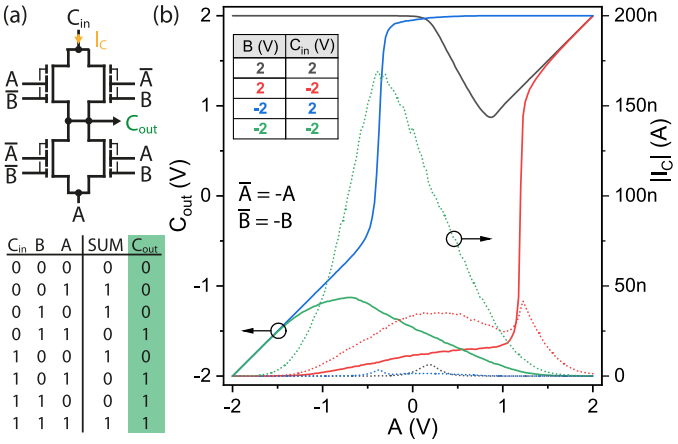
Fig. 3. Output color maps for the sum operation, with two inputs varied between ±2 V and C_{in} (a,b) and B (c,d) fixed at constant values, respectively.

in Fig. 1b for various bias voltages V_{DS}. High symmetry is achieved in terms of on-currents (8.84 µA/µm, 9.02 µA/µm), threshold voltages (−0.2 V, 0.33 V) and subthreshold slopes (217 mV/dec, 203 mV/dec) at $V_{DS} = 4$ V for n- ($V_{PG} = 2$ V) and p-mode ($V_{PG} = -2$ V), respectively, the latter two mainly attributed to the inherent mid-gap pinning Al-Si Schottky junctions [18]. All those parameters can potentially be improved by device scaling down to low nm dimensions [19], introduction of high-κ gate dielectrics or a Ge rich channel for a reduced bandgap [4], [20]. Importantly, the devices are bidirectional, i.e. for positive and negative V_{DS}, their IV characteristic does not change in absolute value. Combined with their ability to switch polarity between n- and p-mode at runtime, efficient logic gates can be built.

B. XOR Based Full Adder

A full-swing static XOR gate can be realized with only four RFETs as proposed by [3] and [5], reducing the transistor count by half vs. conventional CMOS technology. The input signals A and B, and their inverted counterparts $\bar{A}$, $\bar{B}$ are applied to the CGs and PGs. Adapted to a transmission gate architecture, an additional input signal, the carry input (C_{in}), can be used to switch the polarity of the circuit, and thus between XOR and XNOR, to obtain a 3-input XOR gate for the sum functionality, which is depicted in Fig. 2a. Note that additional gates needed to drive the transmission gates are neglected, which may result in additional overhead depending on the application targeted and whether the circuits are realized as a combination of CMOS and transmission gates or in a full transmission logic setup. The measured voltage transfer characteristic for this logic gate is shown in Fig. 2b, with the inputs B and C_{in} fixed at constant logic levels ($V_{dd} = 2$ V for "1", $V_{ss} = -2$ V for "0"), and A swept from -2 V to 2 V. A full-swing operation is achieved, and the cross current flow I_C through the circuit is well suppressed (< 6 nA) at the distinct output states, peaking at the state transitions with short-circuit currents up to 170 nA. The suppression of the steady state currents, with higher current peaks at the state transitions, is characteristic for complementary circuit designs, also when using conventional CMOS technology. Remarkably, this is achieved using only the two fully symmetric operation voltage levels of ±2 V, simplifying the circuit layout. To demonstrate the stability of the RFET based logic gate against input voltage variations, output color maps are plotted in Fig. 3. While for constant C_{in} in (a,b) the SUM output switches rapidly between ±2 V, the state transitions when varying C_{in} (c,d) are more blurred, as the supply voltage for the circuit also changes. Nevertheless, stable operating windows for all states of at least 0.6 V are visible when varying the input levels before the output is flipped.

For full adder functionality, the carry bit also needs to be calculated. Therefore, the same reconfigurable XOR gate can be used, where only the signals defining the polarity



C_{in}	B	A	SUM	C_{out}
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

Fig. 4. (a) Schematic for the carry output C_{out} with the corresponding truth table. (b) Voltage transfer characteristic for A increased from −2 V to 2 V for all inputs states B and C_{in}. The current $|I_C|$ through the circuit is shown by the dotted lines.

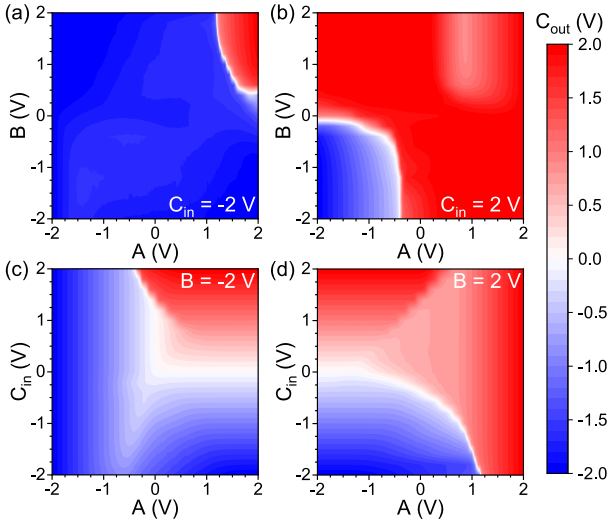


Fig. 5. Output color map for the carry operation, for constant values for C_{in} in (a,b) and B in (c,d) while the other two inputs are varied between ±2 V.

of the circuit, $\overline{C_{in}}$ and C_{in}, are exchanged by C_{in} and A, as shown in the schematic in Fig. 4a, resembling a 3-input MAJ gate. Since A and C_{in} also modulate the supply rail voltages of the circuit, the output C_{out} is changed linearly before switching state when sweeping A from −2 V to 2 V in Fig. 4b, leading to less sharp transitions vs. the sum operation. This can also be seen in the output maps in Fig.5, also clearly showing stable operation regimes for all output states and therefore providing sufficient noise immunity. Remarkably, the complementary four RFET based design again provides low steady state currents of I_C <1.3 nA for low static power consumption, with short-circuit currents up to 170 nA.

The transient operation of the complete full adder based on the two reconfigurable XOR gates is shown in Fig. 6 for the complete input sequence, correctly calculating all output states for SUM and C_{out}. Due to the absence of a back-end-of-line interconnect technology, our lab-based structure design, with large planar contact pads on top of an SOI substrate for contacting the probes induces extremely high parasitic capacitances, limiting the operation speed. Especially when the polarity of the logic gate is inverted with C_{in}

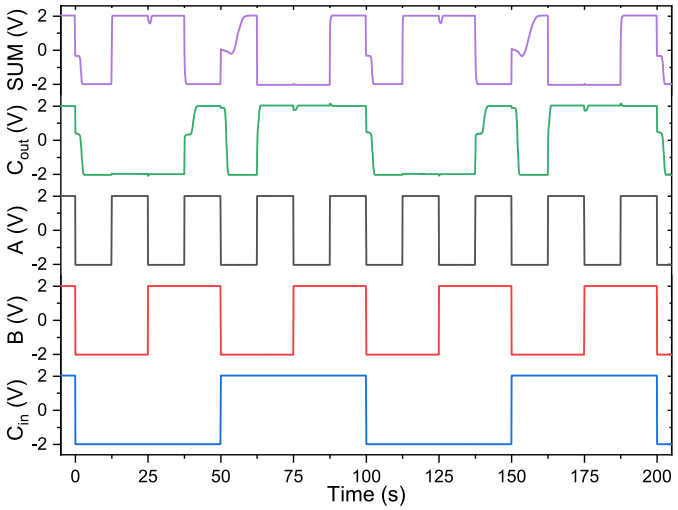


Fig. 6. Time dependent logic operation of the full adder showing the output signals SUM and C_{out} in response to the input signals A, B and C_{in}.

or A, the transitions at the outputs are rather slow due to charge RC delays and capacitive coupling, resulting in logic degradation. However, Amaru et. al [12] used HSPICE circuit simulations of the proposed 1-bit full adder design based on a 22 nm technology node to estimate that switching speeds in the GHz region are feasible, even up to 3.8x faster than their conventional CMOS counterparts given the reduced propagation delay. More recently, Quijada et. al [21] showed simulations using Ge RFETs, further improving the full-adder performance. In addition, Cadareanu et. al [22] calculated a reduction in the energy-delay product of 18 % due to the reduced number of transistors, despite a slight increase in parasitic capacities from the additional gates.

III. Conclusion

In this letter, we report on a 1-bit full adder based on a XOR and MAJ gate, each realized with only four ambipolar RFETs based on Al-Si-Al heterostructures, benefiting from their high on-state symmetry. With only slightly different circuitry, both 3-input XOR for SUM and MAJ for C_{out} operations have been implemented, which can operate reliably and with low static power consumption as a result of their complementary architecture. Compared to conventional CMOS topologies, this RFET based implementation reduces the number of transistors by more than a half. By applying scaling measures and modern interconnect technologies, propagation delays and power consumption can potentially be reduced.

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