Stable High Temperature Operation of p-GaN Gate HEMT With Etch-Stop Layer

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***Abstract*— High-temperature operation of the p-GaN gate high-electron-mobility transistor (HEMT) was investigated, specifically up to 500 °C. The p-GaN gate HEMT demonstrated stable behavior with normally-off operation, steep increase of drain current in the subthreshold region, and suppressed off-state current. By adding Al_2O_3 etch-stop layer, the device showed significant reduction in subthreshold swing when measured at 500 °C, effectively mitigating hysteresis in the transfer characteristics. Additionally, the lifetime of the gate stack with the etch-stop layer was estimated to be much longer than that of the stack without the etch-stop layer. Through the integration of the depletion-mode (D-mode) metal-insulator-semiconductor HEMT (MIS-HEMT) device with the p-GaN gate device, a direct-coupled field-effect transistor logic (DCFL) inverter was fabricated. This inverter showed stable logic operation up to 500 °C, featuring rail-to-rail operation and large gain. A long-term reliability test conducted at 500 °C for 100 hours revealed stabilized on-state and off-state values after about 50 hours of operation.**

***Index Terms*— GaN, HEMT, p-GaN, high temperature, enhancement-mode, depletion-mode, direct-coupled FET logic, inverter, reliability.**

I. Introduction

HIGH temperature electronics have gained significant attention across industries, including aerospace, automotive, and energy production [1], [2], [3]. Challenges faced by conventional electronics under high temperature conditions, such as increased leakage current and poor stability, have prompted extensive research into wide bandgap materials [3], [4], [5]. Among these materials, GaN has demonstrated significant promise due to many advantages, including large bandgap, high breakdown field, excellent thermal stability, and high saturation velocity [3], [4], [5], [6].

AlGaN/GaN Schottky HEMTs have been tested for high temperature electronics, but gate metal diffusion into the barrier layer and large gate leakage severely degraded device characteristics at high temperatures [7], [8]. MIS-HEMT devices, with gate dielectric layer between the gate metal and AlGaN barrier, showed potential for reducing gate leakage current and improving gate stack stability. However, achieving stable high temperature operation with MIS-HEMT structures has been challenging due to threshold voltage instability caused by AlGaN strain relaxation and interface traps [8], [9], [10], [11], [12], [13], [14]. Most studies have focused on operation up to 200 °C, whereas industry applications often require higher temperatures [10], [11], [12], [13]. Furthermore, there is limited research on normally-off high temperature HEMTs, which are more practical and versatile for real-world applications.

In this study, we demonstrated stable high temperature operation of the p-GaN gate HEMT up to 500 °C. By incorporating etch-stop layer, the p-GaN interface was effectively protected from dry etching induced damage, resulting in longer gate stack lifetime and reduced hysteresis. The device showed stable normally-off operation for 100 hours without significant degradation or breakdown at 500 °C. Furthermore, we tested the operation of DCFL inverter utilizing the p-GaN gate HEMT up to 500 °C, demonstrating the feasibility of high temperature logic operation.

II. Device Fabrication

The p-GaN gate HEMT device was fabricated on the p-GaN/AlGaN/GaN heterostructure grown on silicon substrate. The substrate consists of 70 nm p-GaN, 15 nm $Al_{0.2}Ga_{0.8}N$, 0.7 nm AlN, 200 nm unintentionally doped GaN, 5.8 μm GaN buffer, and silicon substrate from top to bottom. The schematic of the device is shown in Fig. 1(a), and the top-view scanning electron microscopy (SEM) image of the fabricated device is shown in Fig. 1(b). The length of gate electrode/p-GaN contact area was 1.5 μm, and the width was designed to be slightly smaller than the width of the mesa-isolated AlGaN/GaN block to prevent the electrodes from directly contacting the sidewall, which may have dry etching induced damage. The fabrication process is shown in Fig. 1(c). The p-GaN layer on top of the substrate was removed, and mesa isolation was carried out by dry etching performed using inductively coupled plasma reactive ion etching (ICP-RIE) with Cl_2 and BCl_3. Ti/Al/Ni/Au (20 nm/120 nm/60 nm/ 50 nm) stack was then deposited as the source/drain electrode using e-beam evaporator, followed by rapid thermal annealing at 900 °C for 30 seconds in N_2 to form the ohmic contact. 10 nm of Al_2O_3 etch-stop layer was deposited using atomic layer deposition (ALD), and 200 nm of Si_3N_4 layer was deposited using plasma-enhanced chemical vapor deposition (PECVD). Gate stack and source/drain contact windows were opened by ICP-RIE using SF_6, and the ALD Al_2O_3 etch-stop layer was removed by wet etching using buffered oxide etch (BOE). Ni/Au (50 nm/150 nm) layer was

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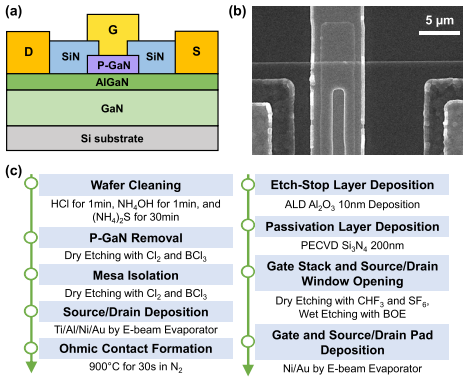

Fig. 1. (a) Schematic of a p-GaN gate HEMT. (b) SEM image of the p-GaN gate HEMT device. ($L_G = 4\ \mu m$, $L_{GS} = 4\ \mu m$, $L_{GD} = 9\ \mu m$, $W = 100\ \mu m$) (c) Fabrication process of the p-GaN gate HEMT.

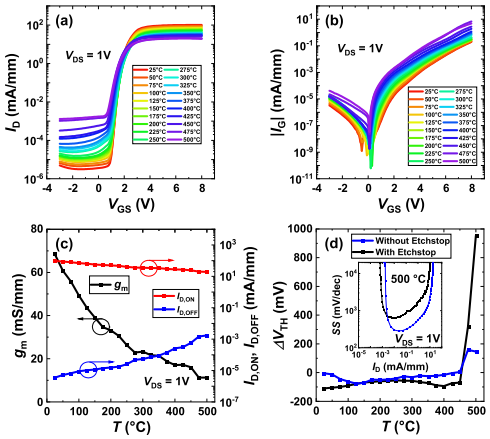

Fig. 2. (a) Transfer characteristic and (b) gate leakage current of a p-GaN gate HEMT with etch-stop layer at various temperatures up to 500 °C. (c) Temperature dependence of the peak transconductance (g_m), on-state current at $V_{GS} = 5$ V, and off-state current at $V_{GS} = 0$ V. (d) V_{TH} hysteresis (ΔV_{TH}) of the transfer curve with V_{GS} sweep range of -3 V $\sim$ 8 V measured at various temperatures for the p-GaN gate HEMT with and without the etch-stop layer. Here, V_{TH} hysteresis was extracted as $\Delta V_{TH} = V_{TH\text{-}F} - V_{TH\text{-}B}$ where $V_{TH\text{-}F}$ is the threshold voltage in the forward sweep and $V_{TH\text{-}B}$ is the threshold voltage in the backward sweep. Inset shows subthreshold swing (SS) of the p-GaN gate HEMT with and without the etch-stop layer at 500 °C.

deposited as the gate electrode using the e-beam evaporator, and post-metallization annealing was performed at 500 °C for 5 minutes in N_2.

III. Results and Discussion

Temperature dependence of the transfer characteristic and gate leakage current of p-GaN gate HEMT with etch-stop layer are shown in Fig. 2(a) and 2(b), respectively. For the high temperature measurements, the device was measured in vacuum environment, with contact made using probe tips. The gate voltage was increased and decreased in steps of 0.1 V, with time interval of approximately 0.2 seconds between each gate voltage value, and there was no delay introduced between the forward and backward sweeps. The device showed stable high temperature operation with suppressed off-state current and sharp subthreshold slope. Normally-off operation was maintained with slight threshold voltage shift towards the negative direction, from 1.4 V at 25 °C to 0.9 V at 500 °C, estimated by the gate bias at which the drain current is 10^{-2} mA/mm. The gate leakage current gradually increased with increasing temperature, but the gate stack demonstrated stable operation without breakdown, even with large gate bias of 8 V up to 500 °C. Fig. 2(c) shows temperature dependence of the on-state current, off-state current, and peak transconductance. As the temperature increases, the on-state current gradually decreased, off-state current gradually increased, and the transconductance decreased. As the temperature increases, the mobility of the channel formed at the AlGaN/GaN interface decreases primarily due to increased phonon scattering, leading to a decrease in the on-state current and transconductance [8], [14], [15], [16]. The off-state drain current can be attributed to the carrier hopping current flowing through the dry etching induced traps on the AlGaN and GaN surfaces, which can be further suppressed by optimizing the dry etching recipe [17], [18].

To investigate the effect of etch-stop layer, another batch of devices without the etch-stop layer was fabricated by depositing PECVD Si_3N_4 layer directly on the p-GaN layer and then etching it away by SF_6 ICP-RIE. The subthreshold swing measured at 500 °C and V_{TH} hysteresis of the transfer curve are shown in Fig. 2(d). The V_{TH} hysteresis (ΔV_{TH}) was extracted using the equation $\Delta V_{TH} = V_{TH-F} - V_{TH-B}$, where V_{TH-F} is the threshold voltage in the forward sweep and V_{TH-B} is the threshold voltage in the backward sweep. The device with etch-stop layer had more suppressed hysteresis, especially starting from 475 °C. The minimum subthreshold swing of the device with and without the etch-stop layer measured at 500 °C were 283 mV/dec and 619 mV/dec, respectively, indicating sharper increase of the drain current in the subthreshold region with the etch-stop layer. Since the ALD Al_2O_3 layer showed extremely low etch rate with SF_6 dry etching and could be easily removed using BOE, addition of this layer effectively prevented dry etching induced damage on the p-GaN layer. We believe that the reduction of hysteresis and subthreshold swing is attributed to the incorporation of etch-stop layer. Hole injection through the gate metal/p-GaN Schottky junction was suppressed by maintaining intact interface with fewer traps, especially at high temperatures and with large gate bias, which led to smaller hysteresis. Furthermore, gate controllability over the channel was enhanced by improving the uniformity of p-GaN layer under the gate, resulting in reduced subthreshold swing.

Lifetime of the device was estimated by applying the gate bias on the array of devices with $L_{GS} = L_{GD} = 4\ \mu m$ while source/drain electrodes were grounded. Weibull plots of the time to breakdown (t_{BD}) distribution and lifetime predictions for the devices are shown in Fig. 3(a) and 3(b), indicating lifetime of 10 years for the device without the etch-stop layer at $V_{GS} = 4.3$ V, and lifetime of 10 years for the device with the etch-stop layer at $V_{GS} = 5.9$ V. Therefore, the addition of the etch-stop layer, which serves to protect the p-GaN surface, significantly improves the lifetime of the gate stack, highlighting the importance of preserving the intact p-GaN interface.

High temperature operation of the DCFL inverter was thoroughly tested. The circuit diagram and schematic of the DCFL inverter are illustrated in Fig. 4(a) and 4(b), respectively. The enhancement-mode (E-mode) p-GaN gate HEMT device and D-mode MIS-HEMT device were integrated with channel width ratio of 100:1. For the D-mode device, the p-GaN layer was completely removed, and 20 nm ALD Al_2O_3 layer was used as the gate oxide. Temperature dependent transfer

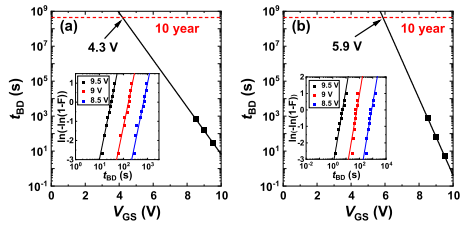

Fig. 3. Lifetime prediction of the gate stack (a) without etch-stop layer and (b) with etch-stop layer at the failure rate of 63.2 % at room temperature (25 °C). Inset of the figures illustrate Weibull plot of t_{BD} distribution for the gate stack at various stress voltages.

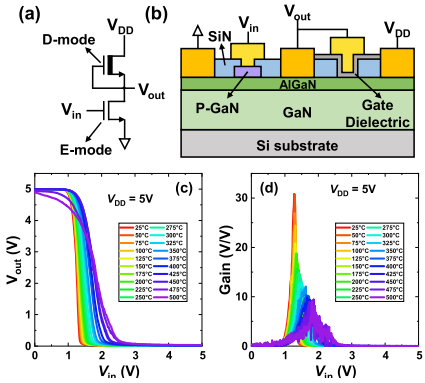

Fig. 4. (a) Circuit diagram and (b) device schematics of a DCFL inverter based on p-GaN gate E-mode HEMT and D-mode MIS-HEMT devices. (c) Transfer characteristics and (d) gain of the DCFL inverter measured at various temperatures.

characteristics and gain of the DCFL inverter are shown in Fig. 4(c) and 4(d), respectively. The transfer curve showed stable operation up to 500 °C, maintaining sharp transition region and consistent rail-to-rail operation with output voltage range from approximately 0 V to 5 V. This inverter demonstrated high gain that gradually decreased as the temperature increased, ranging from peak gain of 30.8 V/V at 25 °C to 9.1 V/V at 500 °C.

Long-term reliability was tested by measuring a p-GaN gate HEMT device with the etch-stop layer for 100 hours at 500 °C. Throughout the 100-hour testing at 500 °C, all terminals of the device were grounded between each I-V measurement sweep. The time-dependent transfer characteristics and gate leakage current are shown in Fig. 5(a) and 5(b), respectively. At 500 °C, the off-state current gradually increased, while the on-state current decreased. Additionally, the threshold voltage showed slight leftward shift, and the gate leakage current increased over time. These time-dependent degradations can be attributed to diffusion in the gate stack. Fig. 5(c) shows the on-state current, off-state current, and gate leakage current measured over time, all of which seem to stabilize after about 50 hours of operation.

The primary mechanism for the time-dependent degradation of the p-GaN gate HEMT has been reported to be the formation of a percolation path in the passivation dielectric near the p-GaN sidewall [19], [20], [21], [22]. In this study, the device was deliberately designed to have large gate metal retraction structure in both the vertical and lateral directions, aiming to enhance the lifetime of the device by reducing the sidewall leakage current. Additionally, for the p-GaN gate HEMT with etch-stop layer, the ALD Al_2O_3 layer serves as surface passivation, which has been reported to successfully suppress surface trapping and percolation path formation within the

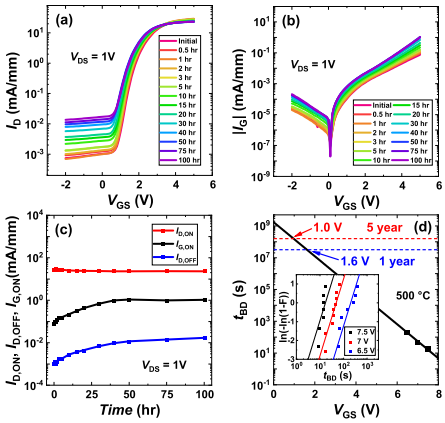

Fig. 5. (a) Transfer characteristic and (b) gate leakage current of a p-GaN gate HEMT measured for 100 hours with 500 °C thermal stress. (c) On-state current at V_{GS} = 5 V, off-state current at V_{GS} = 0 V, and gate leakage current at V_{GS} = 5 V measured for 100 hours at 500 °C. (d) Lifetime prediction of the gate stack with etch-stop layer at the failure rate of 63.2 % at 500 °C. Inset figure illustrates Weibull plot of t_{BD} distribution for the gate stack with etch-stop layer at various stress voltages.

passivation layer [21], [22], [23]. Moreover, impact ionization near the gate metal/p-GaN metal interface under forward gate bias is another contributing factor to the degradation of the p-GaN gate HEMT [24], [25], [26], [27]. We believe that the etch-stop layer preserves the intact p-GaN surface, thereby preventing early breakdown of the device caused by impact ionization. These degradations are expected to be further mitigated by the p-GaN surface reinforcement process, involving several treatments before the gate electrode deposition and the use of refractory metal for the gate [27], [28], [29], [30].

Lifetime estimation of the gate stack at 500 °C is illustrated in Fig. 5(d) with the Weibull plot of t_{BD} distribution. Based on these results, the lifetime of the gate stack at 500 °C with the failure rate of 63 % was estimated to be 5 years at V_{GS} = 1.0 V and 1 year at V_{GS} = 1.6 V. Considering that the threshold voltage was 0.9 V at 500 °C, these findings indicate that the p-GaN gate HEMT device has great potential as the high temperature logic device with reliable long-term operation.

IV. Conclusion

In summary, the p-GaN gate HEMT with the etch-stop layer demonstrated stable operation up to 500 °C, and long-term reliability was further confirmed by the consistent performance observed during 100 hours of device characterization at this temperature. By utilizing the etch-stop layer to preserve the intact p-GaN surface and avoiding direct contact of the gate electrode on the mesa sidewall, the device showed suppressed off-state current, steep subthreshold slope, and improved hysteresis. Additionally, long-term reliability test confirmed reasonably long device lifetime with appropriate supply voltage, and stable high temperature operation of the DCFL inverter was also examined. We believe that this p-GaN gate device with the etch-stop layer is a strong candidate for high temperature logic device, opening another path for development of high temperature electronics.

References

[1] P. G. Neudeck, R. S. Okojie, and L.-Y. Chen, "High-temperature electronics—A role for wide bandgap semiconductors?" *Proc. IEEE*, vol. 90, no. 6, pp. 1065–1076, Jun. 2002, doi: 10.1109/JPROC.2002.1021571.

[2] S. R. Eisner, H. S. Alpert, C. A. Chapin, A. S. Yalamarthy, P. F. Satterthwaite, A. Nasiri, S. Port, S. Ang, and D. G. Senesky, "Extended exposure of gallium nitride heterostructure devices to a simulated Venus environment," in *Proc. IEEE Aerosp. Conf.*, Mar. 2021, pp. 1–12, doi: 10.1109/AERO50100.2021.9438131.

[3] A. Hassan, Y. Savaria, and M. Sawan, "GaN integration technology, an ideal candidate for high-temperature applications: A review," *IEEE Access*, vol. 6, pp. 78790–78802, 2018, doi: 10.1109/ACCESS.2018.2885285.

[4] M. N. Yoder, "Wide bandgap semiconductor materials and devices," *IEEE Trans. Electron Devices*, vol. 43, no. 10, pp. 1633–1636, Oct. 1996, doi: 10.1109/16.536807.

[5] P. H. Carey, F. Ren, A. G. Baca, B. A. Klein, A. A. Allerman, A. M. Armstrong, E. A. Douglas, R. J. Kaplar, P. G. Kotula, and S. J. Pearton, "Extreme temperature operation of ultra-wide bandgap AlGaN high electron mobility transistors," *IEEE Trans. Semicond. Manuf.*, vol. 32, no. 4, pp. 473–477, Nov. 2019, doi: 10.1109/TSM.2019.2932074.

[6] K. H. Teo, Y. Zhang, N. Chowdhury, S. Rakheja, R. Ma, Q. Xie, E. Yagyu, K. Yamanaka, K. Li, and T. Palacios, "Emerging GaN technologies for power, RF, digital, and quantum computing applications: Recent advances and prospects," *J. Appl. Phys.*, vol. 130, no. 16, Oct. 2021, Art. no. 160902, doi: 10.1063/5.0061555.

[7] Y. Cai, Z. Cheng, Z. Yang, C. W. Tang, K. M. Lau, and K. J. Chen, "High-temperature operation of AlGaN/GaN HEMTs direct-coupled FET logic (DCFL) integrated circuits," *IEEE Electron Device Lett.*, vol. 28, no. 5, pp. 328–331, May 2007, doi: 10.1109/.LED.2007.895391.

[8] S. Kargarrazi, A. S. Yalamarthy, P. F. Satterthwaite, S. W. Blankenberg, C. Chapin, and D. G. Senesky, "Stable operation of AlGaN/GaN HEMTs for 25 h at 400 °C in air," *IEEE J. Electron Devices Soc.*, vol. 7, pp. 931–935, 2019, doi: 10.1109/JEDS.2019.2937008.

[9] D. J. Chen, K. X. Zhang, Y. Q. Tao, X. S. Wu, J. Xu, R. Zhang, Y. D. Zheng, and B. Shen, "Temperature-dependent strain relaxation of the AlGaN barrier in AlGaN/GaN heterostructures with and without Si_3N_4 surface passivation," *Appl. Phys. Lett.*, vol. 88, no. 10, Mar. 2006, Art. no. 102106, doi: 10.1063/1.2186369.

[10] M. Meneghini, I. Rossetto, D. Bisi, M. Ruzzarin, M. Van Hove, S. Stoffels, T.-L. Wu, D. Marcon, S. Decoutere, G. Meneghesso, and E. Zanoni, "Negative bias-induced threshold voltage instability in GaN-on-Si power HEMTs," *IEEE Electron Device Lett.*, vol. 37, no. 4, pp. 474–477, Apr. 2016, doi: 10.1109/LED.2016.2530693.

[11] H. Sun, M. Wang, J. Chen, P. Liu, W. Kuang, M. Liu, Y. Hao, and D. Chen, "Fabrication of high-uniformity and high-reliability Si_3N_4/AlGaN/GaN MIS-HEMTs with self-terminating dielectric etching process in a 150-mm Si foundry," *IEEE Trans. Electron Devices*, vol. 65, no. 11, pp. 4814–4819, Nov. 2018, doi: 10.1109/TED.2018.2869703.

[12] J. He, M. Hua, Z. Zhang, and K. J. Chen, "Performance and V_{TH} stability in E-mode GaN fully recessed MIS-FETs and partially recessed MIS-HEMTs with LPCVD-SiN_x/PECVD-SiN_x gate dielectric stack," *IEEE Trans. Electron Devices*, vol. 65, no. 8, pp. 3185–3191, Aug. 2018, doi: 10.1109/TED.2018.2850042.

[13] S. Yang, S. Liu, C. Liu, Z. Tang, Y. Lu, and K. J. Chen, "Thermally induced threshold voltage instability of III-nitride MIS-HEMTs and MOSC-HEMTs: Underlying mechanisms and optimization schemes," in *IEDM Tech. Dig.*, Dec. 2014, pp. 17.2.1–17.2.4, doi: 10.1109/IEDM.2014.7047069.

[14] A. J. Suria, A. S. Yalamarthy, H. So, and D. G. Senesky, "DC characteristics of ALD-grown Al_2O_3/AlGaN/GaN MIS-HEMTs and HEMTs at 600 °C in air," *Semicond. Sci. Technol.*, vol. 31, no. 11, Oct. 2016, Art. no. 115017, doi: 10.1088/0268-1242/31/11/115017.

[15] N. Maeda, K. Tsubaki, T. Saitoh, and N. Kobayashi, "High-temperature electron transport properties in AlGaN/GaN heterostructures," *Appl. Phys. Lett.*, vol. 79, no. 11, pp. 1634–1636, Sep. 2001, doi: 10.1063/1.1400779.

[16] Y. Q. Tao, D. J. Chen, Y. C. Kong, B. Shen, Z. L. Xie, P. Han, R. Zhang, and Y. D. Zheng, "High-temperature transport properties of 2DEG in AlGaN/GaN heterostructures," *J. Electron. Mater.*, vol. 35, no. 4, pp. 722–725, Apr. 2006, doi: 10.1007/s11664-006-0128-7.

[17] N. Xu, R. Hao, F. Chen, X. Zhang, H. Zhang, P. Zhang, X. Ding, L. Song, G. Yu, K. Cheng, Y. Cai, and B. Zhang, "Gate leakage mechanisms in normally off p-GaN/AlGaN/GaN high electron mobility transistors," *Appl. Phys. Lett.*, vol. 113, no. 15, Oct. 2018, Art. no. 152104, doi: 10.1063/1.5041343.

[18] J. Zhu, Y. Zhang, M. J. Uren, S. Liu, P. Wang, M. Mi, B. Hou, L. Yang, M. Kuball, X. Ma, and Y. Hao, "Variable range hopping mechanism and modeling of isolation leakage current in GaN-based high-electron-mobility transistors," *Appl. Phys. Lett.*, vol. 116, no. 22, Jun. 2020, Art. no. 222101, doi: 10.1063/5.0004957.

[19] S. Stoffels, B. Bakeroot, T. L. Wu, D. Marcon, N. E. Posthuma, S. Decoutere, A. N. Tallarico, and C. Fiegna, "Failure mode for p-GaN gates under forward gate stress with varying Mg concentration," in *Proc. IEEE Int. Rel. Phys. Symp. (IRPS)*, Apr. 2017, pp. 4B-4.1–4B-4.9, doi: 10.1109/IRPS.2017.7936310.

[20] S.-W. Tang, Z.-H. Huang, S.-C. Chen, W.-S. Lin, B. de Jaeger, D. Wellekens, M. Borga, B. Bakeroot, S. Decoutere, and T.-L. Wu, "High threshold voltage enhancement-mode regrown p-GaN gate HEMTs with a robust forward time-dependent gate breakdown stability," *IEEE Electron Device Lett.*, vol. 43, no. 10, pp. 1625–1628, Oct. 2022, doi: 10.1109/LED.2022.3198876.

[21] S. Stoffels, N. Posthuma, S. Decoutere, B. Bakeroot, A. N. Tallarico, E. Sangiorgi, C. Fiegna, J. Zheng, X. Ma, M. Borga, E. Fabris, M. Meneghini, E. Zanoni, G. Meneghesso, J. Priesol, and A. Šatka, "Perimeter driven transport in the p-GaN gate as a limiting factor for gate reliability," in *Proc. IEEE Int. Rel. Phys. Symp. (IRPS)*, Mar. 2019, pp. 1–10, doi: 10.1109/IRPS.2019.8720411.

[22] A. N. Tallarico, S. Stoffels, N. Posthuma, B. Bakeroot, S. Decoutere, E. Sangiorgi, and C. Fiegna, "Gate reliability of p-GaN HEMT with gate metal retraction," *IEEE Trans. Electron Devices*, vol. 66, no. 11, pp. 4829–4835, Nov. 2019, doi: 10.1109/TED.2019.2938598.

[23] N. E. Posthuma, S. You, S. Stoffels, H. Liang, M. Zhao, and S. Decoutere, "Gate architecture design for enhancement mode p-GaN gate HEMTs for 200 and 650 V applications," in *Proc. IEEE 30th Int. Symp. Power Semiconductor Devices ICs (ISPSD)*, May 2018, pp. 188–191, doi: 10.1109/ISPSD.2018.8393634.

[24] I. Rossetto, M. Meneghini, O. Hilt, E. Bahat-Treidel, C. De Santi, S. Dalcanale, J. Wuerfl, E. Zanoni, and G. Meneghesso, "Time-dependent failure of GaN-on-Si power HEMTs with p-GaN gate," *IEEE Trans. Electron Devices*, vol. 63, no. 6, pp. 2334–2339, Jun. 2016, doi: 10.1109/TED.2016.2553721.

[25] T.-L. Wu, D. Marcon, S. You, N. Posthuma, B. Bakeroot, S. Stoffels, M. Van Hove, G. Groeseneken, and S. Decoutere, "Forward bias gate breakdown mechanism in enhancement-mode p-GaN gate AlGaN/GaN high-electron mobility transistors," *IEEE Electron Device Lett.*, vol. 36, no. 10, pp. 1001–1003, Oct. 2015, doi: 10.1109/LED.2015.2465137.

[26] A. N. Tallarico, S. Stoffels, P. Magnone, N. Posthuma, E. Sangiorgi, S. Decoutere, and C. Fiegna, "Investigation of the p-GaN gate breakdown in forward-biased GaN-based power HEMTs," *IEEE Electron Device Lett.*, vol. 38, no. 1, pp. 99–102, Jan. 2017, doi: 10.1109/LED.2016.2631640.

[27] L. Zhang, Z. Zheng, S. Yang, W. Song, J. He, and K. J. Chen, "P-GaN gate HEMT with surface reinforcement for enhanced gate reliability," *IEEE Electron Device Lett.*, vol. 42, no. 1, pp. 22–25, Jan. 2021, doi: 10.1109/LED.2020.3037186.

[28] A. M. Potts, S. Bajaj, D. R. Daughton, A. A. Allerman, A. M. Armstrong, T. Razzak, S. H. Sohel, and S. Rajan, "$Al_{0.7}Ga_{0.3}N$ MESFET with all-refractory metal process for high temperature operation," *IEEE Trans. Electron Devices*, vol. 68, no. 9, pp. 4278–4282, Sep. 2021, doi: 10.1109/TED.2021.3095138.

[29] M. Yuan, Q. Xie, J. Niroula, N. Chowdhury, and T. Palacios, "GaN memory operational at 300 °C," *IEEE Electron Device Lett.*, vol. 43, no. 12, pp. 2053–2056, Dec. 2022, doi: 10.1109/LED.2022.3218671.

[30] M. Yuan, Q. Xie, J. Niroula, M. F. Isamotu, N. S. Rajput, N. Chowdhury, and T. Palacios, "High temperature robustness of enhancement-mode p-GaN-Gated AlGaN/GaN HEMT technology," in *Proc. IEEE 9th Workshop Wide Bandgap Power Devices Appl. (WiPDA)*, Nov. 2022, pp. 40–44.