Analytical Modeling of Cryogenic Subthreshold Currents in 22-nm FDSOI Technology

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***Abstract*— The transistor compact model is crucial but has yet to mature for cryogenic electronics. This paper presents a sophisticated analytical model of the MOSFET subthreshold current at cryogenic temperatures, accounting for the thermionic, hopping, source-to-drain tunneling transports, and the Gaussian-distributed interface traps to bridge the gap. Hopping and source-to-drain tunneling transports can co-exist in the subthreshold regime, leading to subthreshold saturation strongly correlated to channel length and drain voltages.**

***Index Terms*— Cryo-CMOS, band tail, FDSOI, hopping, modeling, quantum computing, subthreshold, tunneling.**

I. Introduction

CMOS technology has been proven to be a promising solution to scale-up solid-state quantum computers [1], [2]. In this perspective, CMOS front-end electronics operates at cryogenic temperatures, handling the write-in and readout for quantum bits. However, today's compact models cannot accurately predict transistor performance at cryogenic temperatures [3]. It makes circuit design a real challenge. Although recent works have tempted to modify existing compact models to mitigate the need [3], [4], [5], [6], some cryogenic phenomena are still unclear. For example, the subthreshold swing (SS), measuring the switching efficiency between on- and off-states, decreases and then saturates at cryogenic temperatures [7], [8], [9], [10], [11], [12], [13]. Therefore, transistors do not have sharp subthreshold behavior as predicted by the Boltzmann limit. Nonetheless, the mechanism causing the SS saturation has been debated in the past few years. The saturation of SS has been shown to be due to the exponential band tail that extends from the conduction band or the valence band [7], [8], [14], [15]. If the defect-induced band tail is assumed, the carriers hop via the localized states [16]. On the other hand, source-to-drain tunneling (SDT) has also been shown to lead to SS saturation for a short-channel device [9], [12], [13], [17]. As shown in Fig. 1, the subthreshold current behaves differently between low and high V_{DS}, where a significantly large SS presents in a deep weak inversion for extremely short devices, e.g., channel length $L \lesssim 20$ nm. This behavior can neither be explained by the hopping transport nor by the SDT alone. Instead of a single mechanism, it relies on multiple mechanisms as shown in the simulation work [18]. Hence, this work proposes an analytical subthreshold current and swing model, accounting for thermionic, hopping, and source-to-drain tunneling currents. This model would provide insight into the actual root cause of the degradation.

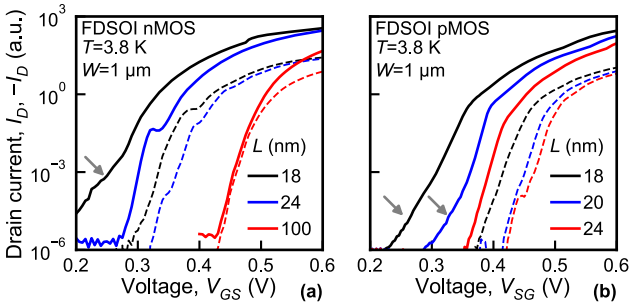

Fig. 1. Experimental transfer characteristics of FDSOI nMOS and pMOS at 3.8 K for various channel lengths. The solid and dashed lines correspond to $V_{DS} = 0.8$ V and 10 mV, respectively. Arrows highlight the parts with significant SDT.

II. Analytical Modeling

At cryogenic temperatures, the thermionic current (I_{th}) may not dominate the subthreshold drain current (I_{sub}) due to the onset of other transport mechanisms, such as tunneling or hopping transports. Among the current components, the resonant tunneling manifests randomly due to the ionized defects in the channel [10], [19]. Also, the resonant tunneling in an FDSOI technology has been modeled based on the single electron transistor [20]. Hence, the model excludes resonant tunneling, and I_{sub} is then given by

$$I_{sub} = I_{th} + I_{hop} + I_{sdt}, \tag{1}$$

with I_{sdt} the source-to-drain tunneling current, I_{hop} the hopping current. The I_{th} is well established by using Landauer formalism [21]. The following derivation focuses on I_{hop} and

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I_{sdt}, and assumes a two-dimensional gas due to the ultra-thin channel for a 22 nm FDSOI technology, e.g., $\lesssim$ 6 nm [22].

By adopting a unified current-voltage model [23], I_{hop} is given by $I_{hop} = \mu_{hop} k_B T \frac{W}{L} n_{hop} \left(1 - e^{\frac{-qV_{DS}}{k_B T}}\right)$ with q elementary charge, n_{hop} hopping carrier density at source, μ_{hop} hopping mobility, k_B Boltzmann constant, T temperature, and W device width. In the following derivation, it is assumed that μ_{hop} remains constant for simplicity, although it theoretically varies with gate bias [24]. The $n_{hop} = N_{2D}^c \int_{-\infty}^{E_b} e^{\frac{E-E_b}{W_t}} f(E)\, dE$ with N_{2D}^c two-dimensional density of states, E_b conduction band edge, W_t characteristic energy of band tail, and $f(E)$ Fermi-Dirac function [8]. The integral of n_{hop} yields the Gauss hypergeometric function [25], which can be simplified by the first-order approximation. It leads to $n_{hop} \approx n_{hop_1} + n_{hop_2}$ with $n_{hop_1} = N_{2D}^c W_t \frac{\theta}{\theta - 1} e^{\frac{-E_{bf}}{k_B T}}$ and $n_{hop_2} = N_{2D}^c W_t \frac{1}{\mathrm{sinc}(\pi\theta)} e^{\frac{-E_{bf}}{W_t}}$, where $\theta = k_B T / W_t$ and E_{bf} is the energy from barrier peak to the Fermi level at the source. Inserting the approximated n_{hop} into the current-voltage model writes $I_{hop} \approx I_{hop_1} + I_{hop_2}$. Two currents correspond to n_{hop_1} and n_{hop_2} and represent the asymptotes of hopping transport; I_{hop_1} exponentially scales with T, and I_{hop_2} depends on energy W_t. The characteristics of I_{hop_1} and I_{hop_2} project themselves to the nearest-neighbor hopping and variable-range hopping, which dominate at high and low temperatures, respectively [26]. The latter hops near the Fermi level and has less temperature dependence [27]. On the other hand, the SDT current can be expressed in an analytical form by adopting a quadratic function that describes the short-channel gate barrier, given by [13] The direct tunneling probability depends on the energy $W_{sdt} = \hbar\sqrt{q V_a} / \left(\pi L \sqrt{2m^*}\right)$ with $\hbar$ the reduced Plank constant and m^* the effective mass. The term V_a is a potential describing the parabolic gate barrier [13].

Consequently, SS is derived from (1) and is written as

$$SS_{tot} = n \left(\frac{k_B T}{q}\right) \ln(10) \left[\alpha_{th} + \alpha_{hop}\beta_{hop_1} + \alpha_{hop}\beta_{hop_2} \frac{k_B T}{W_t} + \alpha_{sdt} \frac{k_B T}{W_{sdt}} \left(1 + \frac{-U_b}{q V_a} \frac{\partial V_a}{\partial V_{pk}}\right)\right]^{-1}, \quad (2)$$

with n the slope factor, U_b the gate barrier energy, current ratios $\alpha_{th} = I_{th}/I_{sub}$, $\alpha_{hop} = I_{hop}/I_{sub}$, and $\alpha_{sdt} = I_{sdt}/I_{sub}$. The sum of the current ratios, $\alpha_{th} + \alpha_{hop} + \alpha_{sdt}$, equals one. The terms $\beta_{hop_1} = I_{hop_1}/I_{hop}$ and $\beta_{hop_2} = I_{hop_2}/I_{hop}$ are the hopping current ratios. Due to the subthreshold regime, it ignores the mobile charges and then writes $V_{GS} = \Phi_{mf} + \psi_{sf} + (Q_{dep}^* - Q_0)/C_{fox}$ with Φ_{mf} the work function difference between the front gate and channel, ψ_{sf} the front-surface potential referenced to Fermi level at source, C_{fox} the front-gate capacitance, Q_{dep}^* the effective depletion change for short-channel effect [28], and Q_0 the interface charges. Gaussian-distributed localized states have been reported to center around the band edge at cryogenic temperatures, resulting in the inflection phenomenon [29]. It is expressed by $Q_0 = -q\frac{N_0}{2}\left[\mathrm{erf}\left(\frac{-2E_{bf}}{W_0\sqrt{2}}\right) + 1\right]$ with W_0 the width of twice the standard deviation and N_0 the scale of Gaussian [29]. As a consequence, $n = \frac{\partial V_{GS}}{\partial \psi_{sf}} = 1 + \frac{1}{C_{fox}}\left(\frac{\partial Q_{dep}^*}{\partial \psi_{sf}} - \frac{\partial Q_0}{\partial \psi_{sf}}\right)$ includes the short-channel effect and Gaussian-distributed interface charges.

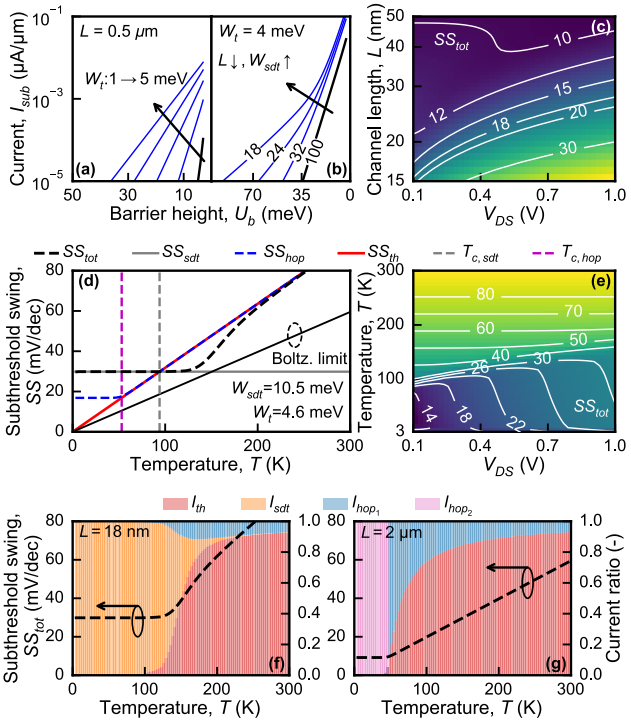

Fig. 2. (a,b) W_t and W_{sdt} influence on I_{sub} versus U_b at 4 K and V_{DS} = 1 V, the various channel lengths in nm are annotated in (b) for each curve. Note that (a, b) are plotted with U_b, the inflection phenomenon embedded in n is not presented. (c) SS_{tot} in terms of L and V_DS with U_b = 50 meV at 4 K (d) Decomposition of SS in terms of T for V_{DS} = 1 V, U_b = 0.1 eV, and L = 18 nm, (e) SS_{tot} with respect to T and V_{DS} for L = 18 nm, $U_b = 10\sqrt{300/Tk_BT}$. Calculated SS_{tot} vs. T with current decomposition for (f) L = 18 nm and (g) L = 2 μm with V_{DS} = 1 V, W_t = 4 meV, and U_b = 0.1 eV. The color shows the percentage for each current component.

In the proposed model, two energies related to the band-tail states and direct tunneling probability, i.e., W_t and W_{sdt}, are crucial for I_{sub}. As presented in Fig. 2(a,b), the increase of W_t and W_{sdt} lifts I_{sub} up, of which the raised W_{sdt} due to the shorten L particularly degrades SS at the lower current level. Fig. 2(c) further analyzes the SDT-induced degradation on SS_{tot} at 4 K, where the down-scaled L and V_{DS} are two main reasons that cause the higher SS_{tot}. Eq. (2) is presented in Fig. 2(d) as a function of temperature with other SS components. The $SS_{th} = SS_{tot}|_{\alpha_{th}=1,\alpha_{hop}=\alpha_{sdt}=0}$ stands for the thermionic SS, which linearly scales with T following the Boltzmann limit. The $SS_{hop} = SS_{tot}|_{\alpha_{hop}=1,\alpha_{sdt}=\alpha_{th}=0}$ for I_{hop} is proportional to T above the critical temperature, denoted by $T_{c,hop}$, where $SS_{hop} = SS_{th}$. For $T < T_{c,hop}$, SS_{hop} saturates at the value of $n\left(\frac{W_t}{q}\right)\ln(10)$ with $\beta_{hop_2} = 1$. Regarding SDT, thermal energy assists carriers in tunneling the gate barrier, which yields a larger current at higher T. Whereas $SS_{sdt} = SS_{tot}|_{\alpha_{sdt}=1,\alpha_{th}=\alpha_{hop}=0}$ is temperature-independent and has a value given by $n\left(\frac{W_{sdt}}{q}\right)\ln(10)\left(1 + \frac{-U_b}{qV_a}\frac{\partial V_a}{\partial V_{pk}}\right)^{-1}$. The critical temperature due to I_{sdt}, denoted by $T_{c,sdt}$, is therefore defined by T such that $SS_{sdt} = SS_{th}$. In the case of an extremely

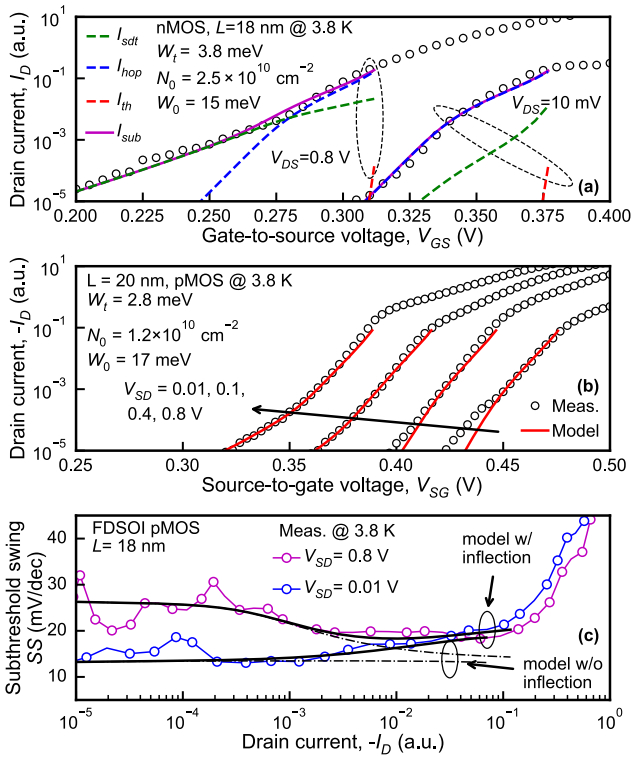

Fig. 3. Model validation by meausrement of 22 nm FDSOI technology at 3.8 K, various voltages are included. (a) transfer characteristic of an nMOS with $L = 18$ nm, each current component is plotted. (b) transfer characteristic of a pMOS with $L = 20$ nm, the model I_{sub} is compared. (c) subthreshold swing versus $-I_D$, Eq. (2) with and without Gaussiandistributed interface charge (inflection) is compared. Tunneling m^* is 0.12 and 0.13 for electrons and holes, separately.

short channel and high V_{DS}, it leads to $W_{sdt} > W_t$, and I_{sdt} dominates at cryogenic temperatures, as shown in Fig. 2(b). Consequently, the SS_{tot} saturates at SS_{sdt} as $T < T_{c,sdt}$. Additionally, it is worth noting that SS_{tot} is lower than SS_{th} as $100\,\text{K} \lesssim T \lesssim 200\,\text{K}$. It is ascribed to I_{sdt} that contributes significantly to I_{sub} over the I_{th} and I_{hop}. However, Eq. (2) shows SS_{tot} varying with U_b. It is difficult to compare the experimental SS to (2) due to the unknown U_b condition. Nevertheless, the averaged SS from the measurement in Fig. 9 of [11] may provide the reference. Fig. 2(e) gives a more realistic example on SS_{tot} with respect to T and V_{DS}, where U_b changing with T gives a reasonable weak inversion condition. It reveals that the higher V_{DS} leads to SS_{tot} saturating at the higher T. Fig. 2(e,g) shows the detailed current break down on SS_{tot} versus T for $L = 18\,\text{nm}$ and $2\,\mu\text{m}$. At $T = 300\,\text{K}$, both cases have around 90% of I_{th} and 10% of I_{hop_1}. With T decreasing, for $L = 18\,\text{nm}$, I_{sdt} gradually takes over other current components and finally dominates I_{sub}. In contrast, for $L = 2\,\mu\text{m}$, I_{hop_1} competes with I_{th} from 300 to 50 K, then $I_{sub} = I_{hop_2}$ below $T_{c,hop}$. The sharp transition from I_{hop_1} to I_{hop_2} is due to the first-order approximation of the Gauss hypergeometric function [25].

III. Experimental Validation and Discussion

The proposed model is validated by the cryogenic measurement of a commercial 22 nm FDSOI technology [22]. Fig. 3(a) presents a good agreement of the current model compared to the transfer characteristics of an nMOS at 3.8 K. At $V_{DS} = 10\,\text{mV}$, I_{hop} dominates the I_{sub} and captures the measured I_D while I_{th} and I_{sdt} are negligible. Conversely, at $V_{DS} = 0.8\,\text{V}$, the experimental I_{sub} shows two regions with different slopes, separated at $V_{GS} \approx 0.275\,\text{V}$. The region with a lower current level is controlled by I_{sdt}, while another region is ascribed to I_{hop}. Note that W_t for the band tail and N_0 and W_0 for the interface states are fitting parameters, while W_{sdt} is the function of V_a, L, and m^* [13]. Since W_{sdt} relates to V_a that changes with U_b, W_{sdt} in Fig. 3(a) ranges from $1.2 \sim 3.4\,\text{meV}$ for low V_{DS} and varies from $8 \sim 10\,\text{meV}$ for high V_{DS}. When W_{sdt} is significantly larger than W_t, the SDT yields a much more degraded SS than that hopping transport does. Fig. 3(b) shows the model validation by a pMOS with $L = 20\,\text{nm}$ at 3.8 K with various V_{SD}. Parameters (W_t, W_0, and N_0) are consistent from $V_{SD} = 10\,\text{mV}$ to 0.8 V. The high V_{SD} results in SDT that degrades SS. At $V_{DS} = 10\,\text{mV}$, the model does not fit well to the lower current region, it is likely due to the weak resonant tunneling phenomenon. Regarding the current-dependent characteristic of SS, Eq. (2) compares to the experiments of a pMOS FDSOI with $L = 18\,\text{nm}$ at 3.8 K shown in Fig. 3(c). The model accounting for the inflection phenomenon agrees better with the measurement than the one excluding inflection. In the case of $V_{DS} = 0.8\,\text{V}$, a clear transition of SS presenting around $-I_D = 10^{-3}$ a.u. is ascribed to I_{sdt} competing with I_{hop}.

Knowing what transport dominates I_{sub} can efficiently improve SS. As presented in Fig. 2(c), devices with $L \gtrsim 40\,\text{nm}$ has a negligible SDT effect, where SS does not vary with V_{DS} significantly. In such a case, SS saturation is due to the band tail. Optimal implantation of ions in the silicide process has been reported to reduce the degradation by the band tail and interface states [30]. When SS saturation is mainly due to SDT, lowering W_{sdt} helps improve SS. In addition to using the minimal L, several methods can reduce the SDT current, such as; (1) implementing a thin tunneling barrier at the source junction [9], (2) increasing m^* by strain engineering [31] or by taking a certain crystal direction, and (3) reducing the supply voltage. The first two approaches require a different device process, and the second comes at the cost of poorer mobility. As shown in Fig. 2(c,e), bringing V_{DS} down can substantially reduce SS saturated value. However, such a method may pull a transistor out of the saturation region, raising the issue of gain or linearity. Fortunately, FDSOI technology modulates the threshold voltage electrostatically through the back-gate voltage (model in [32]). The supply voltage can be scaled down by adopting the low-threshold voltage scheme.

IV. Conclusion

An analytical model of the cryogenic subthreshold current and swing has been derived and validated with a commercial 22 nm FDSOI technology. It finds that hopping and source-to-drain tunneling currents can co-exist in a short channel with strong V_{DS}. Decomposing the subthreshold current into thermionic, hopping, and source-to-drain tunneling components, provides a better understanding of the subthreshold degradation in terms of temperature, voltage, and channel length. This paper proposes approaches to improve cryogenic subthreshold performance by knowing the root reason causing the SS saturation.

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