2.7 kV Low Leakage Vertical PtO$_x$/β-Ga$_2$O$_3$ Schottky Barrier Diodes With Self-Aligned Mesa Termination

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Abstract—In this study, we fabricated superb β-Ga$_2$O$_3$ Schottky barrier diodes (SBDs) with high breakdown voltage (V_{br}) and low leakage through combining platinum oxide (PtO$_x$) and anodic self-aligned mesa termination (SAMT). The PtO$_x$ that forms a high barrier with β-Ga$_2$O$_3$ enables the SAMT to function sufficiently. The in-situ annealing dry etch process repair the mesa sidewall and improve the Schottky contact well. SBDs with different mesa-etched depths (D_{ee}) were systematically studied, including 0, 0.3, 0.6, 0.9, and 1.2 μm. The results showed that the V_{br} of the PtO$_x$/β-Ga$_2$O$_3$ SBD increased from 1120 V to 2738 V, yielding a high power figure of merit (PFOM) of 1.02 GW/cm^2. Meanwhile, the device maintained a less than 10 μA/cm^2 leakage current density until -2000 V. Devices with radii of 200, 100, and 50 μm obtained highest V_{br} of 2508, 2772, and 2738 V at a D_{ee} of 1.2 μm, respectively. The devices can be passivated by SU-8 without V_{br} degradation. This work provides an effective method for further improving the performance of β-Ga$_2$O$_3$ SBDs and promotes the application of β-Ga$_2$O$_3$ power diodes.

Index Terms—β-Ga$_2$O$_3$, PtO$_x$, breakdown voltage, power Schottky barrier diodes, self-aligned mesa termination.

I. Introduction

THE ultra-wide bandgap semiconductor β-Ga$_2$O$_3$ is a promising material for manufacturing high power density and low loss electronic devices due to its wide bandgap (~4.5 eV), high critical breakdown field (8 MV/cm), and high Baliga's figure of merit (3400$_{Si}$) compared with GaN and SiC [1], [2], [3]. The availability of melt-grown single crystal β-Ga$_2$O$_3$ substrates gives it attractive potential for low-cost and high-quality homoepitaxy [4].

Over the past decade, β-Ga$_2$O$_3$-based power electronic devices, especially vertical Schottky barrier diodes (SBDs), have developed rapidly. Most works aim at better electric field modulation, higher voltage/current application [5], and enhanced thermal management [6]. To pursue the theoretical limit of β-Ga$_2$O$_3$ SBD, various structures have been implemented to smooth the electric field distribution at the anode, including field plate [7], [8], mesa termination [9], [10], [11], [12], implanted edge termination [13], [14], [15], thermally-oxidized termination [16], [17], and junction barrier Schottky diodes [18].

Among these, the mesa termination has an obvious performance improvement owing to avoiding lateral depletion region at anode edge. However, the leakage current of mesa-structured SBDs is of considerable relevance to the Schottky contact quality of active region. The leakage current through metal/Schottky contact would be hard to control due to the barrier lowering and tunneling effect under high electric field [19]. Multi-trench combined with metal-oxide-semiconductor structure has been confirmed to be a good solution for the leakage problem in the current p-type lack period [10]. However, since most of the area of the trench SBDs is occupied by dielectric, the forward conduction characteristics are sacrificed. Meanwhile, the potential localized defects in the dielectric will involve the increased leakage current and reliability concerns such as time dependent dielectric breakdown (TDDB) under high electric fields [20], [21].

Increasing the barrier height of the Schottky contact is a simple way to reduce the leakage current. In particular, it will be more effective when the anode edge electric field is sufficiently weakened. Therefore, the combination of high Schottky barrier height and mesa termination is expected to achieve low leakage and high voltage SBD. In addition, the active area of the device would be utilized to the maximum. Recently, the metal-oxide electrode PtO$_x$ has good application prospects in β-Ga$_2$O$_3$ power devices [22], [23]. The barrier height of PtO$_x$/β-Ga$_2$O$_3$ can reach more than 1.8 eV by controlling the oxygen flow during deposition [22], [24], [25]. It can be a good choice for the conceived device structure.

In this work, we achieved over 2.7 kV β-Ga$_2$O$_3$ SBDs based on the PtO$_x$ and anodic self-aligned mesa termination (SAMT). Thanks to the high barrier height of the PtO$_x$/ β-Ga$_2$O$_3$ contact and the edge electric field modulation of the mesa structure, the leakage current density of the fabricated SBDs was suppressed effectively less than 10 μA/cm^2 under -2000 V. The in-situ annealing dry etch process (I-AE)
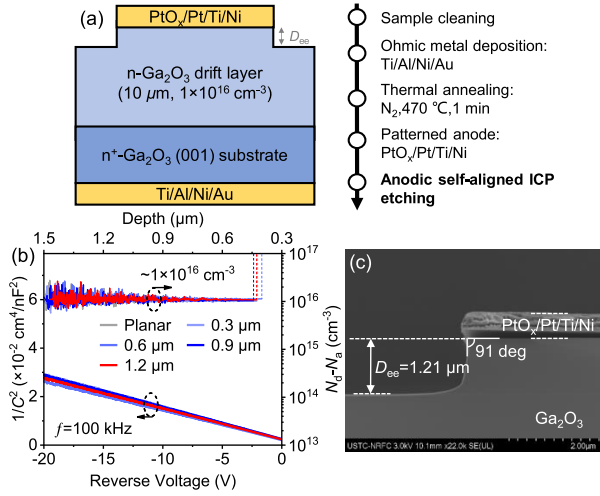
Fig. 1.　(a) Cross-sectional schematic and fabrication details of β-Ga$_2$O$_3$ SBD with SAMT. (b) Carrier concentration extracted by $1/C^2$-V characteristics. (c) Cross-sectional SEM image at the anode edge of the 1.2 μm-SBD.

Fig. 2.　I–V characteristics in (a) linear- and (b) log-scale of the SAMT-SBD with different etching depths. The V_{br} of the SAMT-SBDs (c) without passivation and (d) comparison before and after passivation. Inset in (b): extracted n and $q\Phi$ distributions with etching depth.

reduced the surface charge on the sidewalls and significantly increased the breakdown voltage (V_{br}). In addition, the relationship of electrical properties and electric field distribution to mesa-etched depths (D_{ee}) were systematically investigated.

II. DEVICE STRUCTURE AND FABRICATION

Fig. 1(a) schematically displays the device structure and fabrication details of the SBD featuring SAMT. The wafers used to fabricate the devices were taken from the same 2-inch epitaxial substrate with an epitaxial thickness about 10 μm. The epitaxial structure was grown using halide vapor phase epitaxy (HVPE) on high-conductivity (001) substrates by Novel Crystal Technology, Inc., Japan. Fig. 1(b) shows the carrier concentration (N_d-N_a) extracted by capacitance-voltage (C-V) measurements of five devices at 100 kHz before etching with an average doping about 1×10^{16} cm^{-3}.

The fabrication process flow started from organic and acid cleaning. The Ti/Al/Ni/Au (40/200/50/50 nm) metal stacks were deposited onto the backside of the samples by electron beam evaporation (E-beam), followed by 470 °C rapid thermal annealing in N$_2$ for 1 minute. The PtO$_x$/Pt Schottky anode was patterned through photoresist and deposited in magnetron sputtering system. During PtO$_x$ sputtering, the power was set to 50 W, the chamber pressure was maintained at 5.2 mTorr. And the flow rates of O$_2$ and Ar were 20 and 40 sccm, respectively. The oxygen was turned off during sputtering of Pt. To reduce the resistance of PtO$_x$ anode [25], its thickness was rigorously determined. Finally, 12 nm-thick PtO$_x$ and 84 nm-thick Pt were deposited sequentially at a rate of 1 Å/s.

The Ti/Ni (20/300 nm) metal stacks were deposited on Pt by E-beam with a rate of 1 Å/s as the hard mask for the self-aligned etch. Immediately, lift-off was performed to obtain patterned circular electrodes. Dry etching to form the mesa was performed in ICP 180 system with BCl$_3$/Ar gas flow of 35/5 sccm, 30 W RIE power, 900 W ICP power, and 5 mTorr chamber pressure. Pump oil (PO) was intentionally avoided to be applied between the Si carrier and β-Ga$_2$O$_3$ wafer so that the accumulated temperature (estimated about 150 °C) on the wafer achieved both the post-annealing (PA) of Schottky contact and the in-situ annealing repair to the sidewall.

Four samples were etched at a rate of 100 nm/min for 3, 6, 9, and 12 minutes, obtaining different D_{ee} about 0.3, 0.6,
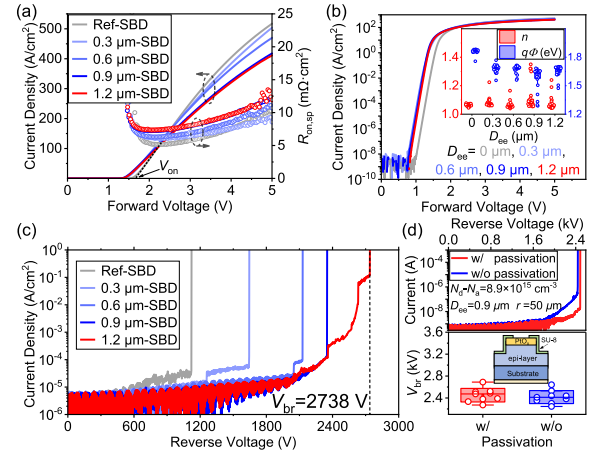
TABLE I
PROPERTIES OF THE DEVICES

Device name	Ref-SBD	0.3 μm-SBD	0.6 μm-SBD	0.9 μm-SBD	1.2 μm-SBD
D_{ee} (μm)	0	0.31	0.60	0.89	**1.21**
$R_{on,sp}$ (m$\Omega\cdot$cm^2)	5.15	6.07	6.27	7.27	**7.33**
V_{on} (V)	1.67	1.50	1.48	1.43	**1.45**
V_{bi} (V)	1.751	1.503	1.484	1.491	**1.564**
V_{br} (V)	1120	1644	2128	2350	**2738**
V_{br-Ni} (V)	654	\	1006	1304	\
PFOM (GW/cm^2)	0.24	0.45	0.72	0.76	**1.02**

All parameters listed in the table except V_{br-Ni} pertain to the PtO$_x$ devices.

0.9, and 1.2 μm. The diodes are named as 0.3, 0.6, 0.9, and 1.2 μm-SBD. Fig. 1(c) shows a scanning electron microscopy (SEM) cross-section of the 1.2 μm-SBD sample, and the rounded corner profile exist at the bottom half of the etched sidewall.

Both forward current-voltage (I-V) and C-V measurements of the devices were performed by Keysight B1500A Semiconductor Device Analyzer. The V_{br} was measured using Keysight B1505A Power Device Analyzer with devices immersed in Fluorinert FC-770.

III. RESULTS AND DISCUSSION

Fig. 2(a) shows the linear plot of forward I-V characteristics and the extracted differential specific on-resistance ($R_{on,sp}$) of five D_{ee} of devices with a diode radius (r) of 50 μm. For different D_{ee}, the $R_{on,sp}$, turn-on voltage (V_{on}) and build-in potential (V_{bi}) are extracted, as shown in Table I. The V_{on} was extracted from extrapolation of the linear fits to $J = 0$ A/cm^2. The current density (@5 V) decreases slightly with increasing D_{ee}, which may be attributed to the decrease of the spreading current and depletion of etched-sidewall [26]. The inset in Fig. 2(b) shows the statistical results of the device ideality factor (n) and barrier height ($q\Phi$) fitted by the thermionic emission (TE) model. The n and $q\Phi$ are 1.05, 1.88 eV respectively before etching. The decrease of $q\Phi$ after etching may be related to the variation of oxidation state of platinum atoms [27], [28] and the reduction of interface state [29], both influenced by the temperature introduced during I-AE.

The reverse breakdown I-V characteristics for the SAMT-SBDs with different D_{ee} are shown in Fig. 2(c). The
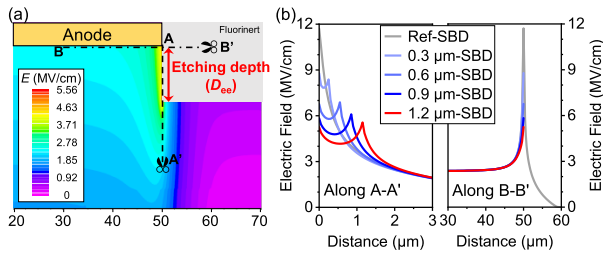
Fig. 3. (a) Simulated electric field distributions of the SAMT-SBDs under 2000 V reverse bias. (b) Extracted electric field profile of the SBDs with different D_{ee} along the vertical (left) and lateral (right) directions respectively.

Fig. 4. Comparison of (a) $1/C^2$- V curves and extracted N_d-N_a and (b) hysteresis effect and (c) breakdown characteristics for devices with (d) different etching schemes.

Fig. 5. (a) Statistical distributions of V_{br} of SAMT-SBD with different anode radii (r) and etching depths. (b) $R_{on,sp}$ versus V_{br} benchmarks of reported state-of-the-art β-Ga$_2$O$_3$ SBDs.

V_{br} values are 1644, 2128, 2350, and 2738 V for the D_{ee} of 0.3, 0.6, 0.9, and 1.2 μm, respectively. Compared with Ref-SBD (without etching), the V_{br} is increased to 2.44 times. It is noteworthy that the device maintains a low leakage current density (below 10 μA/cm^2) until -2000 V, thanks to the high barrier of PtO$_x$ and the suppression of peak electric field by the SAMT. Table I lists the device characteristics of the five types of SBDs. Besides, preliminarily results show that SAMT-SBDs can be passivated by SU-8 [30] with almost unchanged V_{br} to meet practical applications (Fig. 2(d)). Furthermore, Table I also includes the V_{br} of SAMT-SBDs using Ni anode, exhibiting significant gaps compared to the devices with PtO$_x$ anode.

TCAD simulations in Silvaco Atlas are used to simulate the electric field distribution of the device at -2000 V, as shown in Fig. 3. According to the N_d-N_a values of Fig. 4(a), the surface charge is set to -3×10^{11} cm^{-2} as estimated by assuming the depleted space-charge is balanced by the negative surface charge. As depicted in Fig. 3(b)-left, with increasing D_{ee}, the peak electric field of the mesa sidewall decreases from 11.7 MV/cm to 5.5 MV/cm. Besides, the electric field distribution along Schottky interface becomes smoother (as shown in Fig. 3(b)-right). Nevertheless, the surface electric field approaching 3 MV/cm highlights the need for a stronger Schottky contact. Therefore, the high barrier formed by PtO$_x$/β-Ga$_2$O$_3$ plays a crucial part in suppressing the leakage current and enhancing the V_{br} of the device.

Apart from the high Schottky barrier, another key factor for achieving high V_{br} is the repair of etched-sidewall to withstand the high electric fields existing there. The devices are labeled as Sample A, B, C, D, corresponding to the etching schemes of without etching, etching with PO, etching with PO & PA at 150 °C in N$_2$ for 12 minutes, etching without PO, respectively (Fig. 4(d)). The $1/C^2$-V curve of Sample B exhibits noticeable bending (Fig. 4(a)). The extracted depletion depth and N_d-N_a at 0 V (649.7 nm, and 3.6×10^{15} cm^{-3}) quite differ from the values of Sample A (469 nm, and 8.9×10^{15} cm^{-3}). It indicates a substantial surface charge located at the sidewall, which depletes the active region. Besides, for Sample A to B, the V_{br} of the devices show just 25% improvement (Fig. 4(c)), speculating that the damage to the sidewall may be a primary factor limiting the device's performance.

For comparison, the Sample D with I-AE scheme can withstand V_{br} up to 2876 V, an increase of at least 180% compared to Sample A. And the bending of $1/C^2$-V is apparently reduced (500.8 nm, and 6.4×10^{15} cm^{-3}), almost consistent with Sample A. In addition, adding PA in Sample C improves the V_{br} while having little effect on the $1/C^2$-V curve. But the obvious I-V hysteresis reduction shown in Fig. 4(b) indicates the PA mainly affect the Schottky interface quality [29]. In conclusion, the significant improvement in V_{br}
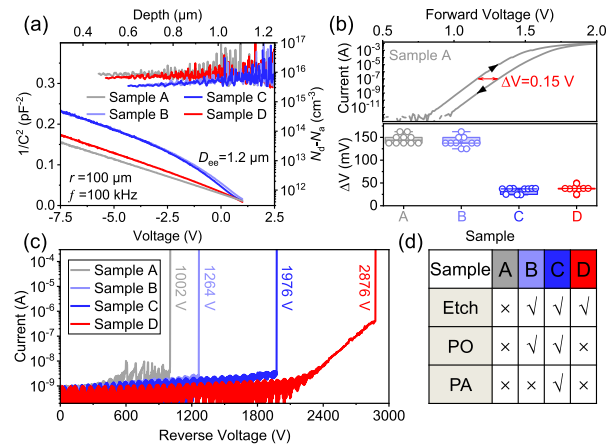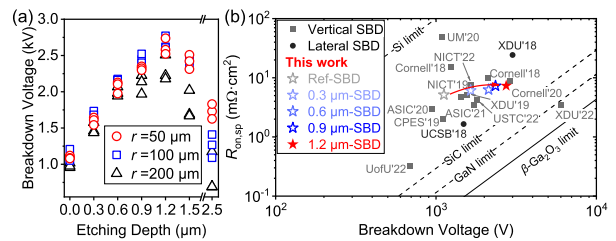
of device with I-AE can be attributed to its dual contribution in sidewall charges and Schottky contact.

The statistics of V_{br} with different r are shown in Fig. 5(a), and further increasing D_{ee} has also been performed. The V_{br} value shows an upward and then downward trend with increasing D_{ee}. The maximum V_{br} values obtained at 1.2 μm with r value of 50 μm, 100 μm and 200 μm are 2738 V, 2772 V and 2508 V, respectively, which are almost 2.4 times that of the corresponding size Ref-SBD. The trade-off point can be attributed to the accumulated damage introduced during etching, despite a monotonous increasing trend of the device's PFOM versus D_{ee} is shown based on our simulation.

The power figure of merit (PFOM) of SAMT-SBDs and Ref-SBD with r of 50 μm is benchmarked against some state-of-the-art vertical and lateral SBDs in the plot of $R_{on,sp}$ versus V_{br} in Fig. 5(b). Compared with Ref-SBD, the PFOM of 1.2 μm-SBD is increased to 4.2 times (1.02 GW/cm^2). In addition, the V_{br} of devices with different sizes in this work is at the forefront of the reported work, demonstrating the potential of combining PtO$_x$ and SAMT to achieve high performance.

IV. CONCLUSION

In summary, we have achieved high performance vertical β-Ga$_2$O$_3$ SBD through anodic self-aligned mesa etching and the meaningful adoption of PtO$_x$. The high Schottky barrier induced by PtO$_x$ endows the SAMT fully realize its function. And the I-AE process combines the dual effects of sidewall repairing and post-annealing. The device maintains a low leakage current density (<10 μA/cm^2) at -2000 V and achieves high PFOM up to 1.02 GW/cm^2. This work provides a practical and effective solution for enhancing the performance of etched terminal devices.

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