Compact Wideband Millimeter-Wave ESD Protection Device With Transformer-Embedded DCSCR

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***Abstract*— This letter presents a novel structure for electrostatic discharge (ESD) protection of millimeter wave (mm-wave) input/output (I/O). The proposed structure features a meticulously embedded transformer in the direct-connected silicon-controlled rectifier (DCSCR), which ensures wideband lossless performance through the resonance between the transformer and parasitic capacitance in DCSCR. In addition, the proposed structure sets a precedent for placing ESD protection devices beneath the inductors with a floating shield, which results in an efficient saving of silicon footprint. Verified in a 40-nm CMOS process, the proposed structure demostrates a 2.55 kV HBM level, 27.5-50 GHz bandwidth, 0.65 ns turn-on time and occupies only 88.2 × 88.2 μm^2.**

***Index Terms*— Electrostatic discharge (ESD), broadband, millimeter wave (mm-wave), silicon-controlled rectifier (SCR), floating shield.**

I. Introduction

ELECTROSTATIC discharge (ESD) has always posed a significant threat to integrated circuits (ICs) [1], [2], [3], [4]. In recent years, the demand for millimeter wave (mm-wave) ESD protection has been accelerated by the applications of 5G New Radio (NR) and mm-wave radar [5], [6]. Typical specifications for radio frequency (RF) I/O ESD protection for low noise amplifier (LNA) and power amplifier (PA) is a 2-kV human-body model (HBM) level, a fast turn-on speed (<1 ns) and $|S_{11}|<-10$ dB and $|S_{21}|>-2$ dB in the operating band. Conventional ESD protection devices often fail to meet those high-frequency specifications at mm-wave due to their parasitic capacitance, which results in losses, noise and mismatch [7], [8], [9], [10].

The utilization of inductors for compensating parasitic capacitance in radio frequency (RF) electrostatic discharge (ESD) protection, such as LC-tank [11], inductor-triggered silicon-controlled rectifier (SCR) [12], and inductor-assisted SCR [13], has become a popular approach. However, their application bandwidth (including their dual-band versions [14], [15]) is typically narrow, and they often suffer from a serious trade-off between ESD robustness and RF performance. Inductor/transmission line distribution strategies have been proposed for wideband RF ESD protection [16], [17], but the high-frequency performance remains inadequate due to their low-pass characteristics. Moreover, while T-coil-based ESD protection designs can theoretically achieve ultra-wideband protection [18], [19], actual process limitations and simulation deviations often result in poor high-frequency performance [20]. The utilization of 3-dB coupler for mm-wave ESD protection can achieve an ultra-wideband characteristic [21]. However, the ESD protection level of it is generally poor, and this approach is recommended when the center frequency $f_0 > 100$ GHz to avoid excessive area occupation.

With these concerns, this work presents a novel transformer-embedded direct-connected SCR (TDCSCR) which aims to enhance application bandwidth and achieve high ESD robustness while minimizing silicon footprint.

II. Device Structure and Operating Principle

A. ESD Protection Principle

Fig. 1(b) shows the I/O ESD protection scheme for mm-wave low voltage applications with a 1.1-2.5 V supply using the proposed TDCSCR. The TDCSCR is reverse connected between I/O-VSS and VDD-I/O. The 3D configuration of the proposed TDCSCR is shown in Fig. 1(a). By connecting the N-Well and P-Well together, the DCSCR offers a diode-like low trigger voltage, an SCR-like high-ESD robustness, and concurrently reduces the overshoot voltage [22], [25].

Between the anode and cathode, P+/N-Well/P-Well/N+ form a typical SCR path. The N-Well and P-Well is directly connected through inductor L_2 and form a two-diode trigger path, as shown in Fig. 2(a). At the onset of ESD stress from anode to cathode, the trigger path is activated to discharge the initial current. Once the SCR is triggered, the intrinsic

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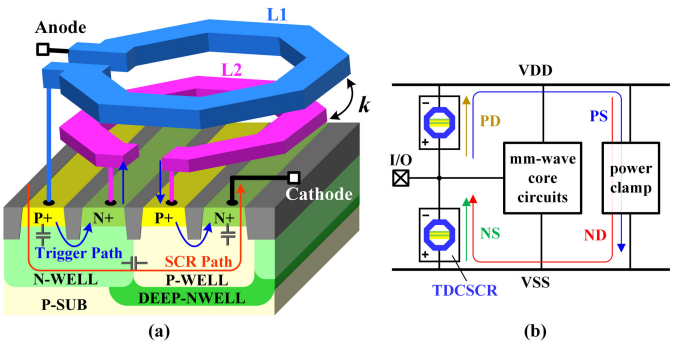

Fig. 1. (a) 3D configuration of the proposed device. (b) mm-wave I/O ESD protection scheme.

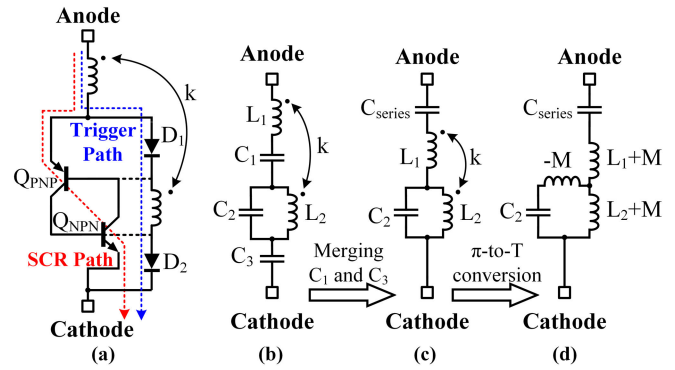

Fig. 2. (a) Equivalent circuit of the proposed device. (b) High-frequency small-signal equivalent circuit of the proposed device. (c) Equivalent circuit after merging C_1 and C_3 together. (d) Equivalent circuit after performing π-to-T conversion.

positive-feedback of Q_{PNP} and Q_{NPN} will divert most of the ESD current. Under normal conditions, the device is in the off state because the voltage between the anode and cathode is negative.

B. High-Frequency Characteristic

The high-frequency equivalent circuit is shown in Fig. 2(b). After simplification (Fig. 2(c), where $C_{series} = C_1C_3/(C_1 + C_3)$) and performing π-to-T conversion of the transformer, the equivalent circuit can be converted to Fig. 2(d). The impedance of the TDCSCR can then be derived as equation (1), shown at the bottom of the page, where the mutual inductance $M = k\sqrt{L_1L_2}$ and k is the coupling factor.

Because the ESD protection device is connected in parallel between the I/O port and VSS/VDD, the higher the impedance of the device, the lower the signal loss is on it (insertion loss $S_{21} \sim 0$ dB). According to equation (1), as shown at the bottom of the page, the TDCSCR can offer a high-impedance range around 30-60 GHz, which is the low-loss band shown in Fig. 3(b). On the other hand, the loss of traditional DCSCR continues to increase as the frequency increases due to its only-capacitance characteristic.

In order to extend the low-loss band around 40 GHz, we have analyzed the effect of the coupling factor k in the

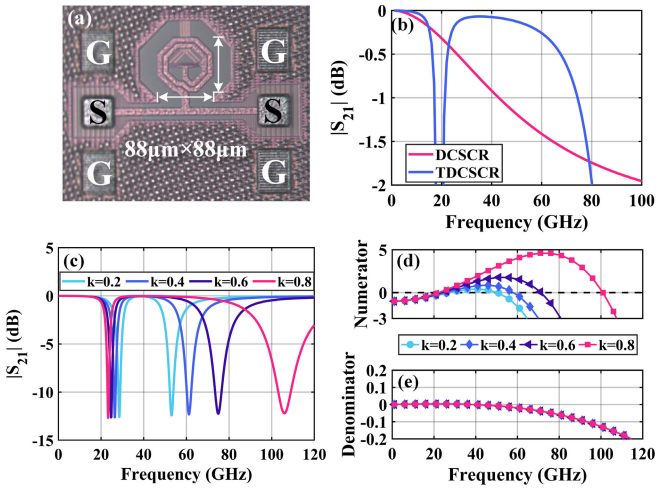

Fig. 3. (a) Chip micrograph. (b) Simulated $|S_{21}|$ of traditional DCSCR and the proposed TDCSCR. (c) Simulated $|S_{21}|$ with different coupling factor k. Calculated (d) numerators and (e) denominators of the impedance of TDCSCR with different coupling factor k.

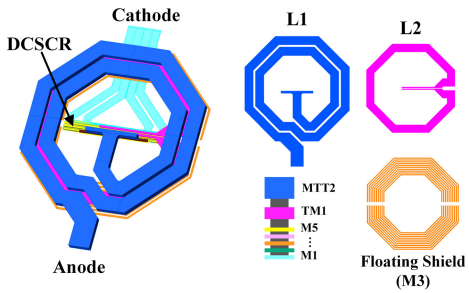

Fig. 4. Layered schematic of the proposed device.

numerator and denominator of $Z(\omega)$ separately. The calculated numerators and denominators of $Z(\omega)$ with different k, are shown in Fig. 3(d) and (e), respectively. For a given k, there are two zeros in the numerator of $Z(\omega)$. And the absolute value of the k-unrelated denominator is small enough from 0 to 100 GHz. Thus the frequency range between the two zeros of the numerator can be seen as a high-impedance range. And the two zeros of the numerator, which respectively indicates the two notches in Fig. 3(c), are more separated as k increases. Therefore the high-impedance band, or the low-loss band, is extended when k is increased.

C. Layout Optimization

To minimize the RF energy coupled into the substrate, there are ground shields placed under inductors. These shields usually contain layers including M1 (Metal 1), GT (Poly Gate) and AA (Active Area), which eliminate all possibilities of placing other semiconductor devices under the inductors. In this work, we exploit the floating shield, instead of conventional ground shield, to free up space under the inductors to place the semiconductor-part of TDCSCR. Fig. 4 shows the actual proportions and shapes of the inductors and the floating

$$Z(\omega) = j\frac{[C_1C_2(M^2 - L_1L_2)\omega^4 + (C_1L_1 + C_1L_2 + C_2L_2 + 2C_1M)\omega^2 - 1]}{\omega C_1(1 - \omega^2C_2L_2)} \quad (1)$$

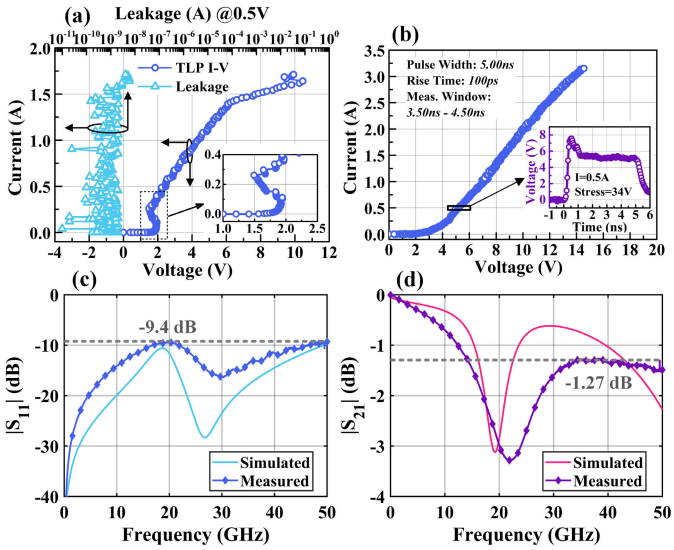

Fig. 5. (a) Measured TLP I-V curve and leakage current at 0.5 V bias. (b) Measured VF-TLP I-V curve and the transient waveform at I=0.5 A. Measured and simulated (c) $|S_{11}|$ and (d) $|S_{21}|$ of the TDCSCR.

shield. The coupling factor k of the transformer is designed as high as possible. The floating shield is implemented using horseshoe-shaped M3. So that AA and M1/M2 can be used to place the DCSCR and metal wires.

III. Experimental Results and Discussion

The proposed TDCSCR is fabricated in a conventional 40-nm CMOS process. Fig. 3(a) shows the chip micrograph. The width of DCSCR is selected as 54 μm. According to the Process Design Kit (PDK) of the manufacturing process, corresponding parasitic capacitances are $C_1 = C_3 = 71$ fF and $C_2 = 200$ fF. L_1 and L_2 are chosen as 480 pH and 160 pH, respectively, for wideband ESD protection around 30-40 GHz.

A. ESD Protection Performance

1) TLP Performance: The measurement results of transmission line pulsing (TLP) test with a rise time of 10 ns and a pulse width of 100 ns is shown in Fig. 5(a). The TDCSCR exhibits a trigger voltage of 1.9 V, with a small snapback to 1.5 V after device triggering. This could be attributed to the increase in high-frequency impedance of the connection between N-Well and P-Well [23], which is caused by L_2 ($Z_L = j\omega L$). The secondary breakdown current (I_{t2}) is 1.7 A, which is equivalent to HBM level of 2.55 kV. The leakage currents are measured with the anode biased at 0.5 V. The leakage currents are $<$ 6 nA, and in most cases are lower than 2 nA.

2) VF-TLP Performance: Another very-fast TLP (VF-TLP) measurement is implemented with a rise time of 100 ps and a pulse width of 5 ns using ESDEMC ES620. As shown in Fig. 5(b), the VF-TLP-measured I_{t2} is at a high level of 3.15 A. The inset of Fig. 5(b) shows the transient voltage waveform at I=0.5 A and stress voltage=34 V. The overshoot voltage is 7.5 V, which is comparable with [22] (7.4 V) and [23] (5.5 V) (see Table I). The turn-on time is 0.65 ns. Further reduction of overshoot voltage can be achieved by implementing the co-design method [25] or secondary clamp [26].

TABLE I
VF-TLP Performance Comparison

	Structure	Overshoot (V)	Conditions	
[22]	DCSCR	7.4	I (N/A)	Stress= 25 V
[23]	DCSCR+R	5.5	I= 0.5 A	Stress (N/A)
This	**TDCSCR**	**7.5**	**I= 0.5 A**	**Stress= 34 V**

TABLE II
Comprehensive Performance Comparison

	This work	EDL'22 [24]	MWCL'20 LASCR [15]	TMTT'12 LTSCR [12]
Technology	**40nm CMOS**	40nm CMOS	180nm CMOS	65nm CMOS
BW@$S_{21}>-2$dB (GHz)	**27.5-50**	37.4-47.8*	25-45*	43-61*
FBW	**58%**	24.4%	57.1%	31.6%
I_{t2} (A)	**1.7**	1.25	1.86	1.75
Leakage (nA)	**6 @0.5V**	40 @1.8V	70 @1.8V	Unknown
Area (μm^2)	**88.2×88.2**	102×239	110×130	100×130
FOM[1] (A·GHz·mm^{-2})	**127.3**	12.5	74.3	42.5

[1] FOM=I_{t2}×FBW(@$S_{21}>-2$dB)÷Area
* Estimated from curves.

B. High-Frequency Performance

Fig. 5(c) and Fig. 5(d) shows the layout EMX simulation results and measured S_{11} (reflection) and S_{21} (transmission), respectively. The S-parameters of the test device is measured by vector network analyzer and de-embedded from the ground-signal-ground (G-S-G) test structure. The measured $|S_{11}|$ is below -9.4 dB from DC to 50 GHz, which means good impedance matching is achieved in a wide range. The $|S_{21}|$ can reach to -1.27 dB at 38.5 GHz and is better than -2 dB from 27.5 GHz to 50 GHz (Due to limitation of the testing equipment). This demonstrates the wideband millimeter-wave ESD protection range of the proposed device.

C. Comprehensive Comparison

A comprehensive comparison between the proposed TDCSCR and the state-of-the-art mm-wave ESD protection devices is shown in Table II. The proposed TDCSCR shows the widest fractional bandwidth (FBW), lowest leakage current, high ESD robustness and a compact area.

IV. Conclusion

In this letter, we proposed a novel broadband mm-wave low voltage I/O ESD protection device. A transformer is embedded in the DCSCR to realize wideband lossless performance in 27.5-50 GHz band. In addition, the idea of placing semiconductor devices beneath inductors provides new possibilities for high-frequency ESD protection design. While reducing silicon footprint, the available area below the inductors has enormous potential to further enhance ESD robustness. The proposed device has been verified in a 40-nm CMOS process, demonstrating high ESD robustness and wideband lossless performance. The turn-on speed of the device is not degraded by the presence of the transformer during CDM events.

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