

# Gate-Bias Induced $R_{ON}$ Instability in p-GaN Power HEMTs

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**Abstract**—In this letter, we investigate the on-resistance ( $R_{ON}$ ) instability in p-GaN power HEMTs induced by a positive or negative gate bias ( $V_{GB}$ ), following the application of a quasi-static initialization voltage ( $V_{GP}$ ) of opposite sign. The transient behavior of this instability was characterized at different temperatures in the 90–135 °C range. By monitoring the resulting drain current transients, the activation energy as well as time constants of the processes are characterized. Not trivially, both  $R_{ON}$  increase/decrease were found to be thermally activated and with same activation energy. We attribute the thermal activation of both  $R_{ON}$  increase/decrease to the charging/discharging of hole traps present in the AlGaN barrier in the region below the gate.

**Index Terms**—pGaN HEMTs, dynamic ON-resistance, instability, NBTI, PBTI, barrier traps.

## I. INTRODUCTION

SEVERAL studies are present in the literature that involve the investigation of the stability of normally-off p-GaN high electron mobility transistors (HEMTs) after applying gate bias stress [1], [2], [3], [4], [5], [6], [7], [8], [9]. These studies mostly focus on the instability of the threshold voltage ( $V_T$ ) [2], [4], [5], [6], [7], [8], [9], [10] caused by dynamic effects occurring at (or near) the device region under the gate [11]. On the other hand, a detailed analysis of

the consequences of gate biasing on device ON-resistance ( $R_{ON}$ ) has not been presented yet, despite  $R_{ON}$  instability can be a more serious concern from the application standpoint (i.e., at large overdrive) than the more widely investigated  $V_T$  drift [7]. Recently, a preliminary characterization of the effects of negative/positive gate bias on  $R_{ON}$  in devices of a previous generation compared to the ones analyzed in this letter was presented in [12], which lacked however the physical interpretation of the observed instabilities.

In this letter, we investigate the influence of gate bias on the  $R_{ON}$  instability and characterize its time- and temperature-dependent behavior. First, we characterize  $R_{ON}$  after applying a quasi-static (50 min) gate bias ( $V_{GP}$ ) of different magnitudes between  $-6$  and  $+6$  V at a baseplate temperature of 90 °C. Then, we characterize the drain current transient response at different temperatures in the 75–135 °C range by applying baseline biases ( $V_{GB}$ ) with different magnitudes and by periodically sensing  $R_{ON}$ . The obtained transients allow characterizing the time constants ( $\tau$ ) and activation energy ( $E_A$ ) of the processes involved. The experiments reveal a set of features of  $R_{ON}$  instability which we attribute to charging/discharging of hole traps present in the AlGaN barrier in the region below the gate.

## II. EXPERIMENTAL CHARACTERIZATION

The devices under test (DUT's) are 650-V, packaged, normally-off, p-GaN power HEMTs with a Schottky gate contact. Typical drain current ( $I_D$ ) and gate current ( $I_G$ ) vs gate-to-source bias ( $V_{GS}$ ) characteristics at a drain-to-source bias ( $V_{DS}$ ) of  $= 50$  mV and  $T = 90$  °C are reported in Fig. 1(a), and (b). Figure 1(c) shows the  $R_{ON}$  variation occurring after applying a constant  $V_{GS}$  bias ( $V_{GP}$ ) for 50 minutes with different magnitudes.  $R_{ON}$  is computed as the ratio between  $V_{DS} = 50$  mV and  $I_D$  measured at  $V_{GS} = 6$  V. Interestingly, little  $R_{ON}$  variation was observed after applying  $V_{GP} \geq 1.5$  V, whereas  $R_{ON}$  increased linearly with decreasing  $V_{GP}$  below 1.5 V, resulting in a  $\approx 17\%$  increase after  $V_{GP} = -6$  V with respect to its minimum value, see Fig. 1(c).

$R_{ON}$  time evolution was investigated by applying to the gate terminal the voltage waveforms depicted in Fig. 2(a). After a 50-minutes initialization bias at  $V_{GP}$ ,  $V_{GS}$  is settled to a baseline bias ( $V_{GB}$ ) while periodically sampling (i.e., every 50 ms)  $I_D$  at  $V_{GM} = 6$  V. A short, 2-ms  $V_{GM}$  pulse is

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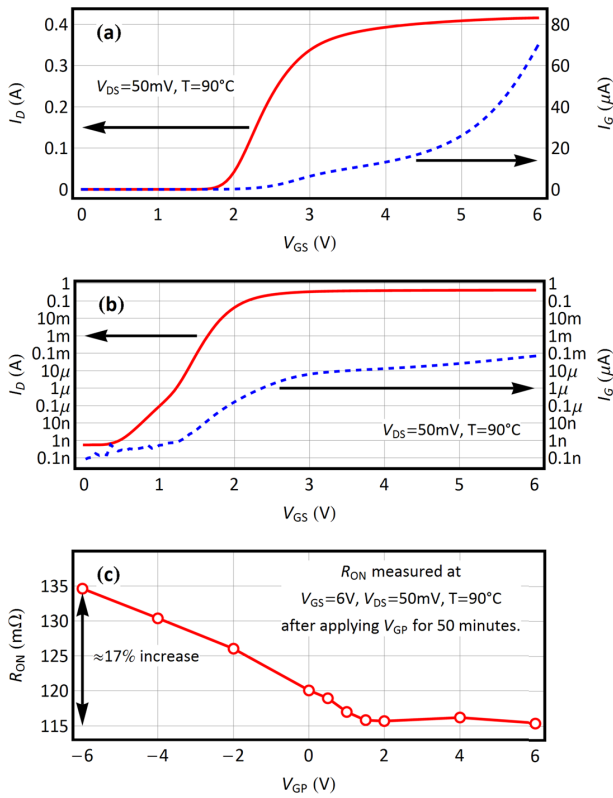


Fig. 1. Typical  $I_D$ - $V_{GS}$  and  $I_G$ - $V_{GS}$  curves in the (a) linear and (b) semi-log scale obtained at  $V_{DS} = 50$  mV and  $T = 90^\circ\text{C}$ . (c) Observed  $R_{ON}$  variation obtained after applying a  $V_{GP}$  bias for 50 minutes with varying magnitude. Maximum  $R_{ON}$  variation after  $V_{GP} = -6$  V is  $\approx 17\%$  of its minimum value obtained at  $V_{GP} \geq 1.5$  V.

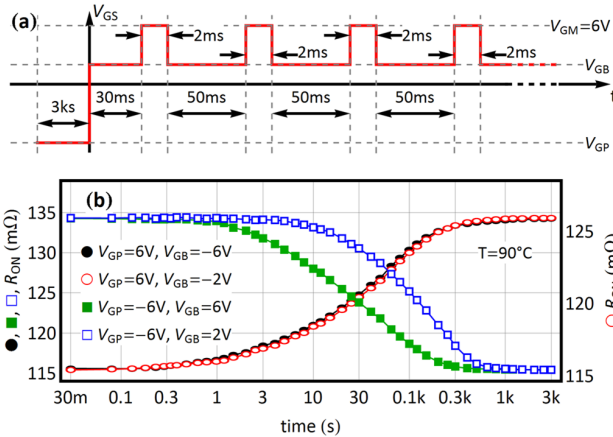


Fig. 2. (a) Voltage waveform applied at the gate terminal for the characterization of  $I_D/R_{ON}$  transients.  $V_{GP}$  is first applied for 3 ks (i.e., 50 minutes), then  $V_{GB}$  is applied and DUT's  $R_{ON}$  is periodically sensed at  $V_{GM} = 6$  V for 2 ms every 50 ms, except for the first sensing done after 30 ms. (b) Results of the characterization in terms of  $R_{ON}$  vs time for four different  $(V_{GP}, V_{GB})$  combinations (see legend).

applied to limit possible influence on the state of the device. This technique allows to acquire dependable data for wider time and temperature windows than the one employed in [12]. By employing a combination of different  $(V_{GP}, V_{GB})$ , several Drain Current Transients (DCTs) are extracted, from which the  $R_{ON}$  instability transients are derived. The initialization phase with positive (negative)  $V_{GP}$  ensures that the traps in the barrier (responsible for the instability, as discussed in Sec. III) are close to being fully occupied (empty) prior to

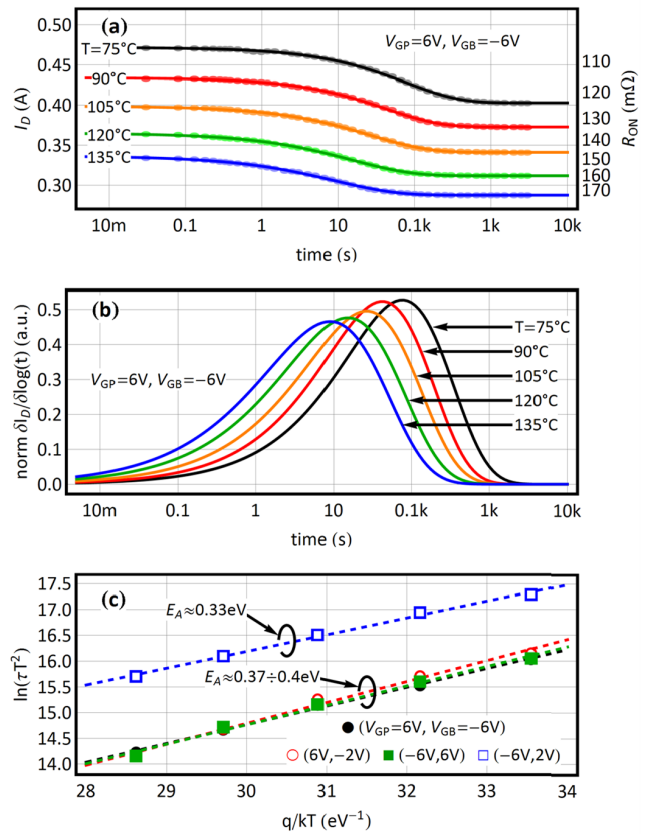


Fig. 3. (a)  $I_D/R_{ON}$  transients taken at different baseplate temperatures,  $T$ , see plot, at  $(V_{GP}, V_{GB}) = (+6, -6)$  V. (b)  $\partial I_D / \partial [\log(t)]$  corresponding to (a) from which  $\tau$ 's are extracted. (c) Arrhenius plots built from the extracted  $\tau$ 's for different  $(V_{GP}, V_{GB})$  combinations, see legend.  $E_A$ 's extracted from the linear fitting of the plots are also indicated.

the subsequent  $R_{ON}$  transient characterization. This comes as a consequence of the chosen  $V_{GP}$  and  $V_{GB}$ , which are always of opposite sign. Figure 2(b) shows the results of the characterization for a selection of the  $(V_{GP}, V_{GB})$  combinations, namely:  $(+6, -6)$ ,  $(+6, -2)$ ,  $(-6, +6)$ , and  $(-6, +2)$  V. In each case, an exponential-like evolution of  $I_D$ , and therefore  $R_{ON}$ , is obtained. We observe that when applying a negative (positive)  $V_{GB}$  after a positive (negative)  $V_{GP}$ ,  $R_{ON}$  increases (decreases). Note that the first three combinations lead to a similar time evolution, whereas a slower transient is obtained for  $(V_{GP}, V_{GB}) = (-6, +2)$  V. We mention that although the first data point is acquired at 30 ms after the initialization phase is completed, no significant  $R_{ON}$  variation occurs for shorter times. This is deduced from the fact that transients taken for equal and opposite  $(V_{GP}, V_{GB})$  are within the same  $R_{ON}$  range. For instance,  $R_{ON}$  transient obtained at  $T = 90^\circ\text{C}$  with  $(V_{GP}, V_{GB}) = (-6, +6)$  V is bound between  $\approx (135, 115)$  m $\Omega$  and the one obtained with  $(V_{GP}, V_{GB}) = (+6, -6)$  V is bound between  $\approx (115, 135)$  m $\Omega$ , see Fig. 2(b). Additional  $R_{ON}$  transients acquired by applying  $V_{GB} = -6/+6$  V sequentially for three consecutive cycles (not shown) also reveal that  $R_{ON}$  stays within the bounds identified previously, further indicating that no additional effects take place for very short times.

DCTs were further characterized at different temperatures to extract the activation energy ( $E_A$ ) of the processes leading to  $R_{ON}$  instability. DCTs obtained at  $T = 75$ – $135^\circ\text{C}$  for  $(V_{GP}, V_{GB}) = (-6, +6)$  V are shown in Fig. 3(a). As it

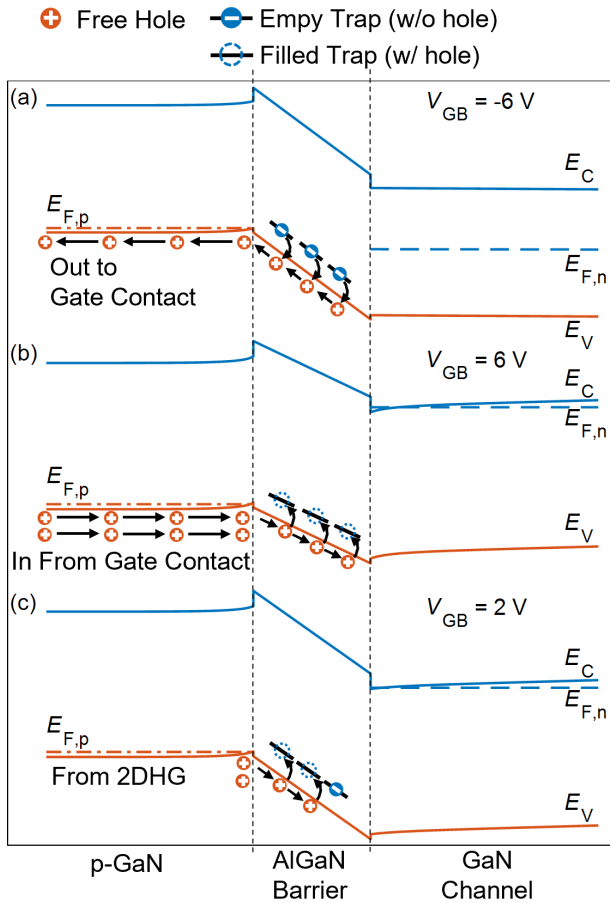


Fig. 4. Sketch of the band diagrams at (a)–(c)  $V_{GB} = (-6, 6, 2)$  V illustrating the processes leading to  $R_{ON}$  instability. At  $V_{GB} = -6$  V, see (a), holes are emitted from barrier traps and collected by the gate contact leaving negatively ionized charges which increase  $R_{ON}$ . This mechanism also occurs at  $V_{GB} = -2$  V. At  $V_{GB} = 6$  V, see (b), holes are injected by the reverse biased Schottky gate contact that get trapped into barrier traps decreasing  $R_{ON}$ . At  $V_{GB} = 2$  V, see (c), holes are supplied by the 2DHG at the pGaN/AlGaN interface. These holes also get trapped into barrier traps thus decreasing  $R_{ON}$  but with longer  $\tau$ 's with respect to (b).

can be seen, the exponential behavior of  $I_D$  vs time is maintained, while the associated time constants ( $\tau$ 's) decrease with increasing  $T$ .  $\tau$ 's are determined as the instants corresponding to peaks in the  $\partial I_D / \partial [\log(t)]$  signals [13]. Figure 3(b) shows the normalized  $\partial I_D / \partial [\log(t)]$  curves, from which the  $\tau$ 's are readily extracted and then used to build the Arrhenius plots reported in Fig. 3(c) for the  $(V_{GP}, V_{GB})$  conditions previously discussed. Interestingly, the linear fitting of the Arrhenius plots corresponding to the DCTs with  $(V_{GP}, V_{GB}) = (+6, -6)$ ,  $(+6, -2)$ ,  $(-6, +6)$  V yield similar signatures with same  $E_A$ 's in the 0.37–0.4 eV range. On the other hand, the DCT at  $(V_{GP}, V_{GB}) = (-6, +2)$  V shows higher  $\tau$ 's compared to the previous conditions for all  $T$ , and the extracted  $E_A$  is slightly lower,  $\approx 0.33$  eV.

### III. DISCUSSION

The observed features of the  $R_{ON}$  transients can be attributed to charge/discharge of hole traps present in the AlGaN barrier in the region below the gate. Figure 4 shows a sketch of the band diagrams under different  $V_{GB}$  that we

use as an aid to the discussion. At  $V_{GB} = -6/-2$  V, see Fig. 4(a), trapped holes in the barrier are emitted from traps and are collected by the gate contact, leaving behind negatively ionized charges which increase  $R_{ON}$ .  $E_A \approx 0.37-0.4$  eV extracted in Fig. 3(b) in this condition corresponds to the energy difference between the trap level and the AlGaN valence band edge. At  $V_{GB} = 6$  V, see Fig. 4(b), holes injected by the reverse biased Schottky gate contact get trapped by the negatively ionized barrier traps, which decreases  $R_{ON}$ .  $T$ -activation of trapping with the same activation energy  $E_A \approx 0.37-0.4$  eV characterizing the hole emission process is not a trivial finding. A possible explanation is that under low hole injection conditions and relatively high trap concentration in the AlGaN barrier, hole density  $p$  is about proportional to  $\exp[-(E_T - E_V)/kT]$ . As a result, also the hole capture rate, that is proportional to  $p$  is thermally activated with the same  $E_A = E_T - E_V \approx 0.37-0.4$  eV [14]. Considering the reported Mg energy level in GaN in the range of 0.16–0.26 eV [11], [15], [16] and the AlGaN/GaN valence band offset [17], the extracted  $E_A$  range is compatible with Mg out-diffused in the barrier during epitaxial growth [18].

Finally, at  $V_{GB} = 2$  V, Fig. 4(c), shows that holes are negligibly injected by the gate contact, which are thus slowly supplied to the barrier traps by the two-dimensional hole gas (2DHG) present at the pGaN/AlGaN heterojunction [6]. Similarly to the previous case, holes also get trapped into barrier traps thus decreasing  $R_{ON}$  but similarly to the previous case but with longer  $\tau$ 's due to the less effective hole injection mechanism within the AlGaN barrier. The injection mechanism also affects the  $T$ -dependence of  $R_{ON}$  decrease in this case. Being limited also by the hole injection mechanism however, the extracted activation energy ( $E_A \approx 0.33$  eV) does not correspond to the trap energy level as in the previous cases.

### IV. CONCLUSION

We investigated the on-resistance ( $R_{ON}$ ) instability in p-GaN power HEMTs induced by gate biases. Results reveal that the activation energy ( $E_A$ ) associated to the  $R_{ON}$  instabilities is to a first approximation unaffected by the applied gate bias, although the time constants ( $\tau$ 's) depend on it. The thermal activation of the  $R_{ON}$  transients points to a charging/discharging mechanism of hole traps present in the AlGaN barrier in the region below the gate.

### REFERENCES

- [1] S. Pan, S. Feng, X. Li, K. Bai, X. Lu, Y. Li, Y. Zhang, L. Zhou, and M. Zhang, "Characterization of hole traps in reverse-biased Schottky-type p-GaN gate HEMTs by current-transient method," *Appl. Phys. Lett.*, vol. 121, no. 15, Oct. 2022, Art. no. 153501, doi: 10.1063/5.0107459.
- [2] A. Stockman, E. Canato, M. Meneghini, G. Meneghesso, P. Moens, and B. Bakeroot, "Schottky gate induced threshold voltage instabilities in p-GaN Gate AlGaN/GaN HEMTs," *IEEE Trans. Device Mater. Rel.*, vol. 21, no. 2, pp. 169–175, Jun. 2021, doi: 10.1109/TDMR.2021.3080585.
- [3] S. Elangovan, E. Y. Chang, and S. Cheng, "Analysis of instability behavior and mechanism of E-mode GaN power HEMT with p-GaN gate under off-state gate bias stress," *Energies*, vol. 14, no. 8, p. 2170, Apr. 2021, doi: 10.3390/en14082170.

- [4] A. Stockman, E. Canato, M. Meneghini, G. Meneghesso, P. Moens, and B. Bakeroot, "Threshold voltage instability mechanisms in p-GaN gate AlGaIn/GaN HEMTs," in *Proc. 31st Int. Symp. Power Semiconductor Devices ICs (ISPSD)*, May 2019, pp. 287–290, doi: [10.1109/ISPSD.2019.8757667](https://doi.org/10.1109/ISPSD.2019.8757667).
- [5] L. Sayadi, G. Iannaccone, S. Sicre, O. Häberlen, and G. Curatola, "Threshold voltage instability in p-GaN gate AlGaIn/GaN HFETs," *IEEE Trans. Electron Devices*, vol. 65, no. 6, pp. 2454–2460, Jun. 2018, doi: [10.1109/TED.2018.2828702](https://doi.org/10.1109/TED.2018.2828702).
- [6] L. Efthymiou, K. Murukesan, G. Longobardi, F. Udrea, A. Shibib, and K. Terrill, "Understanding the threshold voltage instability during OFF-state stress in p-GaN HEMTs," *IEEE Electron Device Lett.*, vol. 40, no. 8, pp. 1253–1256, Aug. 2019, doi: [10.1109/LED.2019.2925776](https://doi.org/10.1109/LED.2019.2925776).
- [7] H. Wang, J. Wei, R. Xie, C. Liu, G. Tang, and K. J. Chen, "Maximizing the performance of 650-V p-GaN gate HEMTs: Dynamic RON characterization and circuit design considerations," *IEEE Trans. Power Electron.*, vol. 32, no. 7, pp. 5539–5549, Jul. 2017, doi: [10.1109/TED.2018.2828702](https://doi.org/10.1109/TED.2018.2828702).
- [8] X. Tang, B. Li, H. A. Moghadam, P. Tanner, J. Han, and S. Dimitrijevic, "Mechanism of threshold voltage shift in p-GaN Gate AlGaIn/GaN transistors," *IEEE Electron Device Lett.*, vol. 39, no. 8, pp. 1145–1148, Aug. 2018, doi: [10.1109/LED.2018.2847669](https://doi.org/10.1109/LED.2018.2847669).
- [9] Y. Shi, Q. Zhou, Q. Cheng, P. Wei, L. Zhu, D. Wei, A. Zhang, W. Chen, and B. Zhang, "Carrier transport mechanisms underlying the bidirectional shift  $V_{TH}$  in p-GaN Gate HEMTs under forward gate stress," *IEEE Trans. Electron Devices*, vol. 66, no. 2, pp. 876–882, Feb. 2019, doi: [10.1109/TED.2018.2883573](https://doi.org/10.1109/TED.2018.2883573).
- [10] J. Wei, R. Xie, H. Xu, H. Wang, Y. Wang, M. Hua, K. Zhong, G. Tang, J. He, M. Zhang, and K. J. Chen, "Charge storage mechanism of drain induced dynamic threshold voltage shift in p-GaN gate HEMTs," *IEEE Electron Device Lett.*, vol. 40, no. 4, pp. 526–529, Apr. 2019, doi: [10.1109/LED.2019.2900154](https://doi.org/10.1109/LED.2019.2900154).
- [11] M. Meneghini, C. De Santi, I. Abid, M. Buffolo, M. Cioni, R. A. Khadar, L. Nela, N. Zagni, A. Chini, F. Medjdoub, G. Meneghesso, G. Verzellesi, E. Zononi, and E. Matioli, "GaN-based power devices: Physics, reliability and perspectives," *J. Appl. Phys.*, vol. 130, no. 16, p. 227, 2021, doi: [10.1063/5.0061354](https://doi.org/10.1063/5.0061354).
- [12] N. Zagni, M. Cioni, M. E. Castagna, M. Moschetti, F. Iucolano, G. Verzellesi, and A. Chini, "Symmetrical VTH/RON drifts due to negative/positive gate stress in p-GaN power HEMTs," in *Proc. IEEE 9th Workshop Wide Bandgap Power Devices Appl. (WiPDA)*, Redondo Beach, CA, USA, Nov. 2022, pp. 31–34, doi: [10.1109/WiPDA.56483.2022.9955267](https://doi.org/10.1109/WiPDA.56483.2022.9955267).
- [13] D. Bisi et al., "Deep-level characterization in GaN HEMTs-part I: Advantages and limitations of drain current transient measurements," *IEEE Trans. Electron Devices*, vol. 60, no. 10, pp. 3166–3175, Oct. 2013, doi: [10.1109/TED.2013.2279021](https://doi.org/10.1109/TED.2013.2279021).
- [14] G. Verzellesi, A. Mazzanti, A. F. Basile, A. Boni, E. Zononi, and C. Canali, "Experimental and numerical assessment of gate-lag phenomena in AlGaAs-GaAs heterostructure field-effect transistors (FETs)," *IEEE Trans. Electron Devices*, vol. 50, no. 8, pp. 1733–1740, Aug. 2003, doi: [10.1109/TED.2003.815134](https://doi.org/10.1109/TED.2003.815134).
- [15] J. L. Lyons, A. Janotti, and C. G. Van de Walle, "Shallow versus deep nature of Mg acceptors in nitride semiconductors," *Phys. Rev. Lett.*, vol. 108, pp. 156403-1–156403-5, Apr. 2012, doi: [10.1103/PhysRevLett.108.156403](https://doi.org/10.1103/PhysRevLett.108.156403).
- [16] W. Götz, N. M. Johnson, J. Walker, D. P. Bour, and R. A. Street, "Activation of acceptors in Mg-doped GaN grown by metalorganic chemical vapor deposition," *Appl. Phys. Lett.*, vol. 68, no. 5, pp. 667–669, Jan. 1996, doi: [10.1063/1.116503](https://doi.org/10.1063/1.116503).
- [17] O. Ambacher, J. Smart, J. R. Shealy, N. G. Weimann, K. Chu, M. Murphy, W. J. Schaff, L. F. Eastman, R. Dimitrov, L. Wittmer, M. Stutzmann, W. Rieger, and J. Hilsenbeck, "Two-dimensional electron gases induced by spontaneous and piezoelectric polarization charges in N- and Ga-face AlGaIn/GaN heterostructures," *J. Appl. Phys.*, vol. 85, no. 6, pp. 3222–3233, Mar. 1999, doi: [10.1063/1.369664](https://doi.org/10.1063/1.369664).
- [18] N. E. Posthuma, S. You, H. Liang, N. Ronchi, X. Kang, D. Wellekens, Y. N. Saripalli, and S. Decoutere, "Impact of Mg out-diffusion and activation on the p-GaN gate HEMT device performance," in *Proc. 28th Int. Symp. Power Semiconductor Devices ICs (ISPSD)*, Prague, Czech Republic, Jun. 2016, pp. 95–98, doi: [10.1109/ISPSD.2016.7520786](https://doi.org/10.1109/ISPSD.2016.7520786).