Room-Temperature Direct Cu Semi-Additive Plating (SAP) Bonding for Chip-on-Wafer 3D Heterogenous Integration With μLED

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***Abstract*— This letter describes a direct Cu bonding technology to there-dimensionally integrate heterogeneous dielets based on a chip-on-wafer configuration. 100-μm-cubed blue μLEDs temporarily adhered on a photosensitive resin are interconnected by semi-additive plating (SAP) without thermal compression bonding. By using SAP bonding, a lot of dielets can be stacked on thin 3D-IC chiplets. The following three key technologies are applied to solve the yield issues of SAP bonding. After pick-and-place assembly, additional coplanarity enhancement eliminates Cu bridges grown to a small gap between the μLEDs and photosensitive resin. The μLEDs arrays with sidewalls insulated by room-temperature ozone-ethylene-radical (OER)-SiO_2-CVD are successfully bonded on sapphire wafers and a thin 3D-IC with through-Si via (TSV). Further design optimization is required, but partial seed pre-etching works well to increase the yield. Fully integrated module implementation with the 3D-ICs will be the next stage, however, we discuss a superior prospect for yield enhancement toward nearly 100%.**

***Index Terms*— Heterogeneous integration, 3D-IC, μLED, flexible hybrid electronics (FHE), direct bonding, chiplets.**

I. Introduction

HETEROGENEOUS integration studies have been started by monolithic stacking of III-V device on Si or GaAs wafers for optoelectronic applications [1]. Until the late 1990s, conventional heterogeneous integration had been limited to the fabrication of heterojunctions, e.g., GaAs/GaAlAs. Over the past two decades, flip-chip bonding technology with small chips has been widely used in industry, and heterogeneous integration research has been extended to other fields such as microelectromechanical systems (MEMS) [2] and sensors [3]. Meanwhile, heterogeneous integration works have been moving beyond 2D structures to 3D [4]. More recently, 3D-DRAM has been split into several high-bandwidth memory (HBM) and integrated with CPU. Such a heterogeneous integration architecture is increasingly used to three-dimensionally stack logic chips manufactured at different technology nodes [5].

Nowadays, these chips called chiplets are expected to be a promising driver to advance not only size scaling according to Moore's law but also performance scaling. Chiplets are Si intellectual property subsystems and do not simply indicate small chips divided from a large system on a chip. They are intended to be interconnected with advanced microelectronic packaging technologies such as redistributed layer (RDL), solder microbumps, and TSV to build complete functionality.

Based on fan-out wafer-level packaging (FOWLP), we have proposed "Smart Skin Display" as a flexible μ LED display with wearable vein viewers and sensors consisting of near-IR/red mini-LEDs and a 3D-IC chiplet array on which blue μ LEDs are stacked and interconnected with TSV [6]. We call the heterogeneous chiplets "dielets" that involve tiny dies, including optics, MEMS, and passives in addition to standard chiplets [7]. This FHE embedding the heterogeneous dielets can monitor vascular information as a predictor of blood clots etc., from the light emitted by the mini-LEDs. The reflected light from hemoglobin is detected with photodiodes designed in the 3D-IC dielets that process and transfer the resulting signals to LED drivers in the 3D-IC to drive the stacked μ LEDs.

μ LED displays have a serious interconnect issue. Thermocompression bonding is typically employed with Sn-series solders at $>250°C$. Low-temperature bonding technologies at $>150°C$ with low-melting-point solders [8] and anisotropic films/pastes (ACF/ACP) [9], [10] have been published. These elevated temperatures would cause significant residual stress and crucial alignment error. A fine-pitch room-temperature bonding has also been reported, but complicated chemical mechanical polishing is required [11]. In this letter, we demonstrate room-temperature μLED array stacking in a dielet-on-wafer/3D-IC configuration using SAP bonding. In addition, a yield enhancement strategy is dis-

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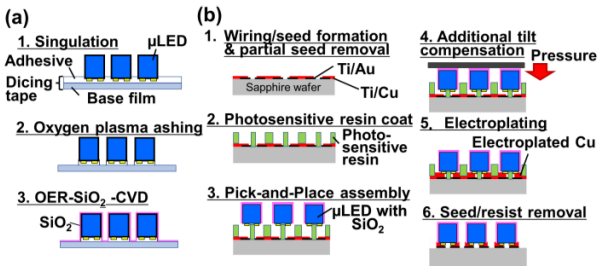

Fig. 1. A process flow of micro-LED sidewall insulation in tape-level processing (a) and SAP bonding (b).

cussed for this FOWLP-based flexible and 3D heterogeneous integration.

II. Fabrication

Fig. 1 shows the process flow of SAP bonding with incoming μLEDs. The 100-μm-square μLEDs have a 6-μm-thick active GaN layer and approximately 100-μm-thick sapphire substrate. The electrode size of the μLEDs is 25 $\times$ 75 μm^2 for both the anode and cathode, and the inter-electrode distance is 25 μm.

The μLEDs were attached to a dicing tape in a face-down fashion. First, the sidewalls of the μLEDs singulated by laser cutting were insulated with a 100-nm-thick SiO_2 deposited by room-temperature OER-SiO_2-CVD (Meiden Nanoprocess Innovation) [12] with tetraethoxysilane at the dicing-tape level. Since such blue tapes were composed of a glue layer and base film, the GaN layer was partially covered with the glue with a thickness of 10 μm. Before OER-SiO_2-CVD, an ashing process was added to fully expose the GaN sidewall. The glue layer surrounding the μLEDs was removed by O_2 plasma (300 W/10 min).

On the other hand, Ti/Au (15/500 nm) wirings were formed on host sapphire wafers by sputtering and standard photolithography with wet etching. Ti/Cu (15 /200 nm) as a seed layer was subsequently deposited on the wirings, and then, the seed layer was partially removed in 170-μm-long short lines to divide the p- and n-type Au electrodes of the μLEDs to be mounted. After that, a photosensitive resin was patterned on the seed layer to open the growth areas (each aperture area: 67.5 $\times$ 67.5 μm^2) for the following Cu electroplating called semi-additive process to interconnect the μLEDs with the wafers. The photosensitive resin also acted as a temporary adhesive to secure the μLEDs during the plating step. The 6 $\times$ 6 arrays of the μLEDs were arranged in a design with an inter-LED space of 200 μm, and the μLED arrays were further arrayed in 5 x 5 3D-IC blocks (inter-block space: 500 μm). The μLEDs were temporarily fixed at room temperature with a high-speed pick-and-place tool with a tacking force of 10 N for each, and then, an additional compressive force of 10 N was correctively applied using a wafer bonder (EV520, EVG) under an atmospheric pressure to compensate the LED tilt. The thicknesses of the photosensitive resin were 7 μm and 5μm before and after the compression processes. Cu pillars were grown by the electroplating process to give electrical connections with the corresponding Au electrodes on the μLEDs.

The electrical characteristics of the μLEDs were evaluated individually with a manual prober (Micro Support, Axis Pro APF) and semiconductor device parameter analyzer (Keysight, B1500). The assembly yield was given by observing the μLED positions with a digital microscope on the manual prober, the interconnect yield was judged by visual light emission from the μLEDs, and the bonding yield was determined by the I-V behaviors of the μLEDs. No decrease in current was the criterion for good bonding yield. The applied voltage of 3 V was basically employed to drive the μLEDs to exhibit blue emission.

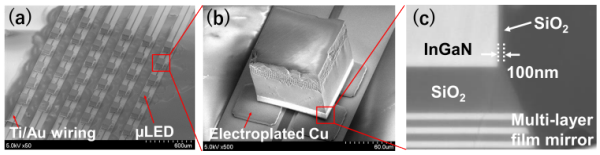

Fig. 2. SEM of a μLED array after SAP bonding (a), a magnified bonded μLED (b), and the cross-section of a μLED with sidewall insulation (c).

III. Results and Discussions

Fig. 2 shows SEM images of a μLED array after SAP bonding. The μLEDs are interconnected to Ti/Au wirings through electroplated Cu pillars. The alignment accuracies in XY directions are found to be $\pm$10 μm, and the maximum angular alignment error is 7°. The XY positional accuracies $\pm$10 μm are acceptable even with the worst angular error, considering that, for example, highly reliable results have been obtained for fine-pitch microbump interconnections with an inter-bump space of 5 μm [13]. The alignment errors would slightly increase DC resistance to drive the μLEDs through the Cu pillars. The increased DC resistance is added to on-resistance, but there is no significant positive shift in threshold voltages (V_{TH}). This alignment errors seem not to be related to SAP bonding failures described below. Thus, the assembly (alignment) yield can be said to be 100%.

However, the yield of interconnection is 63% in the first bonding trial with a conventional process listed at the top of Fig. 3(a). Three blocks of each 6 $\times$ 6 μLED array are extracted, and whether the μLEDs emit blue light is mapped. The bottom of Fig. 3(a) shows the interconnect yield of the μLEDs bonded under current conditions used in this study where three key technologies, 1) μLED sidewall insulation, 2) additional tilt compensation, and 3) partial seed pre-etching, are used to enhance the yield. The interconnect yield eventually increases up to 92% with the new process.

The sidewall insulation of the μLEDs prevents the active GaN layer from electrical short with excess growth of electroplated Cu. When μLEDs without sidewall insulation are bonded, the electroplated Cu, once it reaches the Au electrodes of the μLEDs, is further grown from the GaN sidewall. However, low-temperature processes are required for sidewall protection after the singulation process. Typically, the glue layers of dicing tapes are not thermally stable. Therefore, room-temperature OER-SiO_2-CVD is employed to enhance the interconnect yield with the good quality of SiO_2 [12]. Additional compressive force after chip placement eliminates a small gap between the photosensitive resin and tilted μLEDs, preventing the generation of Cu bridges connecting the p- and n-type Au electrodes. The coplanarity of the tilted μLEDs is also improved. Furthermore, it is difficult to promptly etch the seed layer at the hidden parts underneath the μLEDs. The partial pre-etching of the Cu seed before μLED placement reduces the defects derived from excess Cu pillar undercut/thinning in the seed removal step after SAP bonding.

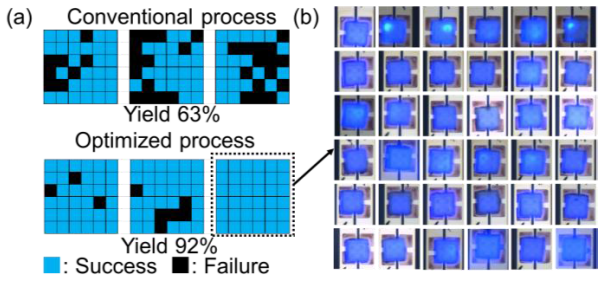

Fig. 3. Yield comparison before/after process optimization (a), and the photo of a μLED array emitting light (b).

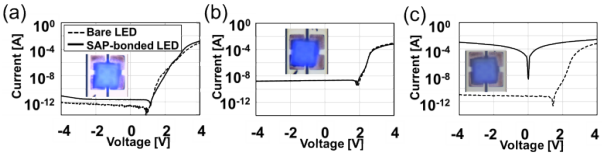

Fig. 4. I-V characteristics of intense-emission (a), weaker-emission (b), and weakest-emission (c) μLEDs before and after SAP bonding.

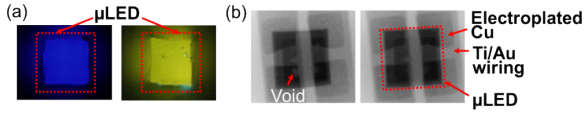

Fig. 5. Fluorescence microscope (a) and X-ray transmission (b) images of intense-emission (left) and weakest-emission (right) μLEDs.

Fig. 3(b) shows the optical microscope images of emitting blue light from the μLEDs taken during I-V measurement. The 6 $\times$ 6 μLED array block is picked up from the bottom right in Fig. 3(a). All the μLEDs emit blue light, although there are variations in electroluminescence intensity.

The I-V characteristics of the μLEDs after SAP bonding are shown in Fig. 4, where the I-V behaviors are mainly classified into three categories. The representative I-V curves of the three μLEDs are exhibited with inset microscope images. Figs. 4(a) and (b) show the I-V characteristics of the 1^{st} and 2^{nd} μLEDs with excellent and relatively lower electroluminescence intensity. The 2^{nd} μLED gives one orders of magnitude lower intensity than the 1^{st} μLED when the voltage is increased up to 3 V. However, they are at a similar level as the pristine μLED dies before SAP bonding. Therefore, the difference in the intensity of the μLEDs between Figs. 4(a) and (b) is due to initial characteristics variation resulting from LED wafer fabrication processes, not due to the impact of SAP bonding. Here, we skipped the wafer test step for known good die selection to make their luminescence intensity uniform. The current flowing to the negative voltage region is the same level as the 1^{st} μLED, which means there is no leakage. On the other hand, Fig. 4(c) shows the I-V curve of the 3^{rd} μLED having considerably low emission intensity. The current is not sufficiently running.

As seen in Fig. 5(a), the image taken by a fluorescence microscope exhibits dark emission from the 3^{rd} μLED. The emission intensity of the 1^{st} and 3^{rd} μLEDs are compared using X-ray transmission images, as shown in Fig. 5(b). Small voids are observed in an intense-emission μLEDs, but there is no resistance increase to positively shift the V_{TH}. In contrast, no voids are observed when the weakest-emission μLEDs are taken. The reason why the emission of the 3^{rd} μLED is extremely low is thought to be small leakage at the pre-etch parts, as mentioned below.

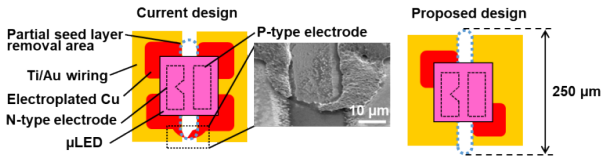

Fig. 6. SEM image of an inter-pillar bridge formed at the interface be-tween the photosensitive resin and wafer, and current (left) and proposed (right) aperture/pre-etch seed designs.

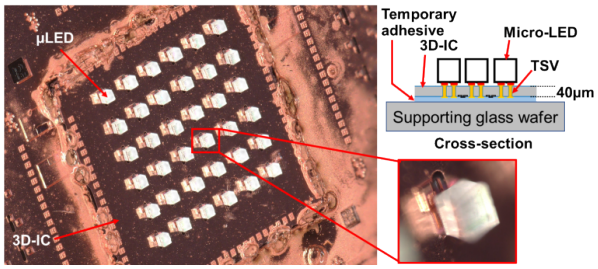

Fig. 7. A photomicrograph of μLEDs stacked on a thin 3D-IC dielet after SAP bonding.

The main reason for the other non-emission μLEDs is discussed. As shown in Fig. 6, another Cu bridge extending over the sapphire wafer is observed at the failure μLED sidewall along partial seed pre-etching patterns. The emission failure is attributed to the adhesion between the photosensitive resin and the underneath sapphire wafers: these parts are exposed after partial seed pre-etching. This pre-etch pattern should be extended to several tens of micrometers in a longitudinal direction in the next optimized design for heterogeneous integration with 3D-ICs. In addition, the bridge and short problems would be solved by designing the inter-aperture spacing formed with the photosensitive resin. The average shear bonding strength of SAP bonding μLEDs was 4 MPa by a bond tester (DAGE 4000 Plus). Reducing the number of bond pads will lower the mechanical strength, but the bondability is expected to be further enhanced by underfilling. The reason why the 3^{rd} μLED shows insufficient emission is also probably due to this structure likely to be bridged at the pre-etch parts. The SAP bonding yield, excluding the weak-emission μLEDs, is 75%.

The bonding yield still has issues, however, this low temperature dielet-on-wafer stacking approach is demonstrated with a 40-μm-thick 3D-IC dielet fabricated using the die-level 3D integration methodology [14] with 2.5-mm-square split dies produced by a 180-nm-node COMS technology in a TSMC shuttle service. The dies consist of photodiodes and LED drivers. As shown in Fig. 7, the 6 $\times$ 6 μLED dielets are successfully assembled on the thin and brittle 3D-IC having TSV without mechanical damage such as microcracks.

IV. Conclusion

We developed a room-temperature direct Cu interconnect technology "SAP bonding" to heterogeneously integrate tiny dies with 3D-ICs. μLED arrays were emitted on sapphire wafers using a dielet-on-wafer 3D integration, and 6 $\times$ 6 μLEDs were stacked on a thin 3D-IC without mechanical failure. OER-SiO_2-CVD and partial seed pre-etching were very effective to increase the interconnect yield, but the design should be further optimized in the next 3D heterogeneous integration with thinned 3D-IC arrays with TSV.

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