A Self-Refresh Memory-in-Pixel for Low-Power Reflective Liquid Crystal Displays

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***Abstract*— In this letter, we propose a self-refresh multi-level memory-in-pixel circuit for reflective low-power liquid crystal displays comprising oxide thin film transistors. In the absence of image update, dynamic power consumption can be minimized by integrating memory cell. The memory cell comprises only two transistors and one capacitor, which are suitable for high-resolution displays. Measurement results verify that the proposed circuit achieves 3-bit grayscale display operating at 1 Hz. Moreover, the proposed circuit consumes only 1.72 % of dynamic power compared to the conventional one. Thus, the proposed circuit is expected to simultaneously achieve high performance and low power consumption.**

***Index Terms*— Low power display, memory-in-pixel (MIP), Oxide thin film transistor (TFT), self-refresh.**

I. Introduction

IN RECENT years, there has been high demand for low-power displays. Memory-in-pixel (MIP) circuits have been studied for low-power reflective liquid-crystal displays (LCDs) [1], [2], [3], [4], [5], [6], [7], [8]. By integrating the memory into pixel circuits, the dynamic power dissipated for refreshing images can be minimized when there is no image update.

Two types of memory are used in MIP circuits: static and dynamic. Since static-type memory can maintain pixel voltage without refreshing, it has low power consumption [1], [2], [3]. However, it has a low aperture ratio owing to its complex structure and large area per unit of memory cell. Thus, static-type memory is not suitable for high-resolution displays. In contrast, dynamic-type memory has a simpler structure than static memory [4], [5], [6]. Therefore, it has the advantage of high-resolution displays compared with the static type.

Generally, the area-ratio variation method is adopted to increase color depth by configuring multiple memory cells in a pixel [7], [8]. However, the method reduces the aperture ratio because a single pixel requires multiple subpixels. Thus, there have also been attempts to achieve multiple levels in a unit memory cell [5], [6].

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Recently, oxide thin-film transistors (TFTs) and low-temperature polycrystalline silicon and oxide (LTPO) TFTs have been intensively studied [9], [10]. Several studies have used oxide or LTPO TFTs in MIP circuits [11], [12], [13], [14]. Owing to the ultralow leakage current characteristics of oxide TFTs, the refresh rate of the dynamic-type MIP was lowered. In a previous study, we proposed multi-level MIP circuits comprising LTPO TFTs [14]. However, the fabrication process of LTPO TFTs is complex and expensive, and has poor uniformity.

In this letter, we propose a new multi-level MIP circuit for low-power reflective LCDs comprising only oxide TFTs. The memory cell was simplified by half compared with the previous circuit while maintaining the same bit depth.

II. Proposed Circuit

Fig. 1(a) shows the circuit diagram of the proposed MIP circuit. A unit pixel comprises two transistors and one capacitor. M1 represents a programming transistor used to program a data voltage to the gate node of driving transistor M2. A storage capacitor is connected to the gate node of M2. M2 can be indirectly controlled by a capacitor connected to its gate node. As illustrated in Fig. 1(a), we assumed the combination of a driving transistor and capacitor as a single transistor (T_{Memory}). Subsequently, the threshold voltage (V_{TH}) of T_{Memory} can be modulated by the programmed data voltage because the programmed voltage affected the electric field applied to the gate node of M2. For instance, as depicted in Fig. 1(a), the larger the stored positive voltage, the lower the V_{TH} becomes. Fig. 1(b) illustrates a timing diagram of the proposed MIP circuit. The detailed operating principle is described as follows:

A. Programming Period

The data voltages are programmed in pixels during the programming period (T_{PRG}).

B. Refresh Period

During the refresh period (T_{RF}), all pixels are refreshed simultaneously according to the data voltage programmed in T_{PRG}. Fig. 2 illustrates an example of the refresh scheme of the proposed circuit. Different data voltages are stored in pixels [A] and [B]. As shown in Fig. 2, the threshold voltages of the two T_{Memory} were different. V_{RF} and V_{PXL} are global signal lines connected to the gate and source of T_{Memory}, respectively. They were simultaneously applied to all pixels in the stepped waveforms. The V_{GS} of T_{Memory} decreases step by step. During (T1), the V_{GS} of T_{Memory} is sufficiently high to turn on both driving transistors. Therefore, both pixels [A] and [B] follow V_{PXL} voltage. During (T2), only pixel [B]

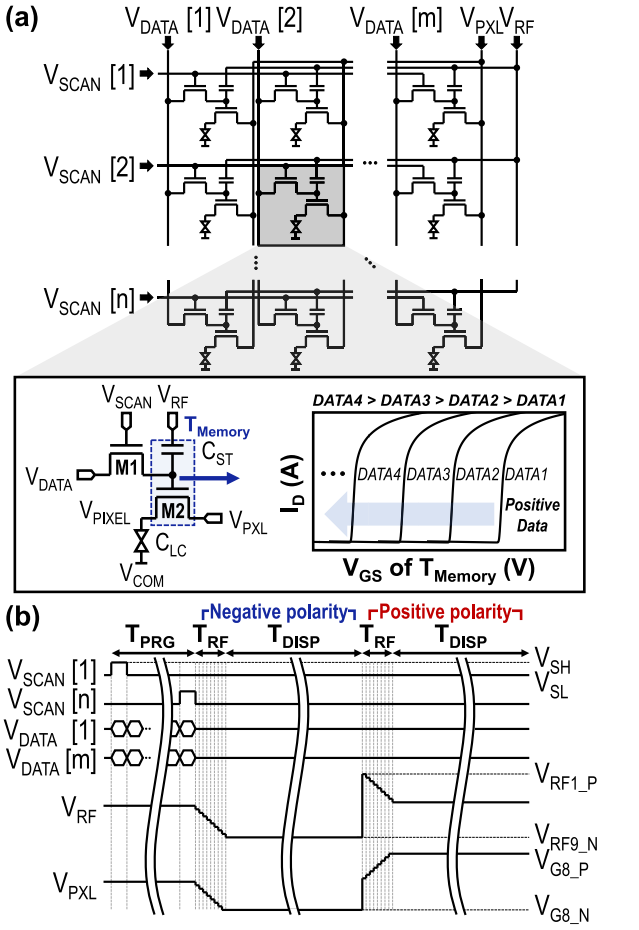

Fig. 1. (a) Circuit diagram and (b) timing diagram of the proposed multi-level MIP circuit.

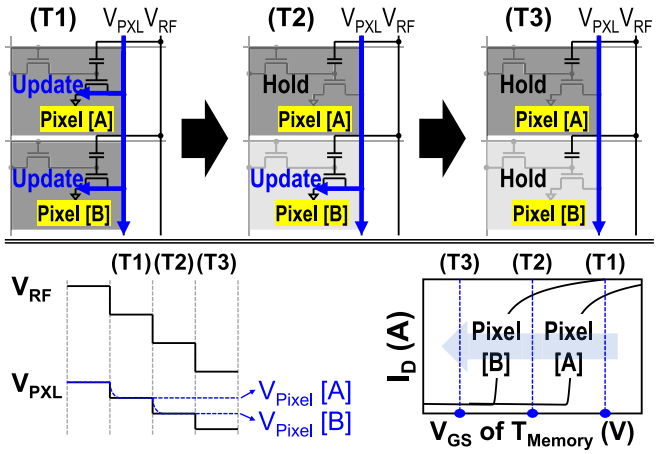

Fig. 2. An example of the refresh scheme of the proposed MIP circuit.

is updated, and pixel [A] holds the voltage charged in the previous step. During (T3), both pixels [A] and [B] are not updated. Accordingly, depending on the programmed data voltage, all pixels can be simultaneously self-refreshed using the proposed refreshed scheme.

C. Display Period

During the display period (T_{DISP}), pixel voltages are retained. At the end of T_{DISP}, they are inverted to opposite polarities to prevent image-sticking [15], [16]. The proposed

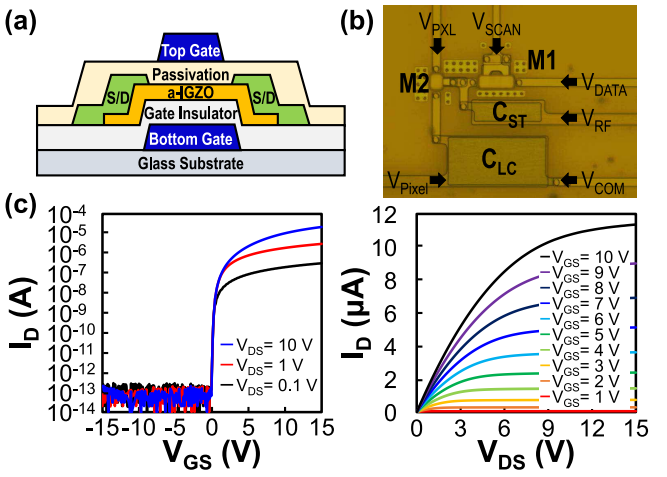

Fig. 3. (a) Cross-section view of fabricated oxide TFT. (b) Micrograph of the fabricated circuit. (c) Transfer and output characteristics of the driving transistor M2 (W/L = 4 μm / 6 μm).

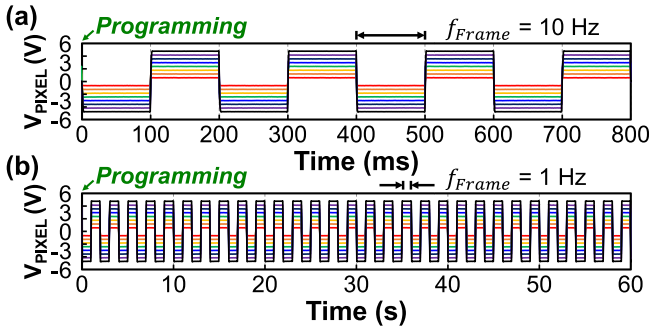

Fig. 4. Measurement results of eight gray levels, driving at (a) 10 Hz and (b) 1 Hz.

circuit repeats the self-refresh operation without additional programming until an image update is required. Both the scan driver and data driver can be idle because there is no need to program the data voltage. Instead, dynamic power is consumed in the global signal lines (V_{RF}, V_{PXL}) for self-refresh because all pixels are refreshed simultaneously, and not line-by-line. Consequently, the driving frequency is significantly lowered. Therefore, it consumes less dynamic power than conventional refresh methods [14].

III. Results and Discussion

We fabricated the proposed circuit to verify its feasibility. Fig. 3(a) displays a cross-sectional view of the fabricated oxide TFT. A dual-gate structure was applied to TFTs to achieve high carrier mobility and low subthreshold swing [17]. Both gates are connected and driven together. Fig. 3(b) shows a micrograph of the fabricated circuit. The widths of M1 and M2 are both 4 μm, and the lengths of M1 and M2 are 12 μm and 6 μm, respectively. C_{ST} and C_{LC} are 300 fF and 1 pF, respectively. Fig. 3(c) presents the transfer and output characteristics of the driving transistor M2 (W/L = 4 μm/ 6 μm).

Fig. 4 illustrates the measurement results of eight gray levels driving at 10 Hz and 1 Hz, respectively. V_{SH} and V_{SL} are +10 and −20 V, respectively. Analog voltages for eight gray levels, V_{G1}-V_{G8}, are ±0.6 V, ±1.2 V, ±1.8 V, ±2.4 V, ±3.0 V, ±3.6 V, ±4.2 V, and ±4.8 V. As shown in Fig. 4(b), owing to the low leakage current of oxide TFTs, the pixel

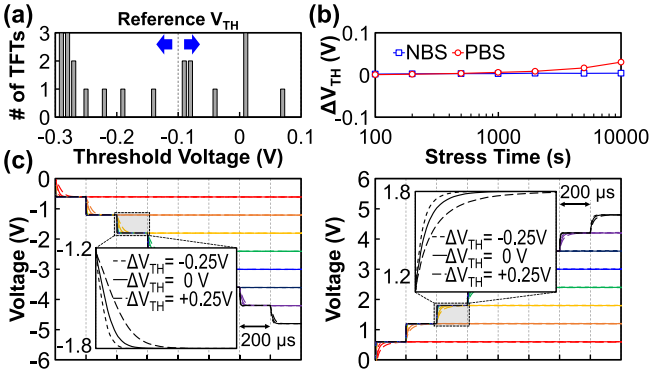

Fig. 5. (a) VTH distribution over the fabricated 21 TFTs, (b) negative and positive bias stress test results of M2 (W/L = 4 μm / 6 μm) for 10,000 s, and (c) simulation results of pixel voltages with V_{TH} variation of ±0.25 V.

refresh frequency could be reduced to 1 Hz, and self-refresh was repeated for 1 min without additional programming.

This novel driving scheme depends on the characteristics of the driving TFT (M2). Therefore, as shown in Fig. 5(a) and 5(b), we investigated possible V_{TH} variation. Fig. 5 (a) shows the V_{TH} distribution of the fabricated TFTs. The maximum difference of V_{TH} among 21 TFTs were 0.36 V. Fig. 5(b) shows V_{TH} shifts of M2 (W/L = 4 μm / 6 μm) caused by bias stresses. A negative bias stress (NBS) test was conducted at $V_{GS} = -15$ V and $V_{DS} = 5$ V, and a positive bias stress (PBS) test was conducted at $V_{GS} = 10$ V and $V_{DS} = 0$ V. The bias stress conditions reflect the worst driving case of the proposed circuit. V_{TH} shifted by 0.004 V in the NBS and 0.031 V in the PBS after 10,000 s of bias stress. The bias stresses were continuously applied to the transistors during the stress tests; however, in practice, the negative and positive biases are alternately applied to M2. Thus, we expect that there is much less effect on V_{TH} owing to the recovery characteristics of the AC bias stress [18], [19], [20]. Given these variations, we determined the interval of the data voltages, including the voltage margin. Fig. 5(c) illustrates the simulation results for pixel voltages. The reference V_{TH} was set to −0.1 V with the variation of by ±0.25 V, as shown in Fig. 5(a). As demonstrated in Fig. 5(c), the pixel voltages reached the target voltage during one step of $T_{RF} = 200$ μs without distortion. This shows that our proposed architecture is highly robust to a large V_{TH} variation of ±0.25 V.

We investigated the dynamic power consumption of the conventional 1T1C and our previous architectures [14]. We assumed that a full-white pattern is displayed on the screen for calculation. In addition, we assumed the following. First, the resolution of the display is FHD (1920 × 1080). Second, the LCD is normally-black mode. Third, the display adopts a dot inversion method. The dynamic power consumption of the conventional LCD ($P_{Dyn,C}$) and proposed LCD ($P_{Dyn,P}$) can be expressed as follows:

$$\begin{aligned} P_{Dyn,C} &= P_{CL} + P_{Pixel} \\ &= (C_{CL} \cdot N_H \cdot 3) \cdot (V_{W,P} - V_{W,N})^2 \cdot (N_V \cdot f_{Frame}/2) \\ &\quad + (C_{LC} \cdot N_H \cdot 3 \cdot N_V) \cdot (V_{W,P} - V_{W,N})^2 \\ &\quad \cdot (f_{Frame}/2) \qquad (1) \\ P_{Dyn,P} &= P_{RF} + P_{PXL} + P_{Pixel} \\ &= (C_{RF} \cdot N_H \cdot 3) \cdot (V_{RF1,P} - V_{RF9,N})^2 \cdot (f_{Frame}/2) \\ &\quad + (C_{PXL} \cdot N_H \cdot 3) \cdot (V_{W,P} - V_{W,N})^2 \cdot (f_{Frame}/2) \\ &\quad + (C_{LC} \cdot N_H \cdot 3 \cdot N_V) \cdot (V_{W,P} - V_{W,N})^2 \\ &\quad \cdot (f_{Frame}/2) \qquad (2) \end{aligned}$$

where P_{CL}, P_{RF} and P_{PXL} represent the powers consumed by the column, V_{RF}, and V_{PXL} lines, respectively. C_{CL}, C_{RF}, C_{PXL}, and C_{LC} represent the capacitances of the column line, V_{PXL} line, V_{RF} line, and pixel, respectively. N_H and N_V represent the horizontal and vertical resolutions, respectively. V_W and V_{RF} denote the pixel voltages for the white level and the refresh voltage, respectively. $V_{RF1,P}$ and $V_{RF9,N}$ are shown in Fig. 1. Note that the subscripts N and P refer to the negative and positive polarities, respectively. Moreover, f_{Frame} indicates the frame frequency. We assume that C_{LC}, C_{CL}, C_{RF}, and C_{PXL} are 1, 100, 200, and 200 pF, respectively.

TABLE I
COMPARISON OF DYNAMIC POWER CONSUMPTION

		Conventional 1T1C	Previous work [14]	This work
Frame frequency	60 Hz	1.74 W	25.70 mW	29.91 mW
	1 Hz	28.95 mW	Not applicable	0.50 mW

TABLE II
COMPARISON OF PROPOSED CIRCUIT WITH OTHER WORKS

	[5]	[6]	[14]	This work
Process	LTPS	LTPS	LTPO	Oxide
Structure	5T2C	7T1C	4T2C	2T1C
Bit-depth	2-bit	2-bit	3-bit	3-bit
Frame frequency	60 Hz	60 Hz	60 Hz	1 Hz

Table I lists the dynamic power consumption at the two frame frequencies. The dynamic power consumption of the proposed circuit was reduced to 1.72 % of that of the conventional circuit when the frame frequencies were the same. Since the data voltage must be changed line-by-line in the conventional LCD, the driving frequency of the column signals is N_V times higher than that of V_{PXL} and V_{RF}. It is reduced to 1.94 % of the previous value because the frame frequency can be lowered from 60 Hz to 1 Hz.

Table II presents a comparison between the proposed circuit and reported dynamic-type MIP circuits. The latest MIP architecture [14] represents the highest bit depth with the simplest structure. However, it is fabricated using the LTPO process, which is complex and expensive, and has poor uniformity. In contrast, the proposed architecture was fabricated using only the oxide TFTs. Therefore, the memory cells were simplified by half while maintaining the same bit depth. Moreover, it was possible to lower the frame frequency from 60 Hz to 1 Hz, primarily owing to the low leakage current of the oxide TFT. The proposed architecture is promising to be used in large-sized displays because the oxide TFT process costs less and has better uniformity than LTPS and LTPO.

IV. CONCLUSION

In this letter, we propose a new MIP circuit for low-power reflective LCDs comprising only oxide TFTs. A 3-bit grayscale was achieved using the simplest structure among reported MIP circuits. Furthermore, the frame frequency was lowered to 1 Hz, owing to the low leakage current of the oxide TFT. We expect that the proposed circuit can simultaneously achieve high performance and low power consumption.

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