AlScN/GaN HEMTs Grown by Metal-Organic Chemical Vapor Deposition With 8.4 W/mm Output Power and 48 % Power-Added Efficiency at 30 GHz

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***Abstract*— We report on DC and RF measurement results of AlScN/GaN high electron mobility transistors (HEMTs) grown by metal-organic chemical vapor deposition (MOCVD). Comparing the properties with those of a wafer grown with the same MOCVD tool but featuring an AlGaN barrier, the sheet carrier density (n_s) of 1.50 × 10^{13} cm^{-2} measured on the AlScN/GaN wafer is around 60 % higher. This translates to a power density (P_{out}) of 8.4 W/mm at a frequency of 30 GHz and a drain bias of 30 V. Also, a high power-added efficiency (PAE) of 48.9% and 46.1% is reached, when biased at 25 V and 30 V, respectively. These early results illustrate the great potential AlScN/GaN devices carry for improving on the achievable output power on device level at millimeter-wave (mmWave) frequencies.**

***Index Terms*— AlScN, ScAlN, GaN, MOCVD, HEMTs, millimeter-wave, Ka-band, small-signal, large-signal, dispersion.**

I. Introduction

NEXT-generation wireless communication networks will make use of millimeter-wave (mmWave) range frequency bands with the intent of boosting data rates. However, due to the matching-bandwidth limitations of electronic devices, the Bode-Fano limit [1], challenges in the design of RF components, in terms of efficiency, output power, and linearity arise. Certain distributed power amplifier (PA) topologies can exceed this limit, e.g. traveling-wave amplifiers (TWAs) [2], [3], [4], [5] and non-uniform distributed power amplifiers (NDPAs) [6], [7], [8]. Still, the obtained efficiency levels are lower than those typically reached with reactively-matched PAs [9], [10], [11], [12].

Whereas the Bode-Fano limit can be improved by supply-voltage reduction, this also limits the achievable output power. Raising both, Bode-Fano limit and output power, can be achieved by providing a higher saturation drain current density ($I_{D,sat}$), which can be expressed as $I_{D,sat} = e\ n_s\ v_{eff}$, where e, n_s and v_{eff} are the elementary charge, sheet carrier density and effective velocity of electrons, respectively [13]. Consequently, $I_{D,sat}$ can be increased by either raising n_s or v_{eff}. At high electric fields, however, v_{eff} is close to the saturation drift velocity (v_{sat}), rendering it impossible to substantially improve on that. Instead, increasing n_s can be accomplished by engineering the hetero junction accordingly.

Due to the high polarization charge in AlScN/GaN heterostructures, n_s can become as high as 5 × 10^{13} cm^{-2} [14], [15], which is around a factor of four greater than what has been reported for single-channel AlGaN/GaN structures [16], [17]. Values up to 5.2 × 10^{13} cm^{-2} have so far only been shown for vertically stacked multi-channel AlGaN/GaN heterostructures [18]. Besides, the ability to grow a lattice-matched AlScN barrier on GaN prevents excessive strain in the films, promising enhanced reliability [19].

Encouraging results of AlScN/GaN and AlGaScN/GaN high electron mobility transistors (HEMTs) grown by molecular beam epitaxy (MBE) have been published [20], [21], [22], [23]. Commercialization of Sc-based HEMT technologies is certainly difficult when relying on MBE growth, due to slow growth rates, low growth yields and high cost of operation. In contrast, growth by means of metal-organic chemical vapor deposition (MOCVD) would allow to greatly boost manufacturability.

We report on DC and RF performance of MOCVD-grown AlScN/GaN HEMTs. For reference, also data of a AlGaN/GaN wafer, grown with the same MOCVD tool, is given.

II. Epitaxial Growth and Device Fabrication

Epitaxial growth of the AlGaN/GaN and AlScN/GaN stacks was performed in house using the same MOCVD tool. First,

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a thin AlN nucleation layer is grown on top of a 100-mm semi-insulating 4H-SiC substrate, followed by an Fe-doped GaN buffer and n.i.d. GaN channel. For the baseline stack, a 14-nm-thick $Al_{0.31}Ga_{0.69}N$ barrier and 4 nm of GaN cap are subsequently grown. The layer thicknesses and stoichiometric compositions were verified by high-resolution X-ray diffraction (HRXRD) measurements and subsequent model fitting. For the wafer with Sc-based barrier, a different layer stack has been used. On top of the identical GaN buffer and channel layer stack, an AlN interlayer with a nominal thickness of 0.7 nm is deposited before the growth of an 8.5-nm-thick AlScN barrier which is capped with 8 nm of in-situ SiN_x. The choice of the capping layer is based on findings from earlier growth experiments showing a non-coalescent cap when using GaN on top of an AlScN barrier [24]. In comparison to previous publications [24], [25], [26], a different precursor with higher vapor pressure was used. This enabled a substantially higher growth rate to be obtained which also translated to a better surface morphology and higher mobility (μ) over a wider range of growth temperatures [27].

Examining the exact composition of the AlScN barrier as well as the determination of its thickness is challenging and not as straight forward as for AlGaN barriers. This is due to the indistinct interfaces and Sc gradients that typically occur during MOCVD growth of AlScN [24]. A best possible determination of the thickness, including the AlN interlayer and the amorphous SiN_x cap layer was achieved from a combination of HRXRD and X-ray reflectivity (XRR). Moreover, the HRXRD reciprocal space mapping shows that AlN interlayer and barrier are grown fully strained on GaN. The average Sc composition of the barrier was determined by secondary-ion mass spectrometry (SIMS) and amounts to 5 %.

Device processing for both wafers was identical and incorporated an advanced version of our *GaN15* 0.15-μm GaN-on-SiC technology. First, ohmic contacts were formed using Si implantation underneath the subsequently deposited ohmic metal stack, followed by an annealing step. For the AlScN/GaN wafer a dry etch is performed beforehand for complete removal of the in-situ SiN_x. After deposition of a Si-rich SiN_x film, the 0.15-μm gate openings are defined by e-beam lithography before optically defining the dimensions of the asymmetrical gate head with integrated gate field plate. Pt-Au gates are then evaporated to define the Schottky contacts, followed by a gate-head passivation and formation of the source-terminated field plates. The dual-field-plate configuration allows for enhanced field control on the drain side, leading to an increased breakdown voltage [28]. The Gate-to-source and gate-to-drain spacings are 0.7 μm and 1.2 μm, respectively.

III. Static and Pulsed DC Measurement Results

Median ohmic contact resistance was 0.90 Ω · mm and 0.25 Ω · mm for the AlScN/GaN and AlGaN/GaN wafer, respectively. Clearly, the contact resistance of the wafer with Sc-based barrier is higher than desired. Si implantation has proven to form low-resistance contacts, also when employing AlN barriers [29]. However, the AlN layers have been considerably thinner, in the range of 3 nm to 5 nm, than the AlScN barrier used in this work. Alternative processes might yield better results for thick Al-rich barriers, e.g. ohmic recess and regrowth of n^+ GaN [20], [22].

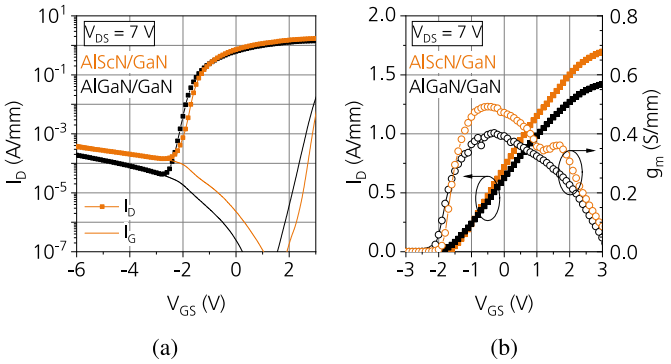

Fig. 1. (a) Semi-log IV curves and (b) DC transfer characteristics of 6 × 50-μm AlScN/GaN and AlGaN/GaN HEMTs, measured at $V_{DS} = 7$ V.

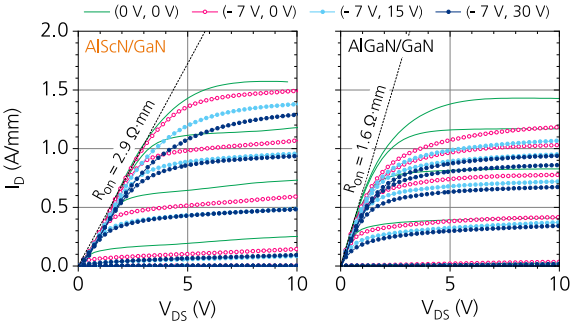

Fig. 2. Pulsed DC-IV data of 2 × 25-μm AlScN/GaN and AlGaN/GaN HEMTs, measured with a pulse width of 1 μs and a duty cycle of 0.1%, respectively. The devices were measured for V_{GS} ranging from −5 V to 2 V in steps of 1 V.

Hall data of the fully SiN_x-passivated wafers reveal an n_s of 1.50 × 10^{13} cm^{-2} and 0.93 × 10^{13} cm^{-2} and a (μ) of 920 $cm^2/(V \cdot s)$ and 1660 $cm^2/(V \cdot s)$, for the AlScN/GaN and AlGaN/GaN wafers, respectively. Despite a 60 % higher n_s, the lower μ of the AlScN/GaN wafer leads to a higher sheet resistance (R_{sh}) of 452 Ω/sq than the 405 Ω/sq obtained for the wafer with AlGaN barrier.

Fig. 1 shows DC transfer characteristics of 6 × 50-μm devices, measured at a drain-source voltage (V_{DS}) of 7 V. $I_{D,sat}$ of the AlScN/GaN device measures to 1.7 A/mm, extracted at a gate-source voltage (V_{GS}) of 3 V. This is around 20 % higher than the 1.4 A/mm achieved on the AlGaN/GaN epi stack. The difference in $I_{D,sat}$ is notably smaller than that in n_s, which can be attributed to the roughly three-times higher ohmic contact resistance for the AlScN/GaN wafer. Still, the transconductance (g_m) for the AlScN/GaN device peaks at 490 mS/mm, whereas the AlGaN/GaN device shows a lower maximum g_m of 400 mS/mm. Hard off-state breakdown occurs at 75 V for the AlScN/GaN and 95 V for the AlGaN/GaN wafer. The ScAlN/GaN devices show a sudden onset of buffer leakage current at a gate-drain voltage (V_{GD}) of around 30 V, which stays constant up to the breakdown voltage. The origin of this is not fully understood, yet. Though, we believe that ensuring a better carrier confinement, e.g. by reducing the GaN channel thickness, can help to eliminate that.

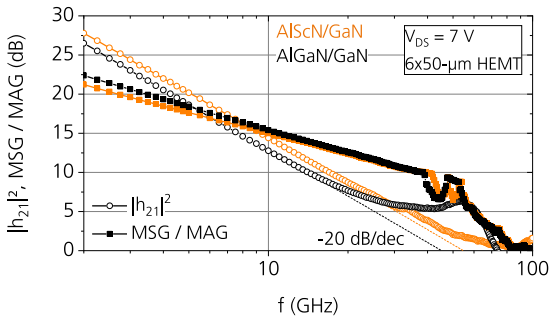

Fig. 3. Current gain as well as maximum stable and available gain of 6 × 50-μm AlScN/GaN and AlGaN/GaN HEMTs, measured at V_{DS} = 7 V with V_{GS} set for maximum g_m.

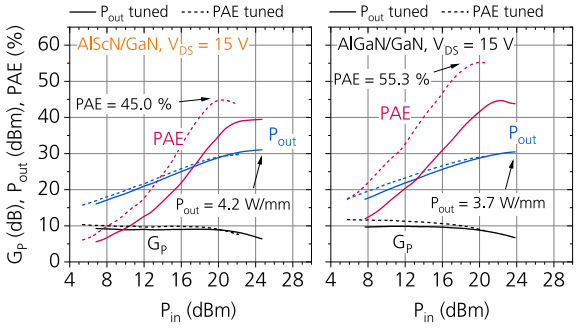

Fig. 4. 30-GHz CW load pull of 6 × 50-μm AlScN/GaN and AlGaN/GaN devices at a V_{DS} of 15 V, given for optimal P_{out} as well as PAE tuning.

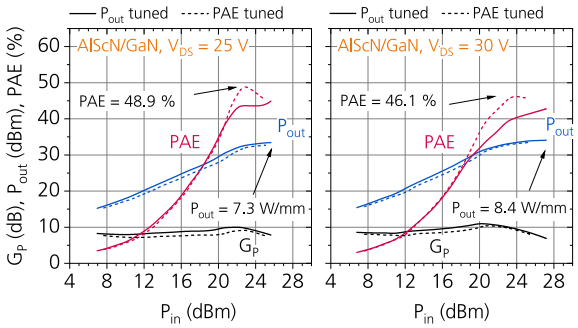

Fig. 5. 30-GHz CW load pull of a 6 × 50-μm AlScN/GaN device at a V_{DS} of 25 V and 30 V, given for optimal P_{out} as well as PAE tuning.

Fig. 2 shows pulsed DC performance (1 μs pulse width, 0.1 % duty cycle) for 2 × 25-μm devices from both wafers. V_{GS} was swept from −5 V to 2 V in steps of 1 V. Again, the AlScN/GaN device shows a higher pulsed $I_{D,sat}$ than the AlGaN/GaN device for the (0 V, 0 V) condition as well as lower gate and drain lag. The total current collapse, when extracted at V_{DS} = 5 V, amounts to 17 % and 29 % at (−7 V, 15 V) and to 25 % and 37 % at (−7 V, 30 V) for the AlScN/GaN and AlGaN/GaN device, respectively. As stated before, the AlScN/GaN wafer features a higher ohmic contact resistance than the AlGaN/GaN one. This is also seen in the on-resistance (R_{on}) of 2.9 Ω · mm, whereas the device from the baseline AlGaN/GaN wafer features a low R_{on} of 1.6 Ω · mm.

IV. RF Measurement Results

A. Small-Signal Measurement Results

Small-signal performance of 6 × 50-μm AlScN/GaN and AlGaN/GaN HEMTs is given in Fig. 3, respectively. The devices were biased for maximum g_m at a V_{DS} of 7 V. When fitting a 20-dB/dec slope to the measured current gain ($|h_{21}|^2$), a transition frequency (f_T) of 52 GHz and 45 GHz is obtained for the AlScN/GaN and AlGaN/GaN device, respectively. Despite the low drain bias, both devices reach a maximum stable gain (MSG) of 10 dB at 40 GHz.

B. Load Pull Measurement Results

Class-AB Continuous-wave (CW) power performance at 30 GHz was evaluated by active load pull. Fig. 4 shows the performance for optimal power density (P_{out}) tuning as well as the tuning yielding maximum power-added efficiency (PAE) of 6 × 50-μm devices from both wafers. The quiescent drain current was 125 mA/mm for the AlScN/GaN and 35 mA/mm for the AlGaN/GaN device.

The AlScN/GaN device shows a roughly 15-% higher P_{out} than the device from the AlGaN/GaN wafer, reaching 4.2 W/mm at 3 dB of power gain (G_P) compression. However, at 55.3 % an around ten-percentage-points higher PAE is reached for the AlGaN/GaN device due to the lower R_{on}.

Further measurements of the AlScN/GaN device, as given in Fig. 5, show a P_{out} of 7.4 W/mm and 8.4 W/mm with an associated PAE of 44.3 % and 42.0 %, when biased at 25 V and 30 V, respectively. With a 25 V bias applied the PAE tops out at 48.9 % for a P_{out} of 5.0 W/mm, whereas at 30 V a maximum PAE of 46.1 % at a P_{out} of 6.7 W/mm is achieved. The performance is close to best reported results of Ga-polar devices in terms of P_{out} and PAE at 30 GHz [17], [30], [31], [32], [33]. Although, individually better performance in terms of P_{out} and PAE has been achieved by other groups, the combination of a P_{out} of 8.4 W/mm and a PAE of 42.0 % is the highest reported to date for Ga-polar devices, operated in CW at or below 30 V at Ka-band frequencies.

V. Conclusion

We reported on DC and mmWave RF performance results of MOCVD-grown AlScN/GaN HEMTs. For reference, the results were benchmarked against an AlGaN/GaN wafer, grown in the same MOCVD tool. In comparison, the AlScN/GaN devices featured a higher $I_{D,sat}$ at 1.7 A/mm than the AlGaN/GaN one. Large-signal performance at 30 GHz is well comparable with that of the best reported Ga-polar devices, reaching a PAE of 48.9 % and a P_{out} of 8.4 W/mm at a V_{DS} of 25 V and 30 V, respectively.

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References

[1] R. M. Fano, “Theoretical limitations on the broadband matching of arbitrary impedances,” Massachusetts Inst. Technol., Res. Lab. Electron., Cambridge, MA, USA, Tech. Rep. 41, 1948.

[2] F. Thome and A. Leuther, "First demonstration of distributed amplifier MMICs with more than 300-GHz bandwidth," *IEEE J. Solid-State Circuits*, vol. 56, no. 9, pp. 2647–2655, Sep. 2021, doi: 10.1109/JSSC.2021.3052952.

[3] T. Jyo, M. Nagatani, M. Ida, M. Mutoh, H. Wakita, N. Terao, and H. Nosaka, "A 241-GHz-bandwidth distributed amplifier with 10-dBm P1dB in 0.25-μm InP DHBT technology," in *IEEE MTT-S Int. Microw. Symp. Dig.*, Jun. 2019, pp. 1430–1433, doi: 10.1109/MWSYM.2019.8700975.

[4] D. F. Brown, A. Kurdoghlian, R. Grabar, D. Santos, J. Magadia, H. Fung, J. Tai, I. Khalaf, and M. Micovic, "Broadband GaN DHFET traveling wave amplifiers with up to 120 GHz bandwidth," in *IEEE Compound Semiconductor Integr. Circuit Symp. Dig.*, Oct. 2016, pp. 1–4, doi: 10.1109/CSICS.2016.7751031.

[5] K. W. Kobayashi, V. Kumar, A. Xie, J. L. Jimenez, E. Beam, and A. Ketterson, "A baseband-65 GHz high linearity-bandwidth GaN LNA using a 1.7 A/mm high current density ScAlN based GaN HEMT technology," in *IEEE MTT-S Int. Microw. Symp. Dig.*, Jun. 2021, pp. 772–775, doi: 10.1109/IMS19712.2021.9575038.

[6] C. F. Campbell, S. Nayak, M.-Y. Kao, and S. Chen, "Design and performance of 16–40 GHz GaN distributed power amplifier MMICs utilizing an advanced 0.15 μm GaN process," in *IEEE MTT-S Int. Microw. Symp. Dig.*, May 2016, pp. 1–4, doi: 10.1109/MWSYM.2016.7540019.

[7] P. Dennler, R. Quay, P. Brückner, M. Schlechtweg, and O. Ambacher, "Watt-level non-uniform distributed 6–37 GHz power amplifier MMIC with dual-gate driver stage in GaN technology," in *Proc. IEEE Top. Conf. Power Modeling Wireless Radio Appl. (PAWR)*, Jan. 2014, pp. 37–39, doi: 10.1109/PAWR.2014.6825727.

[8] M. Roberg, M. Pilla, T. R. M. Kywe, R. Flynt, and N. Chu, "A 20 W 2–20 GHz GaN MMIC power amplifier using a decade bandwidth transformer-based power combiner," in *IEEE MTT-S Int. Microw. Symp. Dig.*, Aug. 2020, pp. 1287–1290, doi: 10.1109/IMS30576.2020.9223886.

[9] M. Roberg, T. R. M. Kywe, M. Irvine, O. Marrufo, and S. Nayak, "40 W Ka-band single and dual output GaN MMIC power amplifiers on SiC," in *Proc. IEEE BiCMOS Compound Semiconductor Integr. Circuits Technol. Symp. (BCICTS)*, Oct. 2018, pp. 140–143, doi: 10.1109/BCICTS.2018.8551075.

[10] S. Din, M. Wojtowicz, and M. Siddiqui, "High power and high efficiency Ka band power amplifier," in *IEEE MTT-S Int. Microw. Symp. Dig.*, May 2015, pp. 1–4, doi: 10.1109/MWSYM.2015.7166776.

[11] B. Schmukler, J. Barner, J. Fisher, D. A. Gajewski, S. T. Sheppard, J. W. Milligan, K. M. Bothe, S. Ganguly, T. Alcorn, J. Gao, C. Hardiman, E. Jones, D. Namishia, and F. Radulescu, "A high efficiency, Ka-band, GaN-on-SiC MMIC with low compression," in *Proc. IEEE BiCMOS Compound Semiconductor Integr. Circuits Technol. Symp. (BCICTS)*, Nov. 2019, pp. 1–4, doi: 10.1109/BCICTS45179.2019.8972749.

[12] P. Neininger, L. John, F. Thome, C. Friesicke, P. Brückner, R. Quay, and T. Zwick, "Limitations and implementation strategies of interstage matching in a 6-W, 28–38-GHz GaN power amplifier MMIC," *IEEE Trans. Microw. Theory Techn.*, vol. 69, no. 5, pp. 2541–2553, May 2021, doi: 10.1109/TMTT.2021.3065108.

[13] U. Mishra and J. Singh, *Semiconductor Device Physics and Design* (Series on Integrated Circuits and Systems). Amsterdam, The Netherlands: Springer, 2007. [Online]. Available: https://books.google.de/books?id=6NAtk7zr3n4C

[14] M. A. Caro, S. Zhang, T. Riekkinen, M. Ylilammi, M. A. Moram, O. Lopez-Acevedo, J. Molarius, and T. Laurila, "Piezoelectric coefficients and spontaneous polarization of ScAlN," *J. Phys., Condens. Matter*, vol. 27, no. 24, Jun. 2015, Art. no. 245901, doi: 10.1088/0953-8984/27/24/245901.

[15] O. Ambacher, B. Christian, M. Yassine, M. Baeumler, S. Leone, and R. Quay, "Polarization induced interface and electron sheet charges of pseudomorphic ScAlN/GaN, GaAlN/GaN, InAlN/GaN, and InAlN/InN heterostructures," *J. Appl. Phys.*, vol. 129, no. 20, May 2021, Art. no. 204501, doi: 10.1063/5.0049185.

[16] K. Shinohara, A. Corrion, D. Regan, I. Milosavljevic, D. Brown, S. Burnham, P. J. Willadsen, C. Butler, A. Schmitz, D. Wheeler, A. Fung, and M. Micovic, "220 GHz f_T and 400 GHz f_{max} in 40-nm GaN DH-HEMTs with re-grown ohmic," *IEDM Tech. Dig.*, Dec. 2010, pp. 30.1.1–30.1.4, doi: 10.1109/IEDM.2010.5703448.

[17] J.-S. Moon, B. Grabar, J. Wong, D. Chuong, E. Arkun, D. V. Morales, P. Chen, C. Malek, D. Fanning, N. Venkatesan, and P. Fay, "Power scaling of graded-channel GaN HEMTs with mini-field-plate T-gate and 156 GHz f_T," *IEEE Electron Device Lett.*, vol. 42, no. 6, pp. 796–799, Jun. 2021, doi: 10.1109/LED.2021.3075926.

[18] K. Shinohara, C. King, E. J. Regan, J. Bergman, A. D. Carter, A. Arias, M. Urteaga, B. Brar, R. Page, R. Chaudhuri, M. Islam, H. Xing, and D. Jena, "GaN-based multi-channel transistors with lateral gate for linear and efficient millimeter-wave power amplifiers," in *IEEE MTT-S Int. Microw. Symp. Dig.*, Jun. 2019, pp. 1133–1135, doi: 10.1109/MWSYM.2019.8700845.

[19] J. Joh and J. A. D. Alamo, "Mechanisms for electrical degradation of GaN high-electron mobility transistors," in *Proc. IEDM*, Dec. 2006, pp. 1–4, doi: 10.1109/IEDM.2006.346799.

[20] A. J. Green, J. K. Gillespie, R. C. Fitch, D. E. Walker, M. Lindquist, A. Crespo, D. Brooks, E. Beam, A. Xie, V. Kumar, J. Jimenez, C. Lee, Y. Cao, K. D. Chabak, and G. H. Jessen, "ScAlN/GaN high-electron-mobility transistors with 2.4-A/mm current density and 0.67-S/mm transconductance," *IEEE Electron Device Lett.*, vol. 40, no. 7, pp. 1056–1059, Jul. 2019, doi: 10.1109/LED.2019.2915555.

[21] A. J. Green, N. Moser, N. C. Miller, K. J. Liddy, M. Lindquist, M. Elliot, J. K. Gillespie, R. C. Fitch, R. Gilbert, D. E. Walker, E. Werner, A. Crespo, E. Beam, A. Xie, C. Lee, Y. Cao, and K. D. Chabak, "RF power performance of Sc(Al,Ga)N/GaN HEMTs at Ka-band," *IEEE Electron Device Lett.*, vol. 41, no. 8, pp. 1181–1184, Aug. 2020, doi: 10.1109/LED.2020.3006035.

[22] T. E. Kazior, E. M. Chumbes, B. Schultz, J. Logan, D. J. Meyer, and M. T. Hardy, "High power density ScAlN-based heterostructure FETs for mm-wave applications," in *IEEE MTT-S Int. Microw. Symp. Dig.*, Jun. 2019, pp. 1136–1139, doi: 10.1109/MWSYM.2019.8701055.

[23] M. B. Tahhan, J. A. Logan, M. T. Hardy, M. G. Ancona, B. Schultz, B. Appleton, T. Kazior, D. J. Meyer, and E. M. Chumbes, "Passivation schemes for ScAlN-barrier mm-wave high electron mobility transistors," *IEEE Trans. Electron Devices*, vol. 69, no. 3, pp. 962–967, Mar. 2022, doi: 10.1109/TED.2021.3140016.

[24] C. Manz, S. Leone, L. Kirste, J. Ligl, K. Frei, T. Fuchs, M. Prescher, P. Waltereit, M. A. Verheijen, A. Graff, M. Simon-Najasek, F. Altmann, M. Fiederle, and O. Ambacher, "Improved AlScN/GaN heterostructures grown by metal-organic chemical vapor deposition," *Semicond. Sci. Technol.*, vol. 36, no. 3, Mar. 2021, Art. no. 034003, doi: 10.1088/1361-6641/abd924.

[25] J. Ligl, S. Leone, C. Manz, L. Kirste, P. Doering, T. Fuchs, M. Prescher, and O. Ambacher, "Metalorganic chemical vapor phase deposition of AlScN/GaN heterostructures," *J. Appl. Phys.*, vol. 127, no. 19, May 2020, Art. no. 195704, doi: 10.1063/5.0003095.

[26] S. Leone, J. Ligl, C. Manz, L. Kirste, T. Fuchs, H. Menner, M. Prescher, J. Wiegert, A. Žukauskaitė, R. Quay, and O. Ambacher, "Metal-organic chemical vapor deposition of aluminum scandium nitride," *Phys. Status Solidi, Rapid Res. Lett.*, vol. 14, no. 1, Jan. 2020, Art. no. 1900535, doi: 10.1002/pssr.201900535.

[27] I. Streicher, S. Leone, L. Kirste, C. Manz, P. Straňák, M. Prescher, P. Waltereit, M. Mikulla, R. Quay, and O. Ambacher, "Enhanced AlScN/GaN heterostructures grown with a novel precursor by metal–organic chemical vapor deposition," *Phys. Status Solidi, Rapid Res. Lett.*, Nov. 2022, Art. no. 2200387, doi: 10.1002/pssr.202200387.

[28] S. Karmalkar and U. K. Mishra, "Enhancement of breakdown voltage in AlGaN/GaN high electron mobility transistors using a field plate," *IEEE Trans. Electron Devices*, vol. 48, no. 8, pp. 1515–1521, Aug. 2001, doi: 10.1109/16.936500.

[29] D. Schwantuschke, B. J. Godejohann, P. Brückner, A. Tessmann, and R. Quay, "mm-wave operation of AlN/GaN-devices and MMICs at V-&W-band," *Proc. Int. Microw. Radar Conf.*, May 2018, pp. 238–241, doi: 10.23919/MIKON.2018.8405187.

[30] B. Romanczyk, S. Wienecke, M. Guidry, H. Li, E. Ahmadi, X. Zheng, S. Keller, and U. K. Mishra, "Demonstration of constant 8 W/mm power density at 10, 30, and 94 GHz in state-of-the-art millimeter-wave N-polar GaN MISHEMTs," *IEEE Trans. Electron Devices*, vol. 65, no. 1, pp. 45–50, Jan. 2018, doi: 10.1109/TED.2017.2770087.

[31] Y. Cao, V. Kumar, S. Chen, Y. Cui, S. Yoon, E. Beam, A. Xie, J. Jimenez, A. Ketterson, C. Lee, D. Linkhart, and A. Geiler, "Qorvo's emerging GaN technologies for mmWave applications," in *IEEE MTT-S Int. Microw. Symp. Dig.*, Aug. 2020, pp. 570–572, doi: 10.1109/IMS30576.2020.9223913.

[32] T. E. Kazior, G. M. Jones, and T.-H. Chang, "Emerging millimeter-wave device technology—Next generation GaN and beyond," in *IEEE MTT-S Int. Microw. Symp. Dig.*, Jun. 2022, pp. 287–290, doi: 10.1109/IMS37962.2022.9865442.

[33] J. Chang, S. Afroz, B. Novak, J. Merkel, K. Nagamatsu, and R. Howell, "Advances in the super-lattice castellated field effect transistor (SLCFET) for high power density, energy efficient RF amplification," in *IEEE MTT-S Int. Microw. Symp. Dig.*, Aug. 2020, pp. 576–579, doi: 10.1109/IMS30576.2020.9224099.