# Why Ideal Constant Power Loads Are Not the Worst Case Condition From a Control Standpoint

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*Abstract*—This paper investigates the influence of control bandwidth on the stability of loads, which are interfaced through power electronic converters and are fed from a dc power source. When tightly regulated, these loads exhibit a constant power load (CPL) behavior. It is shown here that the ideal CPL assumption, prevalent in literature, may not represent the worst case in real-life applications. If the control bandwidth of the load is sufficiently high, the load behaves like a CPL, and the system stability margin decreases with the increase in output power. However, in a practical range, with a lower control bandwidth, the system stability margin is influenced critically by the converter's characteristic impedance, as well as its output power. Under these conditions, the minimum stability margin may occur at a low-power range.

*Index Terms*—Closed loop systems, dc–dc power converters, dc power systems, linear feedback control systems, load modeling, negative feedback, nonlinear control systems, power system stability, system analysis and design, voltage control.

## I. Introduction

I N RECENT years, different topologies of smart distribution systems have been proposed in the scientific literature; one of these concepts is the microgrid. These microgrids can be classified as ac or dc [1]–[3] based on the coupling point or main bus.

The dc microgrid is, from a technology standpoint, an interesting case, as all distributed generation and storage devices are connected through an inverter and the majority of the loads are also connected to the grid via a power electronics interface.

The application of the dc microgrids is not limited to terrestrial distribution systems but can also be applied in other dc systems with distributed generation from renewable and nonrenewable energy such as aircraft power systems and shipboard power systems [1], [4], [5].

The direct interface of a load through a converter introduces significant challenges. These challenges lie in the dynamic stability of the system, due to the nonlinear behavior of the constant power load (CPL) [6]. From the point of view of the

dc bus, such converters exhibit a CPL behavior, as they tend to maintain the load power constant under fast current and voltage disturbances (e.g., drive applications).

As a consequence, the converters present to the dc bus a negative incremental resistance behavior, which may cause, in certain conditions, instability of the bus voltage in a medium voltage dc (MVDC) distribution [7]. These conditions and the methods for stability analysis of MVDC systems have been reviewed and discussed in [9].

The efforts to prevent MVDC instability due to small-signal negative resistance behavior have been concentrated on the design of the power converters interfacing the loads to the MVDC distribution. With this approach, it is up to the load themselves and their converters, to prevent the MVDC from voltage instability: either through dedicated control algorithms [9], [10], or through forcing disconnection, when jeopardizing the MVDC system stability. Other solutions that focus on guaranteeing the stability on the MVDC bus from the generation-side converters were proposed in [11]–[14].

## II. Challenges and Method

In order to analyze the stability of MVDC systems, an ideal constant power assumption is often applied [15]. However, this assumption has limitations when the input characteristic of a load deviates from the CPL behavior. Furthermore, the assumption of an ideal CPL does not take into account the influence of the controller design and operating conditions on the system stability. Therefore, it is necessary to establish detailed models of the power system to fully account the dynamic behavior and its influence on stability [16]–[23].

However, there is very little systematic research on large signal stability analysis of MVDC systems due to the lack of reliable large-signal models of the converters. Youssef *et al.* [24] use the state space averaging method or controlled voltage and current source to replace the power converter switches in the circuit. The duty ratio is embedded in the main parameters of the model so that the model is different according to operating conditions, necessitating a case-by-case analysis depending on the operating mode. This problem also exists in the behavioral model proposed in [25]. Another approach is shown in [18], where ideal transformers are used instead of switches. All of these approaches share the ideal CPL assumption as the worst case behavior. However, it was shown that this assumption may not always be true, as there is an interdependency between the bandwidth of the involved generation and load units [26], [27].
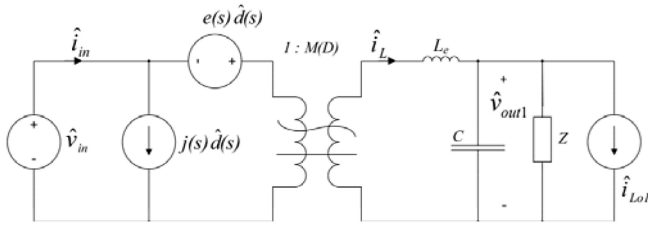
Fig. 1. Canonical model: a small signal equivalent circuit that models dc–dc converter dynamics and transfer functions.

Nonetheless, until now the interdependency of the control bandwidth of the load-side converter on the control goal of the generation-side converter with respect to the control variable (e.g., the voltage of the dc bus) has not been sufficiently addressed: in effect, the ideal CPL assumption in the form of a nonlinear controlled source inherits the time constant of the passive components of the dc link.

In this paper, we will show how the practical results of different converter power levels and loads, switching frequency, and control bandwidth yield a load behavior different from the ideal CPL behavior. Main goal is to determine under which circumstances the ideal representation is actually meaningful and under which it may even produce misleading results.

## III. SINGLE CONVERTER MODEL

### A. Canonical Model

To be able to design the control system of the converter, it is necessary to model its dynamic behavior. Typically, this includes how the variations of the input voltage, the load current, and the duty cycle affect the output voltage. As converters are nonlinear components due to the switching behavior, state space averaging is often used to generate small signal models. By using this method, equivalent circuit models of dc–dc converters can be synthesized and, consequently, the canonical circuit model in Fig. 1 can be used to represent the physical properties of pulse width modulated (PWM) dc–dc converters in continuous conduction mode (CCM) [28], [29]. In this paper, $\hat{v}_{in}$ and $\hat{v}_{out}$ corresponds to the small signal perturbation in the input and output voltage. The small signal perturbation in the duty cycle is represented by $\hat{d}$, while $\hat{i}_{Lo1}$ represents the load current variation.

Canonical model parameters for the ideal buck, boost, and buck-boost converter are listed in Table I. As the representation in Fig. 1 is a general one, it can be used for all three models by changing the values of $M(D)$, $L_e$, $e(s)$, $j(s)$ and, therefore, describes the behavior of the selected converter. The transformer being used in this paper is an ideal dc transformer with the turns ratio of $1{:}M(D)$, which is a function of the duty cycle $D$, where $D' = 1 - D$. The term $e(s)\hat{d}(s)$ and $j(s)\hat{d}(s)$ represent perturbations in the duty cycle which are usually caused by a control circuit.

### B. Mathematical Representation of the Canonical Model

The canonical circuit model of Fig. 1 can be solved using conventional linear circuit analysis techniques. It is then possible to derive the transfer functions for a converter operating in open-loop. The quantities of interest are: 1) control-to-output

TABLE I
CANONICAL MODEL PARAMETERS FOR CONVERTERS IN CCM

| Converter | $M(D)$ | $L_e$ | $e(s)$ | $j(s)$ |
|---|---|---|---|---|
| Buck | $D$ | $L$ | $\dfrac{V_{out1}}{D^2}$ | $\dfrac{V_{out1}}{Z}$ |
| Boost | $\dfrac{1}{D'}$ | $\dfrac{L}{D'^2}$ | $V_{out1}\left(1 - \dfrac{sL}{ZD'^2}\right)$ | $\dfrac{V_{out1}}{ZD'^2}$ |
| Buck-Boost | $-\dfrac{D}{D'}$ | $\dfrac{L}{D'^2}$ | $-\dfrac{V_{out1}}{D^2}\left(1 - \dfrac{sLD}{ZD'^2}\right)$ | $-\dfrac{V_{out1}}{ZD'^2}$ |

transfer function $G_{vd}(s)$; 2) converter line-to-output transfer function $G_{vg}(s)$; 3) converter output impedance $Z_{out}(s)$; 4) converter input impedance $Z_{in}(s)$; 5) the control-to-inductor current transfer function $G_{id}(s)$; and 6) the line-to-inductor current transfer function $G_{ig}(s)$. The formalism for transforming the canonical model to a mathematical model is given in [28] and [29] and the exact definitions of the transfer functions are the following:

$$G_{vd}(s) = \left.\frac{\hat{v}_{out1}(s)}{\hat{d}(s)}\right|_{\hat{v}_{in},\hat{i}_{Lo1}=0} = \frac{M(D)e(s)}{C_1 L_e s^2 + \frac{L_e}{Z}s + 1} \quad (1)$$

$$G_{vg}(s) = \left.\frac{\hat{v}_{out1}(s)}{\hat{v}_{in}(s)}\right|_{\hat{d},\hat{i}_{Lo1}=0} = \frac{M(D)}{C_1 L_e s^2 + \frac{L_e}{Z}s + 1} \quad (2)$$

$$Z_{out}(s) = \left.\frac{\hat{v}_{out1}(s)}{-\hat{i}_{Lo1}(s)}\right|_{\hat{d},\hat{v}_{in}=0} = \frac{L_e s}{C_1 L_e s^2 + \frac{L_e}{Z}s + 1} \quad (3)$$

$$G_{id}(s) = \left.\frac{\hat{i}_L(s)}{\hat{d}(s)}\right|_{\hat{v}_{in},\hat{i}_{Lo1}=0} = \frac{M(D)e(s)(\frac{1}{Z} + C_1 s)}{C_1 L_e s^2 + \frac{L_e}{Z}s + 1} \quad (4)$$

$$G_{ig}(s) = \left.\frac{\hat{i}_L(s)}{\hat{v}_{in}(s)}\right|_{\hat{d},\hat{i}_{Lo1}=0} = \frac{M(D)(\frac{1}{Z} + C_1 s)}{C_1 L_e s^2 + \frac{L_e}{Z}s + 1} \quad (5)$$

$$Z_{in}(s) = \left.\frac{\hat{v}_{in}(s)}{\hat{i}_{in}(s)}\right|_{\hat{d},\hat{i}_{Lo1}=0} = \frac{1}{M(D)\,G_{ig}(s)}. \quad (6)$$

This approach leads to the following mathematical representation of the converter:

$$\begin{pmatrix} \hat{v}_{out1} \\ \hat{i}_L \end{pmatrix} = \begin{pmatrix} -Z_{out} & G_{vg} & G_{vd} \\ \frac{Z_{out}}{sL_e} & G_{ig} & G_{id} \end{pmatrix} \begin{pmatrix} \hat{i}_{Lo1} \\ \hat{v}_{in} \\ \hat{d} \end{pmatrix}. \quad (7)$$

This matrix is depicted in a control block representation of Fig. 2, where the open loop small signal model can be derived by setting $\hat{d}(s)$ equal to zero.

### C. Closed-Loop Transfer Functions

As the goal of this paper is to derive a cascaded closed-loop converter system, the small-signal-closed loop transfer functions are also required. Those transfer functions are needed for the closed-loop input and output impedance $Z_{in\_CL}$, $Z_{out\_CL}$ and the transfer function representing the closed-loop input to output voltage perturbation $G_{vg\_CL}$ [30].

In order to show the concept, we assume one of the most common control system operations for a dc–dc converter which is the voltage mode control (VMC) [29]. The
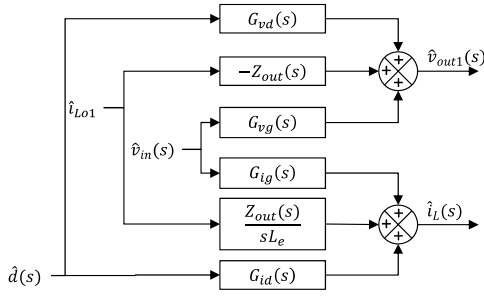
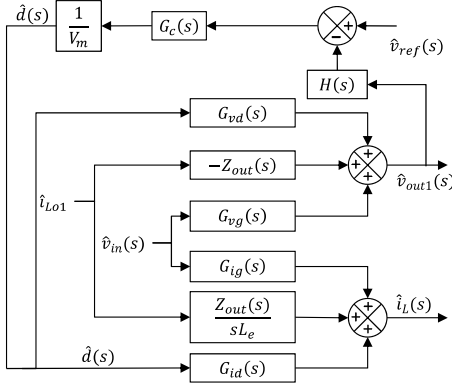Fig. 2.  Mathematical representation of small-signal converter.



Fig. 3.  Block diagram of VMC of converter.

corresponding schematic is depicted in Fig. 3. The changes from Figs. 2 and 3 are as follows.

1) $\hat{v}_{\text{ref}}(s)$ is the perturbation in the reference voltage.
2) The term $H(s)$ is the transfer function of the sensing network, which often can be considered as a pure gain.
3) $G_c(s)$ is the compensator transfer function. Commonly used compensators are proportional-integral (PI), proportional-derrivative (PD), or proportional-integral-derivative (PID).

The PWM gain is equal to $(1/V_m)$, where $V_m$ corresponds to the amplitude of the dc bus.

*1) Feedback:* The solution of Fig. 3 according to [29] yields for (8) the voltage output variation, where $T(s)$ is defined in general as the product of gains around the forward and feedback paths of the loop. This equation shows how the addition of a feedback loop modifies the transfer function of the system

$$\hat{v}_{\text{out1}} = \hat{v}_{\text{ref}}\frac{1}{H(s)}\frac{T(s)}{1+T(s)} + \hat{v}_{\text{in}}\frac{G_{vg}}{1+T(s)} - \hat{i}_{\text{Lo1}}\frac{Z_{\text{out}}}{1+T(s)} \quad (8)$$

$$T(s) = H(s)G_c(s)\,G_{vd}(s)\,\frac{1}{V_m} \quad (9)$$

$$G_{vg\_CL}(s) = \frac{\hat{v}_{\text{out1}}(s)}{\hat{v}_{\text{in}}(s)}\bigg|_{\hat{v}_{\text{ref}},\hat{i}_{\text{Lo1}}=0} = \frac{G_{vg}}{1+T(s)} \quad (10)$$

$$Z_{\text{out\_CL}}(s) = \frac{\hat{v}_{\text{out1}}(s)}{-\hat{i}_{\text{Lo1}}(s)}\bigg|_{\hat{v}_{\text{ref}},\hat{i}_{\text{Lo1}}=0} = \frac{Z_{\text{out}}}{1+T(s)}. \quad (11)$$

It can be seen that through the feedback the closed-loop transfer function and the output impedances are reduced by the factor of $1/(1+T(s))$.

*2) Closed-Loop Input Impedance:* The definition of the closed loop input impedance is the ratio of perturbations in

the input voltage $\hat{v}_{\text{in}}$ to the perturbations in the input current $\hat{i}_L(s)$, while the perturbations in the load current $\hat{i}_{\text{Lo1}}$ are zero

$$Z_{\text{IN\_CL}}(s) = \frac{\hat{v}_{\text{in}}(s)}{\hat{i}_{\text{In1}}(s)}\bigg|_{\hat{v}_{\text{ref}},\hat{i}_{\text{Lo1}}=0}. \quad (12)$$

Analyzing Fig. 3 and setting $\hat{v}_{\text{ref}}$ and $\hat{i}_{\text{Lo1}}$ to zero the following equations is obtained. The last equation, which gives the relationship between input current perturbation $\hat{i}_{\text{In1}}$ and inductor current perturbation $\hat{i}_L(s)$, is obtained by examining the circuit in Fig. 1

$$\hat{d}(s) = -\hat{v}_{\text{out1}}H(s)G_c(s)\,\frac{1}{V_m} \quad (13)$$

$$\hat{v}_{\text{out1}} = \hat{d}(s)\,G_{vd}(s) + \hat{v}_{\text{in}}(s)\,G_{vg}(s) \quad (14)$$

$$\hat{i}_L(s) = \hat{d}(s)\,G_{id}(s) + \hat{v}_{\text{in}}(s)G_{ig}(s) \quad (15)$$

$$\hat{i}_{\text{In1}} = j(s)\,\hat{d}(s) + M(D)\,\hat{i}_L(s). \quad (16)$$

After solving this system of equations, we get the following relationship for the closed-loop input impedance. This relationship will be used in the cascaded converter model in the next section

$$Z_{\text{IN\_CL}}(s) = \frac{\hat{v}_{\text{in}}(s)}{\hat{i}_{\text{In1}}(s)}\bigg|_{\hat{v}_{\text{ref}},\hat{i}_{\text{Lo1}}=0}$$

$$= Z_{\text{IN}}(s)\left(\frac{1+T}{1-T\frac{j(s)}{e(s)M(D)G_{ig}(s)}}\right). \quad (17)$$

Solving (17) for a closed-loop converter loaded with a generic impedance load $Z$ holds

$$Z_{\text{IN}_{CL}}(s) = \frac{(ZC_1L_es^2 + L_es + Z)V_m + ZH(s)G_c(s)M(D)e(s))}{V_m(M(D))^2(1+ZC_1s) - j(s)ZH(s)G_c(s)M(D)}. \quad (18)$$

## IV. Cascaded Converter Model

Cascading two dc–dc converters means that the downstream converter now referred to as converter 2 or point of load converter (POL) acts as load of the upstream converter now labeled as converter 1 or also called line regulating converter (LRC). Using the previously mentioned canonical model, this leads to the topology depicted in Fig. 4. Cascading also means that the output voltage of LRC is equal to the input voltage of POL and the input current of the POL equals the output current of the LRC. This correspondence can be extended for the small-signal values of the perturbations of the voltages and currents.

Therefore, it follows that the small-signal current drawn from the LRC $\hat{i}_{\text{Lo1}}$ depends on the dynamics of the POL converter, which has to be equal to the input current $\hat{i}_{\text{in2}}$ of the POL. The same conclusion can be made for the output voltage perturbation of the LRC $\hat{v}_{\text{out1}}$, which has to be equal to the input voltage perturbation of the POL $\hat{v}_{\text{in2}}$. We assume that in cascading two converters the LRC is only supplying one POL: therefore the load impedance $Z$, which appears in Fig. 1, is eliminated and instead the small-signal model of the converter in Fig. 1 is used again.

The output filter capacitor $(C_{oF})$ and input filter capacitor $(C_{iF})$ are represented by the equivalent capacitor $C_1$ in
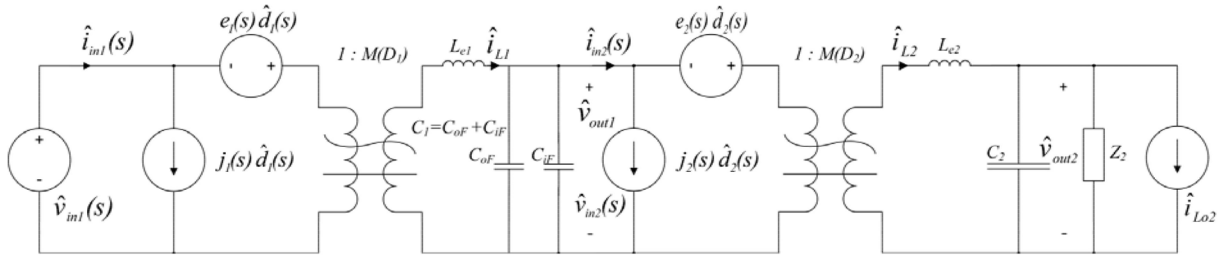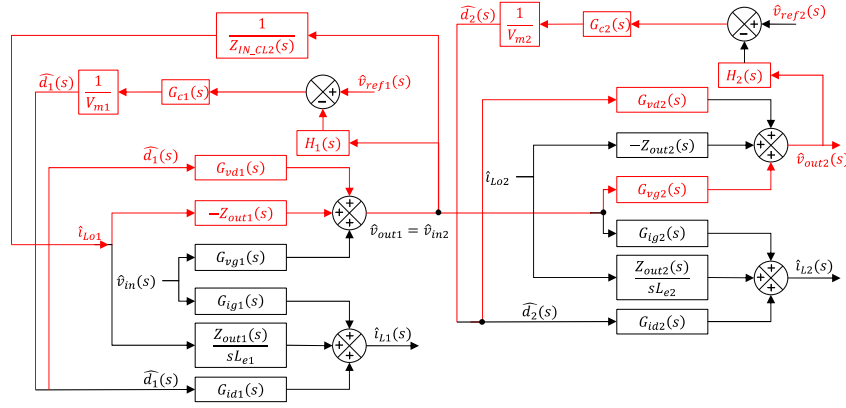
Fig. 4. Canonical cascaded system.



Fig. 5. Cascaded control blocks.

Fig. 4. The same approach as in the previous section can be used, which leads to the mathematical representation of the cascaded system. When assuming that the POL converter acts as load to the LRC converter, the small-signal current drawn from LRC $\hat{i}_{Lo1}$ can be expressed by means of the Thevenins theorem, where POL converter is an impedance element which corresponds to the closed loop input impedances $Z_{IN\_CL2}$. This relation is depicted in Fig. 5

$$\hat{i}_{Lo1} = \frac{\hat{v}_{out1}}{Z_{IN\_CL2}}. \tag{19}$$

Combining (8) and (19) leads to the following expression for the voltage of the dc bus capacitor in a cascaded system:

$$\hat{v}_{out1} = \hat{v}_{ref} \frac{1}{H} \frac{T}{1+T} + \hat{v}_{in} \frac{1}{H(s)} \frac{G_{vg}}{1+T} - \frac{\hat{v}_{out1}}{Z_{IN\_CL2}} \frac{Z_{out1}}{1+T}. \tag{20}$$

Normally, a cascaded converter architecture is designed in such a way that it delivers a defined voltage $\hat{v}_{out2}$ to the load under the assumption of a predefined reference voltage $\hat{v}_{ref1}$. For the initial loop design, the effect of possible perturbations in the input voltage of the cascaded system $\hat{v}_{in1}$ and the load current $\hat{i}_{Lo2}$ are neglected. When further inspecting Fig. 5, it becomes clear that for the path $\hat{v}_{ref1}$ to $\hat{v}_{out2}$ (marked in red) it is not necessary to consider the inductor currents $(\hat{i}_{L1}, \hat{i}_{L2})$. The positive feedback loop containing the block $-Z_{out1}/Z_{IN_{CL2}}$ can be condensed to $1/(1 + Z_{out1}/Z_{IN_{CL2}})$ which makes it possible to write the reference to output voltage

transfer function for the first converter

$$\frac{\hat{v}_{out1}(s)}{\hat{v}_{ref1}(s)} = \frac{\frac{1}{V_{m1}} G_{C1} G_{vd1} \frac{1}{1 + \frac{Z_{out1}}{Z_{IN\_CL2}}}}{1 + \frac{H_1}{V_{m1}} G_{C1} G_{vd1} \frac{1}{1 + \frac{Z_{out1}}{Z_{IN\_CL2}}}}. \tag{21}$$

Inspecting the second converter loop yields the following equation:

$$\hat{v}_{out2}(s) = \left(\hat{v}_{ref2}(s) - H_2 \hat{v}_{out2}\right) \frac{1}{V_{m2}} G_{C2} G_{vd2} + G_{vg2} \hat{v}_{out1}. \tag{22}$$

From (17), (21), and (22), it can be clearly seen that there exists an interdependence on how the selection of parameters of the controllers $G_{C1}$ and $G_{C2}$ influence each other. It also can be seen how the dynamics of the load supplied by the second converter influences the voltage of the dc bus. This interdependence poses some interesting questions on the nontrivial design process but this is not the scope of this paper.

## V. CPL MODEL

Due to the integration in dc grids of LRC and POL converters the efficiency of the network is increased and due to the control algorithm implemented in the converters these grids are able to handle a wide variation in either load or source [31].

As an example, a buck POL converter with a resistive load is shown in Fig. 6, where $Z_L(s) = R$. Power converters such as a buck converter are used because of their tight output voltage control capability, which enables them to respond almost immediately to system changes.
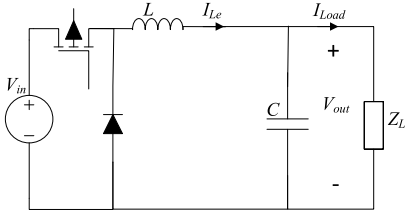
Fig. 6.   Buck converter loaded with a resistive load.

On the other hand, under these conditions, the converter tends to operate as a CPL. When averaging the states and applying the canonical model with the parameters of Table I and (1), the linearized impedance model of the buck converter systems for a given operating point is given in (23). As all denominator coefficients are positive and not zero the perturbation transfer function for a single POL converter which is supplied by an ideal voltage source satisfies the Hurwitz criteria for stability

$$\frac{\hat{v}_{\text{out}}(s)}{\hat{d}(s)} = \frac{\frac{V_c}{D}}{CLs^2 + \frac{L}{R}s + 1} = \frac{\overline{v}_{\text{in}}\frac{1}{LC}}{s^2 + \frac{1}{RC}s + \frac{1}{LC}1} \qquad (23)$$

$$Z_{\text{IN}_{CL}}(s) = \frac{(C_1 L_e s^2 Z + L_e s + Z)V_m + ZH(s)G_c(s)\frac{V_{\text{out1}}}{D}}{V_m D^2(1 + ZC_1 s) - H(s)G_c(s)V_{\text{out1}}D} \qquad (24)$$

$$G_c(s) = \frac{K_D}{s}\left(s^2 + \frac{K_P}{K_D}s + \frac{K_I}{K_D}\right). \qquad (25)$$

We assume now a constant sensor gain and PWM gain of 1 and also assume a general PID controller (25) with proportional gain $K_P$, integral gain $K_I$, and derivative gain $K_D$ for regulating the closed-loop converters which yields the following generalized expression (26) as shown at the bottom of the page.

By assuming that $Z_L(s) = R$, the numerators are defined as $n_3 = RC_1 L$; $n_2 = L + RK_D\overline{v}_{\text{in}}$; $n_1 = R + RK_P\overline{v}_{\text{in1}}$; $n_0 = RK_I\overline{v}_{\text{in}}$ while the denominators are defined as

$$d_2 = RC_1 D^2 - K_D D^2 \overline{v}_{\text{in}}, \quad d_1 = D^2 - K_P D^2 \overline{v}_{\text{in1}},$$
$$d_0 = -K_I D^2 \overline{v}_{\text{in1}}.$$

The steady-state error for a step input can be calculated with the final value theorem and corresponds to the dc gain which will yield for $Z_L(s) = R$

$$e_{ss} = \lim_{s \to 0} s \frac{1}{s} Z_{\text{IN}_{CL}}(s) = \frac{n_0}{d_0} = -\frac{R}{D^2}. \qquad (27)$$

This behaves like a negative destabilizing resistance. Rivetta et al. [15] and Zamierczuk et al. [32] state that the closed-loop input resistance $Z_{\text{IN}_{CL}}$ of a POL is approximately $-Z_{\text{IN}_{\text{open}}}$. The negative resistance of (27) pushes an open-loop pole into the right half plane and destabilizes the transfer function of (23). Therefore, often in literature the approximation of

a complex load is performed, which exhibits constant power behavior

$$Z_{\text{Load}}(s) = \frac{\hat{v}_l(s)}{\hat{i}_l(s)} = \frac{v_c^2}{P_L}; \quad P_L = const. \qquad (28)$$

What has to be noted is that by using (28) instead of (26) it is assumed that no dynamic interactions will take place between the converters, which is a very optimistic assumption, particularly when considering that the POL converters are operating at a higher switching frequency than the LRC [27].

## VI. DESTABILIZING LOAD MODELS

A generalized load impedance model was described under the assumption that the closed-loop buck converter is PI-regulated [33]. We will extend the proposed destabilizing load forms, which were proposed by LeSage et al. [33], to match a PID regulator. Those load forms represent destabilizing characteristics under certain parameter variations and dynamic conditions which exhibit a different dynamic behavior in contrast to the CPL assumption.

### A. First-Order Lag

In this case, the first-order lag function replaces the constant resistance where $R$ is the dc gain of the load and $\tau$ is the time constant [33]. This type of load corresponds to a parallel circuit of a resistive and a capacitive load

$$Z_{\text{Load}}(s) = \frac{R}{\tau s + 1}; \quad \tau \in \mathbb{R}^+ \qquad (29)$$

$$Z_{\text{IN}_{CL}}(s) = \frac{n_3 s^3 + n_2 s^2 + n_1 s + n_0}{d_3 s^3 + d_2 s^2 + d_1 s + d_0} \qquad (30)$$

where the numerator and denominator coefficients in (29) $n_3 = (RC_1 + \tau)L$, $n_2 = L + RK_D\overline{v}_{\text{in}}$, $n_1 = R(1 + K_P\overline{v}_{\text{in1}})$, $n_0 = RK_I\overline{v}_{\text{in}}$, $d_3 = -K_D D^2 \overline{v}_{\text{in}}\tau$, $d_2 = D^2((RC_1 - K_D\overline{v}_{\text{in1}}) + (1 - K_P\overline{v}_{\text{in1}})\tau)$, $d_1 = D^2 + D^2\overline{v}_{\text{in1}}(K_P + K_I\tau)$, $d_0 = -K_I D^2 \overline{v}_{\text{in1}}$.

If $\tau = 0$, we are consequentially back at the CPL case as it is assumed that the load responds instantaneously.

### B. First-Order Unstable

Replacing the load in (26) by an unstable impedance function yields a $Z_{\text{IN}_{CL}}$ equal to

$$Z_{\text{Load}}(s) = -\frac{b}{s - a}; \quad a, b \in \mathbb{R}^+ \qquad (31)$$

$$Z_{\text{IN}_{CL}}(s) = \frac{n_3 s^3 + n_2 s^2 + n_1 s + n_0}{d_3 s^3 + d_2 s^2 + d_1 s + d_0} \qquad (32)$$

where the numerator and denominator coefficients in (32) $n_3 = 1 - bC_1$, $n_2 = -(bK_D\overline{v}_{\text{in}} + La)$, $n_1 = -(b + bK_P\overline{v}_{\text{in1}})$, $n_0 = -bK_I\overline{v}_{\text{in}}$, $d_3 = -K_D D^2 \overline{v}_{\text{in}}$, $d_2 = D^2(1 - K_P\overline{v}_{\text{in1}} - bC_1 + aK_D\overline{v}_{\text{in1}})$, $d_1 = D^2(aK_P\overline{v}_{\text{in1}} - a - K_I\overline{v}_{\text{in1}})$, $d_0 = K_I D^2 \overline{v}_{\text{in1}}$.

As in this case, the Hurwitz necessary conditions of stability are not met: we observe instability in $Z_{\text{IN}_{CL}}$. It has to be noted

$$Z_{\text{IN}_{CL}}(s) = \frac{ZC_1 Ls^3 + (L + ZK_D\overline{v}_{\text{in}})s^2 + (Z + ZK_P\overline{v}_{\text{in1}})s + ZK_I\overline{v}_{\text{in}}}{(ZC_1 D^2 - K_D D^2 \overline{v}_{\text{in}})s^2 + (D^2 - K_P D^2 \overline{v}_{\text{in1}})s - K_I D^2 \overline{v}_{\text{in1}}} = \frac{n_3 s^3 + n_2 s^2 + n_1 s + n_0}{d_2 s^2 + d_1 s + d_0}. \qquad (26)$$

that while instability can be observed its cause is different from the CPL case.

### C. Nonminimum Phase

Nonminimum phase systems are quite seldom found as time continuous systems, but they merit a consideration due to the wide implementation of digital controllers, where the minimum phase property can be lost due to the sampling. Their response to changes in the input signal are typically in opposite directions, i.e., when the input signal increases, the system output drops briefly before rising again, in contrast to systems with negative reinforcement. Due to the presence of zeros in the right complex half plane, a high feedback system will exhibit instability. We assume now a first-order nonminimum phase load described

$$Z_{\text{Load}}(s) = -\frac{s-b}{s+a}; \quad a, b \in \mathbb{R}^+ \tag{33}$$

$$Z_{\text{IN}_{CL}}(s) = \frac{n_4 s^4 + n_3 s^3 + n_2 s^2 + n_1 s + n_0}{d_3 s^3 + d_2 s^2 + d_1 s + d_0} \tag{34}$$

where in (34)
$n_4 = -C_1 L, n_3 = L + bC_1 L - K_D \bar{v}_{\text{in}}, n_2 = La + bK_D \bar{v}_{\text{in}} - 1 - \bar{v}_{\text{in}1} K_P, n_1 = b + b\bar{v}_{\text{in}1} K_P - K_I \bar{v}_{\text{in}}, n_0 = bK_I \bar{v}_{\text{in}}, d_3 = -C_1 D^2 - K_D D^2 \bar{v}_{\text{in}1}, d_2 = D^2(bC_1 - aK_D \bar{v}_{\text{in}1} + 1 - K_P \bar{v}_{\text{in}1})s^2, d_1 = aD^2 + D^2 \bar{v}_{\text{in}1}(K_I - aK_P), d_0 = -aK_I D^2 \bar{v}_{\text{in}1}$.

With the previously performed analysis, we have shown that a stability analysis has to include assumptions about the dynamic behavior on top of the CPL assumption. Load impedances which have either zeros or poles in the right half plane will exhibit a drastically different behavior than the nondynamic CPL assumption.

### D. Generalized Load

When using generalized impedance loads which follow the polynomial structure given in (35), it is possible to derive with (18) a generalized load input impedance of a closed loop buck converter [see (35) and (36)] at the bottom of the page.

Where in (36)
$n_3 = C_1 L, n_2 = K_D \bar{v}_{\text{in}}, n_1 = (1 + K_P \bar{v}_{\text{in}1}), n_0 = K_I \bar{v}_{\text{in}}, n_{d2} = L, d_{n2} = C_1 D^2, d_2 = -K_D D V_{\text{out}1}, d_1 = D^2 - K_P D^2 \bar{v}_{\text{in}1}, d_0 = -K_I D^2 \bar{v}_{\text{in}1}$

We can see how the distribution of the poles and zeros of $Z_{\text{IN}_{CL}}$ is influenced by the location of the poles and zeros of the generalized load, as right-handed poles and zeros of the load can lead to power system instability that are not obvious while analyzing a stable load converter.

## VII. SIMULATION ENVIRONMENT AND TEST CASE

A small-scale dc power system, consisting of one generating unit connected with one detailed CPL, based on the setup of Fig. 4, has been simulated. As this is a canonical

### TABLE II
### COMPONENT PARAMETERS

|  | LRC(1kHz) | POL(1kHz) | POL(3kHz) |
|---|---|---|---|
| $P_n$ [MW] | 20 | 15 | 15 |
| $V_{in}$ [kV] | 8.91 | 6 | 6 |
| $V_{out}$ [kV] | 6 | 3 | 3 |
| $f_s$ [kHz] | 1 | 1 | 3 |
| $\Delta V$[%] | 3 | 3 | 3 |
| $\Delta I$[%] | 30 | 30 | 30 |
| $R^0$ [$\Omega$] | 1.8 | 1.2//1.2 | 1.2//1.2 |
| $R_e$ [m$\Omega$] | 0.0997 | 0.0332 | 0.0332 |
| $L_e$ [mH] | 2.1 | 1.1 | 0.35088 |
| $C_{of}$ [$\mu$F] | 659.72 | 2000 | 659.72 |
| $C_{if}$ [$\mu$F] | - | 3608 | 1327 |
| $P_n$ [MW] | 20 | 15 | 15 |

### TABLE III
### PID CONTROLLER PARAMETERS FOR POL CONVERTER

|  | 1kHz | 3kHz |
|---|---|---|
| $K_p$ | 5.7154e-5 | 2.8577e-5 |
| $K_i$ | 0.0314 | 0.0471 |
| $K_d$ | 6.5417e-8 | 1.0903e-8 |

model, we selected for the POL and LRC converter in our test case the buck type. Firstly, a small signal analysis is performed in Simulink, based on the averaged model to verify the plausibility of the assumption made in the theoretical part. A large-signal analysis is implemented both in Simulink (averaged model) and real time digital simulator (RTDS) (switching model). On one hand, it helps validating the equivalent impedance modeling method, introduced in Section V with respect to the switching model performance; on the other hand, it helps understanding whether conclusions from small signal analysis have value in a large signal context. The LRC converter was operated in all cases with a switching frequency of 1 kHz. For the POL converter, two switching frequencies were implemented (1 and 3 kHz). The parameters of the corresponding input and output filters were sized as in Table II.

### A. CPL

As shown in Fig. 6, a good example of CPL behavior is a tightly regulated buck converter connected to a resistor. A PID controller is designed as in Table III with the goal to cancel the poles of the open-loop transfer function (23) to match a desired bandwidth. According to [29], the output RLC filter parameters of 15 MW POL buck converter are designed with the criteria of 3% voltage ripple and 30% current ripple, meanwhile, in order to attenuate the switching harmonics and protect the converter and its load from transients that appears in the input voltage $V_{\text{out}1}$, the input filter parameter $C_{if}$ is settled as in Table II. Because of the significantly different

$$Z_L(s) = \frac{\sum_{i=0}^m b_i s^i}{\sum_{j=0}^n a_j s^j}, a_j, b_i \in \mathbb{R} \tag{35}$$

$$Z_{\text{IN}_{CL}}(s) = \frac{n_3 \sum_{i=0}^m b_i s^{i+3} + n_2 \sum_{i=0}^m b_i s^{i+2} + n_1 \sum_{i=0}^m b_i s^{i+1} + n_0 \sum_{i=0}^m b_i s^i + n_{d2} \sum_{j=0}^n a_j s^{j+2}}{d_{n2} \sum_{i=0}^m b_i s^{i+2} + d_2 \sum_{j=0}^n a_j s^{j+2} + d_1 \sum_{j=0}^n a_j s^{j+1} + d_0 \sum_{j=0}^n a_j s^j}. \tag{36}$$

TABLE IV
LINEARIZING STATE FEEDBACK CONTROL PARAMETERS

| | Connected to 1kHz CPL | Connected to 3kHz CPL |
|---|---|---|
| $C_1=C_{of}+C_{if}$ [μF] | 659.72+3608 | 659.72+1327 |
| $K_1$ | 1.464e6 | 1.334e6 |
| $K_2$ | 1459 | 1459 |

resonant frequency of 1 and 3 kHz POL buck converters, the input filters are also sized differently.

## B. Generation Side

The output filter parameters of 20 MW LRC buck converter are designed as shown in Table II. As a tightly regulated buck converter exhibits CPL behavior, which is nonlinear, a linearizing state feedback control strategy [11], [12], is implemented to linearize the overall system behavior, so that the theoretical assumption of Section IV is valid. It has to be noticed that, due to the different input filter $C_{if}$ of the 1 and 3 kHz detailed CPL, the equivalent dc system parameter $C_{i2}$ is changed. The control parameters are also updated accordingly to obtain the same dominant poles with the natural angular frequency 1256 rad/s and damping factor (0.6) as shown in Table IV.

## C. Averaged Model Simulink

Small load connection and disconnection is a common situation in dc power systems. Therefore, a small perturbation in dc system is simulated as a first step to analyze whether the theoretical analysis based on small signal is valid. The dc system, which is based on the buck realization of Fig. 4, is modeled according to the average model via Simulink, $Z_2$ is equivalent to 15 resistances each with the same value in parallel, which can be switched on and switch off. At the beginning the generating unit supplies 14 MW to the system, at $t = 0.01$ s, a resistance (1 MW) in parallel is connected, consequently the total power becomes 15 MW, which corresponds to the rated power of the POL buck converter. In order to compare the different CPL modeling methods, a CPL is represented as an ideal one according to (27) in the first case, and as a detailed one according to (26) in the second case. Both models are connected to the same averaged generating unit regulated by the linearizing state feedback control [12]. In Fig. 7(a), it can be observed that the voltage drop in the case of an ideal CPL model is higher than in the case of 1 kHz detailed CPL model. The reason for this lies in the bandwidth of the ideal CPL, which corresponds to the bandwidth of the overall system $V_{out1}$ ($\approx 1256rad/s$). This one is much higher than the one of the 1 kHz detailed CPL (which is defined by the PID controller, $\approx 690rad/s$).

Likewise, in Fig. 7(b), due to the fact that the bandwidth of the 3 kHz detailed CPL ($\approx 2072rad/s$) is much higher than ideal CPL, the observed voltage drop is higher.

In Fig. 7(c), it is evident that the transient characteristic of bus voltage in case of 1 and 3 kHz detailed CPL is significantly different because of the largely different bandwidth, making clear that using equivalent impedance method to model CPL reflects better the actual behavior.

TABLE V
CIRCUIT PARAMETERS

| | LRC$_{1,2}$(1kHz) | DC POL$_{1...4}$(3kHz) |
|---|---|---|
| $P_n$ [MW] | 25 | 12.5 |
| $V_{in}$ [kV] | 8.91 | 6 |
| $V_{out}$ [kV] | 6 | 1 |
| $f_s$ [kHz] | 1 | 3 |
| $R^0$ [Ω] | - | 0.08 |
| $R_e$ [mΩ] | 0.0097 | 0.005 |
| $L_e$ [mH] | 2 | 1.2 |
| $C_{of}$ [μF] | 2400 | 2000 |
| $C_{if}$ [μF] | - | 4000 |

## D. Switched Model

In order to verify the accuracy of the equivalent impedance modeling method and test the validity of the theory designed based on small-signal model, the same dc system is implemented with switched components in RTDS and with average model in Simulink separately. Instead of using a small perturbation now a large perturbation is set to appear at $t = 0.02$ s where the load changes from 7.5 to 15 MW.

The corresponding results are plotted in Fig. 8. The transient characteristics in the switching model match the one of the averaged model. The steady-state performance of bus voltages and generator currents fits the 5% and 30% ripple constraint.

In addition, Figs. 8(c) and 9(c) represent an apparent different time constant (nearly three times) on the sub-bus voltage $V_{out2}$ due to the different switching frequency, which leads to different bandwidths via PID controller. This different bandwidth causes the relative different transient performance on the main-bus voltage and current. Also in this case, the proposed new CPL modeling method considering the time constant (switching frequency and control design) appears to be more realistic than the previous modeling assumption.

## VIII. DYNAMIC INTERACTION IN MULTIMACHINE SYSTEM

A small-scale MVDC microgrid according to the IEEE 1709 Standard [7] with radial topology was implemented in RTDS, consisting of two gas turbines, which are interfaced through a diode bridge and a buck converter to a dc bus, and four dc load centers where each one is connected via a buck converter. All microgrid loads are fed through buck POL converters, loaded with a resistance and operated in VMC. This configuration exhibits a CPL behavior [15].

The total installed electrical power of 50 MW is provided by the two 25 MW (30 MVA) gas turbine generators. The voltage of the MVDC bus is ±6 kV and the voltage is stepped down to low-voltage dc (±1 kV) in load centers 1 through 4 via dc/dc converters. The main parameters of the scheme are shown in Table V.

Each main generation system includes: 1) a gas turbine with speed governor; and 2) a three-phase 25 MW (30 MVA) synchronous machine and excitation system (automatic voltage regulator). The load sharing among the two generators is achieved by droop control. The setting of the synchronous
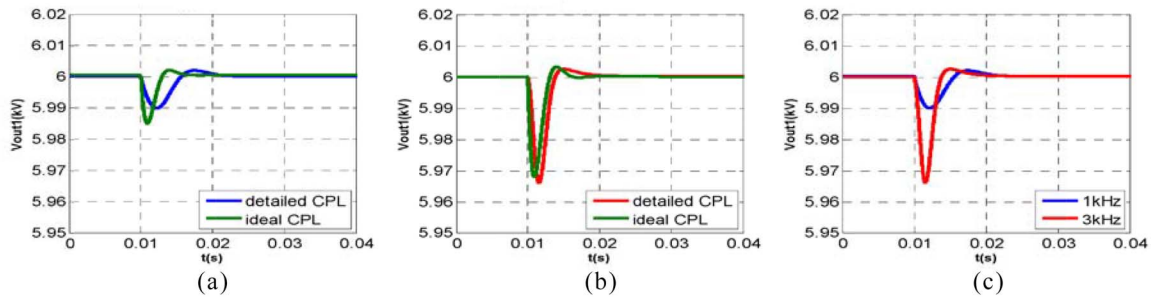
Fig. 7. Small signal [power level from 14 to 15 (rated power of CPL)]. (a) 1 kHz. (b) 3 kHz. (c) Comparison of 1 and 3 kHz.
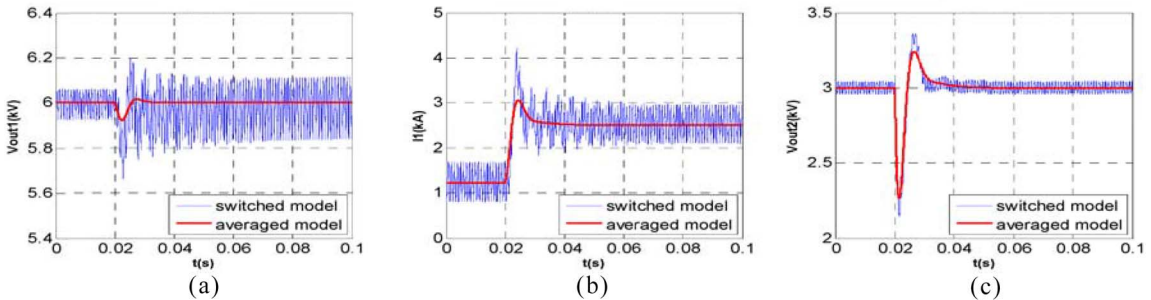


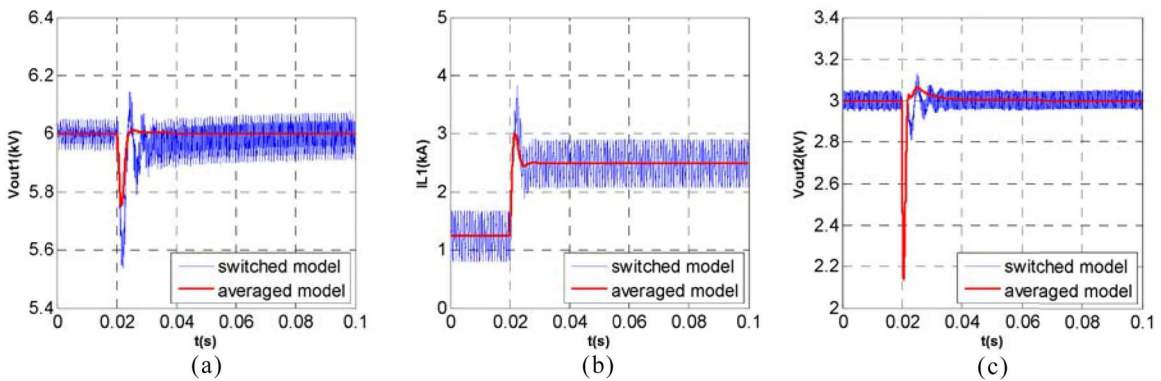Fig. 8. Large signal analysis (power level from 7.5 to 15 MW)—1 kHz CPL. (a) $V_{out1}$. (b) IL1. (c) $V_{out2}$.



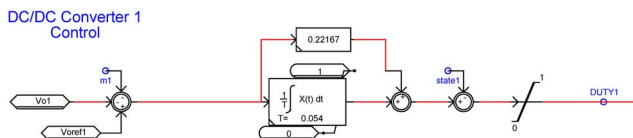Fig. 9. Large signal analysis (power level from 7.5 to 15 MW)—3 kHz CPL. (a) $V_{out1}$. (b) IL1. (c) $V_{out2}$.



Fig. 10. Control block of the dc voltage regulator.



Fig. 11. Closed-loop bode diagram of dc zone load—voltage control—bandwidth $5300\omega$.

generator was done according to [34] and the excitation system of type ST1 was set according to [35]. The topology chosen for the generation side interfacing converter (LRC) is a diode rectifier coupled to a buck dc–dc converter. The bus voltage control method of the LRCs is the same as in Section VII-B, where a linearizing state feedback control strategy [11], [12] is implemented to linearize the overall system behavior, so that the theoretical assumption of Section IV remains valid. Fig. 10 summarizes the control scheme where "state1" is the sum of linearization function and state feedback function
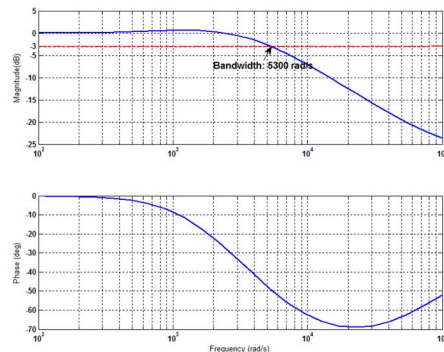
for each generator interface converter and "m1" is the current feedback loop for load sharing.

Considering that the derivative in the feedback function may exasperate noise in the control loop, the derivative of
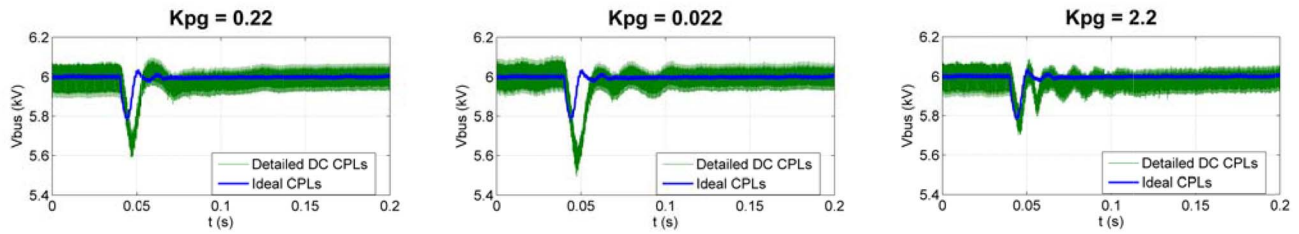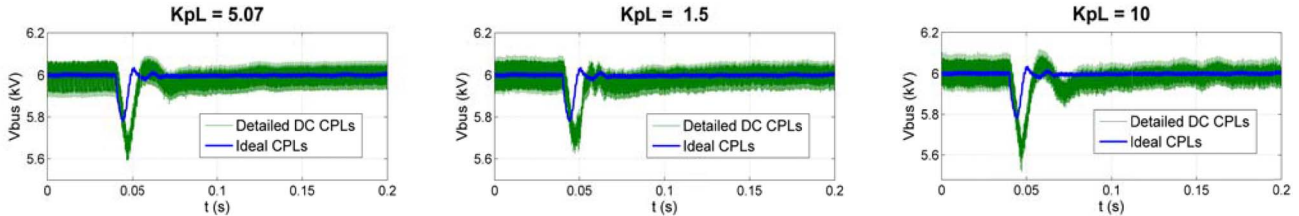
Fig. 12. Variation of generation-side bandwidth.



Fig. 13. Variation of POL bandwidth.

TABLE VI
LINEARIZING STATE FEEDBACK CONTROL PARAMETERS—LRC

|         | Condition 1 | Condition 2 | Condition 2 |
|---------|-------------|-------------|-------------|
| $K_1$   | 3.465       | 3.465       | 3.465       |
| $K_2$   | 580         | 580         | 580         |
| $K_{pg}$| 0.022       | 0.22        | 2.2         |
| $K_{ig}$| 0.054       | 0.054       | 0.054       |

TABLE VII
PID CONTROLLER PARAMETERS FOR EACH POL CONVERTER

|         | Condition 1 | Condition 2 | Condition 3 |
|---------|-------------|-------------|-------------|
| $K_{pl}$| 1.5         | 5.07        | 10          |
| $K_i$   | 2e-4        | 2e-4        | 2e-4        |
| $K_d$   | 1.75e-6     | 1.75e-6     | 6.5417e-8   |

the bus voltage (which is one of the feedback state variables) is substituted by the current of capacitor branches in the output filters of the generator interface converters.

The buck converter output low-pass filter is designed according to the same specifications as in Section VII-A and provided in Table V. A PID controller is used for the load center with the parameters provided in Table VII. An anti-windup [36] is added to avoid the saturation of the integral, which may happen at the moment the load is connected to the bus. The resulting close-loop bode diagram of the system is depicted in Fig. 11.

A load increase of 12.5 MW is performed during the simulation. We performed simulation runs for different control parameters of the generation side and the load side. The variation was done on the proportional part of the controller to increase the bandwidth of the LRC or the POL converter. The coefficients are stated in Tables VI and VII.

The simulation results are presented in Figs. 12 and 13. It can be observed in Fig. 12 that the voltage drop in the case of the detailed CPL model is higher than in the case of an ideal CPL when the bandwidth of the detailed CPL (influenced by

the POL converter PID control) is higher than the ideal CPL (determined by bus voltage).

As $K_{pg}$ increases, the bandwidth of the system increases, therefore, the observed system behavior while loaded with a detailed CPL approximates the one of an ideal CPL. It can be seen in Fig. 13 that when $K_{pl}$, which is the control parameter of the POL converter's PID controller, increases, the bandwidth of the detailed CPL and approximates the behavior of the ideal CPL. The simulation shows that increasing the control bandwidth of the 3 kHz CPL, the observed voltage drop on the bus is also increasing in comparison with the ideal CPL. The simulation also reveals that when increasing the bandwidth of the LRC converters the simulated system behavior approaches the one of the ideal CPL. Additionally, it is observed an interdependency between the control bandwidth of the LRC and POL converters and that the theory introduced Sections III–V are not only valid in a single LRC single CPL system but also for multimachine systems.

IX. CONCLUSION

This paper has focused on the derivation of the small signal transfer functions of voltage mode regulated converters for a cascaded system. Main goal is to achieve a realistic model of the so-called CPL behavior. Result of the analysis is an impedance-based model that appears to be a more realistic approximation.

Focus is placed on how the load through the POL converter interacts with the generating unit and LRC converter.

With the help of small and large-signal simulations, the analytical hypothesis is verified. The comparison was extended to include the dynamic interaction among different converters and loads, where the observation is consistent with the theoretical background.

Moreover, it was shown that CPL assumption is dynamic wise not always the worst-case condition. The transient influence of the other load types were also analytically presented via an equivalent impedance modeling method.

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