Bulk-Si Platform: Born for DRAM, Upgraded With On-Chip Lasers, and Transplanted to LiDAR

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***Abstract*—The CMOS industry has been expecting silicon photonics to provide photonic and electro-photonic integrated circuits based on the CMOS processes and infrastructures for scalability of incumbent technology evolutions and creation of novel technologies. However, the compatibility with the legacy CMOS has been compromised with the development convenience of early silicon photonics in that the specialty silicon-on-insulator substrates have been widely used as integration platforms. Since this specialty substrate may hinder the photonics integration with legacy volume products later, a legacy-friendly integration platform with a generic bulk-silicon substrate has been developed for better compatibility. This paper overviews the bulk-silicon photonics platform born for DRAM integration, upgraded with III/V-on-bulk-Si lasers, and transplanted to LiDAR applications requiring the virtuous cycle of cost and volume. The photonics integration with DRAM was to resolve the speed-capacity trade-off in the DRAM interconnects, and technical feasibility as well as lessons learned from the integration attempt are reviewed. The bulk-silicon device performance approaches that of silicon-on-insulator devices with the thermal advantage of ∼40-% lower thermal impedance and the optical disadvantage of ∼0.4-dB/mm higher waveguide loss. In the LiDAR applications, detection performance up to ∼20 m at 20 fps by a single-chip scanner integrating tunable laser, semiconductor optical amplifiers, and optical phased array are presented with future outlooks.**

***Index Terms*—DRAM, heterogeneous integration, LiDAR, optical interconnect, silicon photonics.**

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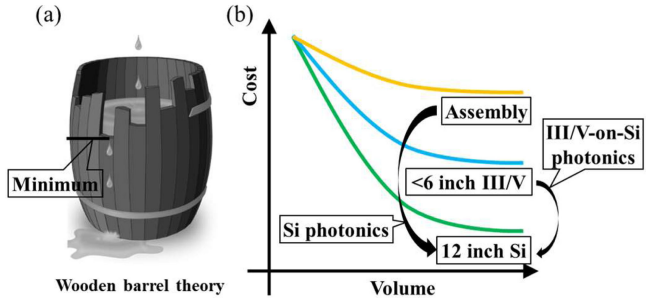

Fig. 1. Conceptual illustration of the rationale behind Si photonics and III/V-on-Si photonics. (a) Minimum dictates the overall performance or cost. (b) Volume-cost curves for assembly, III/V, and Si technologies.

I. Introduction

From the industry perspective, silicon(Si) photonics has begun to fabricate photonic integrated circuits(PICs) and electro-photonic integrated circuits(EPICs) using the existing complementary-metal-oxide-semiconductor(CMOS) process facilities and production infrastructures [1]–[9]. By doing so, it has been expected that photonics could enjoy the transistor revolution that took place in the mid-20th century in electronics [10], [11]. Fig. 1 illustrates the industry expectations on Si photonics and III/V-on-Si photonics. In most modern systems combining Si semiconductors, III/V compound semiconductors, and discrete assemblies, the volume cost is mostly dictated by the assembly first and the III/V next, due to the current differences of the industrial production scales. While the Si semiconductor had reduced its volume cost down to the lowest level thanks to the transistor revolution and the subsequent CMOS evolution, the photonics has just begun to reduce its volume cost entering the 21st century with the advent of Si photonics [1], [4]. As the cost of the photonics assembly has been reduced by the Si photonics, the III/V has become the next cost bottleneck to overcome. Since the III/V cost primarily comes from its smaller production scales, the III/V-on-Si photonics combining the III/Vs to the established bigger-scale Si production processes has attracted great industrial interest, and has paved the way for commercialization [2], [6], [8].

Beyond intra-photonics integration, by integrating the PICs into the electronics, it has been also expected to cope with

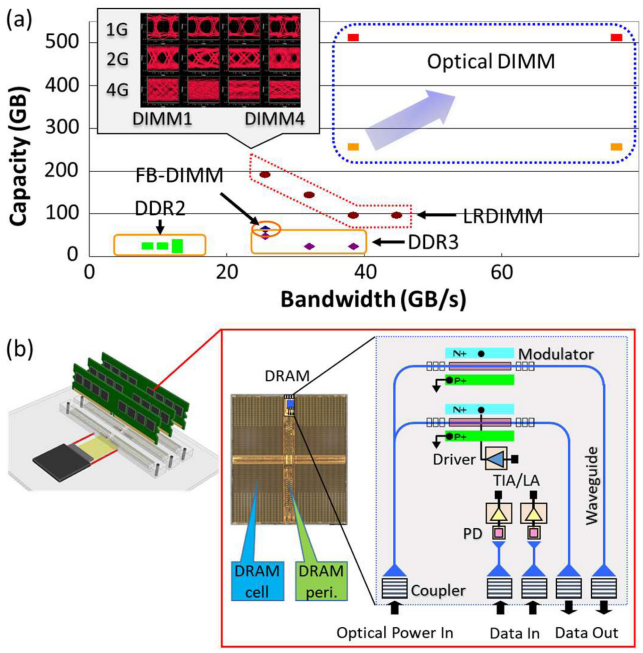

Fig. 2. The first attempt to integrate photonics into legacy VLSI. (a) Memory module trend in ∼2010. (b) Concept of DRAM photonic I/O in ∼2010.

technical problems that are difficult to solve with electrical engineering only [5], [7]. One example is the speed-capacity trade-off in the dynamic random access memory(DRAM) interconnects as depicted in Fig. 2(a) [12]. Around 2010, the traditional multi-drop memory bus architecture confronted the technical problem that the input-output(I/O) speed and the memory module count cannot increase independently. It was due to the increasing complexity of the electrical impedance matching over increasing I/O speeds in the multi-module configurations. Since this electrically complicated problem becomes virtually a single-frequency problem in the optical domain, the bold research-level attempt embedding PICs into DRAM was made around 2010 [12]–[24]. Note that the on-chip integration was chosen because of the tight cost expectation of the commodity DRAM. This was the first attempt to integrate photonics directly into the legacy very-large-scale integration(VLSI) technology on the generic platform, and to the best of authors' knowledge, it is still the only one so far.

From the industrial background of the photonic and electro-photonic integrations, it is quite important to ensure compatibility with existing CMOS infrastructures, and for this purpose, Si photonics is required to inherit the existing CMOS technology as much as possible. However, the initial development of Si photonics has been relying on less compatible specialty substrates such as silicon-on-insulators(SOIs) mainly due to the convenience of waveguide formation, whereas most volume CMOS products use the generic bulk-Si(BS) substrate. It is interesting to note that this substrate preference originates from the fundamental difference between electrons and photons, which are fermions and bosons, respectively. While delivering fermionic electrons without leakage to the substrate can be easily done by controlling dopants or using metal lines, delivering bosonic photons without the substrate leakage needs a wavelength-thick dielectric underclad layer. Because of this underclad layer, the SOI platform has been established as the dominant integration platform for Si photonics so far. Redeveloping Si photonics on the generic BS substrate required challenging process and device developments, but it could promise many merits including low substrate cost, backward compatibility to volume products, flexible underclad structure, and efficient heat dissipation. The compatibility advantage of the BS platform was demonstrated in the DRAM integration attempt as shown in Section II. Moreover, the thermal advantage was also verified in the on-chip laser development as shown in Section III.

Fig. 3 illustrates the photonics integration schemes over possible generations for legacy-free and legacy-driven applications. For legacy-free applications, the integration scheme is flexible and application-dependent. However, for legacy-driven applications which are of more interest from the CMOS industry, critical difference exists in high and low ends. In the performance-centric high ends, one can adopt the specialty SOI platform and the single-chip integration with legacy could be optional. In the cost-sensitive low ends, the generic BS platform is preferred to avoid any constraints from photonics on legacy, which makes the final single-chip integration to be confirmed first. This was the rationale behind the BS platform development for future DRAM applications.

This paper consists of 5 sections each on introduction, DRAM application, III/V-on-BS platform, solid-state light detection and ranging(LiDAR), and future application possibilities. In the DRAM application section, we review the key process of the BS platform and the photonics integration into DRAM with succinct feasibility summary. Lessons learned from the DRAM attempt are also presented in high level. Then, the BS device library including III/V-on-Si lasers and SOI-BS platform comparison are summarized in the III/V-on-BS platform section. The solid-state LiDAR section presents the motivations for LiDAR applications, initial results from III/V-on-BS optical phased arrays(OPAs), BS-to-SOI library conversion under process environment change, up-to-date progresses of OPA-based LiDAR chip and module, and future LiDAR outlooks. Finally, future application possibilities using the III/V-on-Si technology are discussed in the final section.

II. DRAM Application

There have been a series of reports on the BS photonics and its application to DRAM [12]–[24]. In Section II, we review the key results and summarize lessons learned from the DRAM integration.

A. SPE Process

Fig. 4(a) illustrates the cross-sections of the SOI and BS platforms. Whereas the SOI platform has the global underclad layer, that is more friendly to PICs, the BS platform has the local underclad, that is more friendly to CMOS ICs. It should be stressed that this substrate change is not simple starting material change but directly affects several subsequent steps in the entire

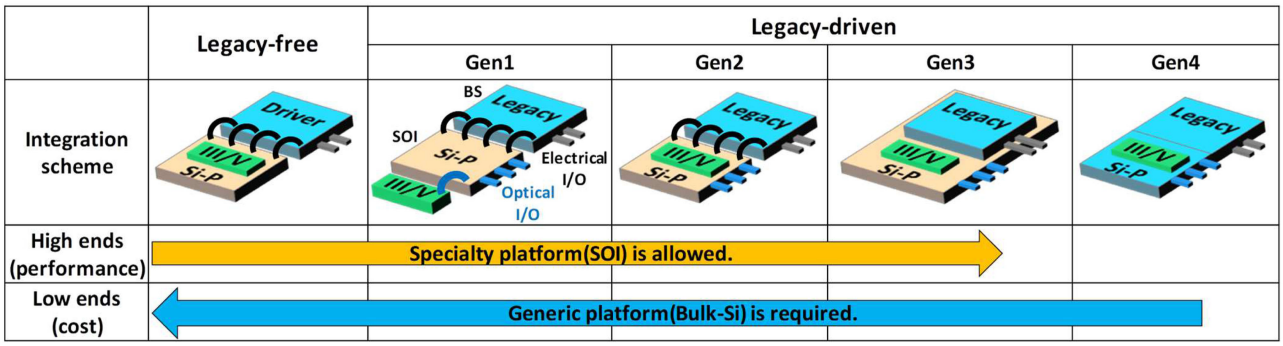

Fig. 3. Conceptual illustration of photonics integration with legacy.

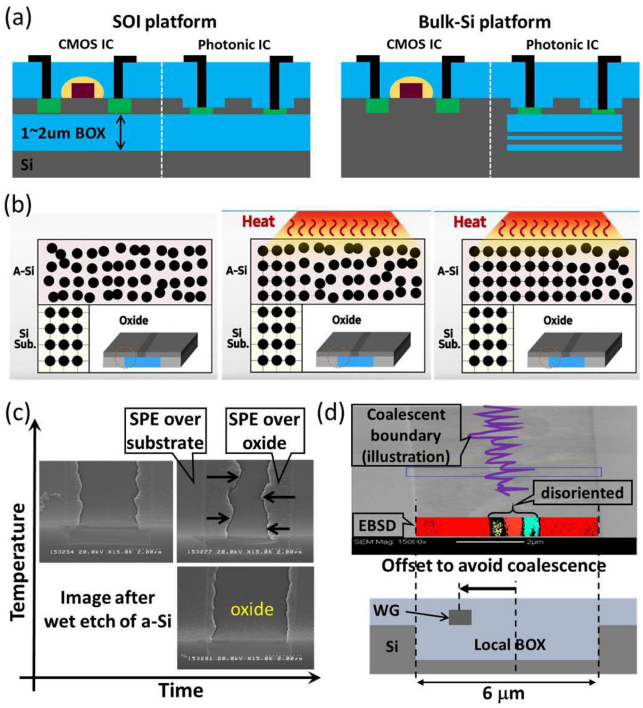

Fig. 4. BS platform and SPE process. (a) Cross-sections of SOI and BS platform. (b) Principle of SPE. (c) SPE process optimization. (d) SPE structure optimization. The crystallinity of the SPE Si was analyzed in the electron backscatter diffraction(EBSD) image.

process flow and overall device and circuit performances, resulting in the platform change as shown in Section III. Fig. 4(b) illustrates the SPE process for crystallizing the amorphous Si layer deposited on top of the local underclad through carefully-controlled thermal annealing processes. Note that the crystallization starts from the crystalline surface of the BS substrate, and laterally propagates over the local buried oxide(BOX). The lateral epitaxial fronts propagated from both sides collide in the middle, inevitably forming the coalescence boundary with poor crystallinity on top of the BOX center. In the SPE development, the process parameters including temperature and time were optimized as in Fig. 4(c), and the structure parameters including the BOX width and the offset position of the waveguide(WG) were optimized as in Fig. 4(d). Note that the WG is offset from the BOX center to avoid the coalescence boundary. The details of the SPE can be found in the previous reports [13]–[15].

B. Process Flow and Chip Structure

The process flow to embed the PIC into DRAM is briefed in Fig. 5(a). The photonics processes were integrated into the 12-inch 65-nm DRAM periphery process with the DRAM capacitor process skipped at the initial attempt. Except the photonics underclad layer formed before the shallow trench isolation(STI) of DRAM, most photonics devices were processed after the source/drain activation of DRAM transistors to minimize process perturbation to DRAM. The main process integration problems included heat budget, step height, and boundary treatments, and the resultant process overhead was less than 20% in 2010. For SOI-based legacy applications, there has been an integration approach to combine the SOI-based photonics and BS-based electronics all on the SOI substrate [25].

The lateral and vertical structures of the fabricated chip are summarized in Fig. 5(b) and (c). The PIC was embedded in the DRAM periphery section along with its EIC driver. The area overhead of the EPIC was calculated to be less than 1%. The PIC included 3 modulators, 3 photodiodes(PDs), 15 grating couplers for optical fiber, passives, and WGs, but no on-chip laser at that time. The modulator was a PIN-type Mach-Zehnder modulator. The PD was a butt-coupled PIN-type Ge PD. The EIC included 2 4:1 serializers and 2 1:4 deserializers for (de)multiplexing the 8 electrical signals to 2 optical signals, 2 modulator drivers, 2 trans-impedance amplifiers(TIAs) and limiting amplifiers(LAs) for 2 PDs, and clock tree circuit. Details of the EPIC can be found in the previous reports [19], [21], [24]. In short, the PIC and EIC were physically integrated side-by-side, but not chemically because of design rule conflicts at the moment. It was all due to maturity difference between the photonics and electronics around 2010.

C. Feasibility

In the co-fabrication of the DRAM and PIC, the main concern was whether the DRAM transistors and photonic devices attack or degrade each other. Fig. 6(a) shows the DRAM periphery transistor performance before and after the photonics integration. Whereas the NMOS transistor remained in the target range,

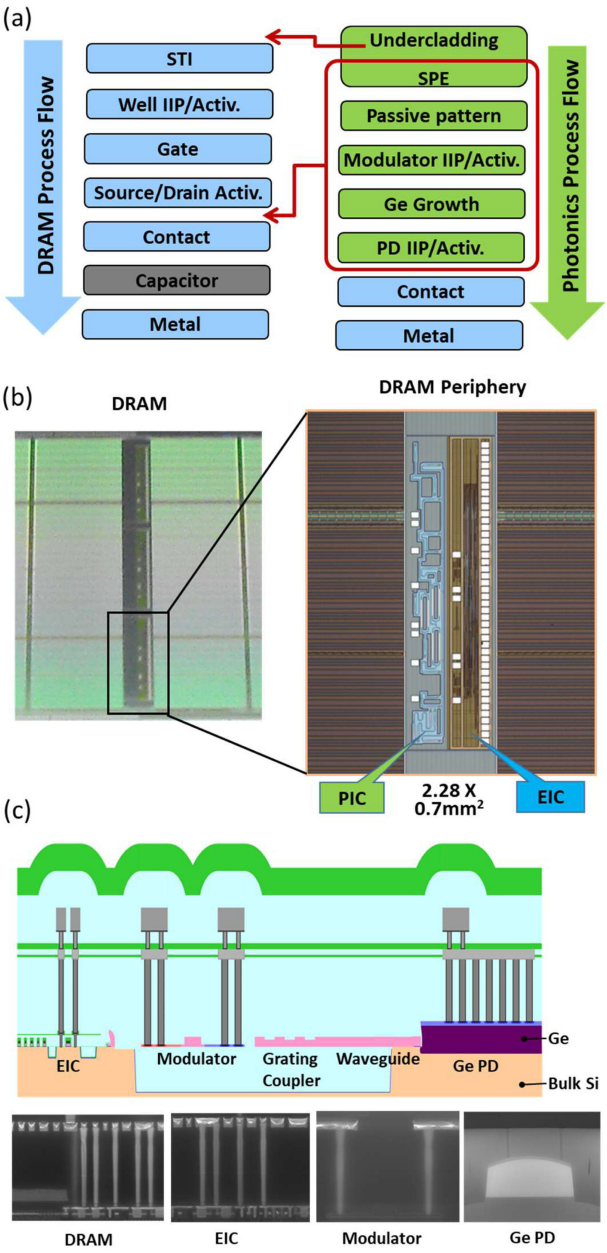

Fig. 5. Process flow and structure of PIC-DRAM integration around 2010. (a) Overall process integration. (b) Optical microscope images of the fabricated structure. (c) Conceptual illustration and SEM images of cross-sections of the fabricated structure.

the PMOS transistor moved out of the range. The degradations were mostly due to diffusion problems, which were corrected in following lots. Fig. 6(b), (c), and (d) show the performances of the co-fabricated modulators, which were similar to PIC-only ones. On the other hand, the co-fabricated PDs showed the bandwidth degradation from 20 Gbps to ∼6 Gbps as shown in Fig. 6(e), (f), and (g), mainly due to diffusion problems. The low PD responsivity was due to the grating coupler loss of ∼7 dB from unoptimized cladding layers at the moment. Despite the PD bandwidth degradation, the co-fabricated PIC functioned well for the DRAM interconnect designed to operate at 6.4 Gbps. Summarizing the device-level feasibility, the photonic devices

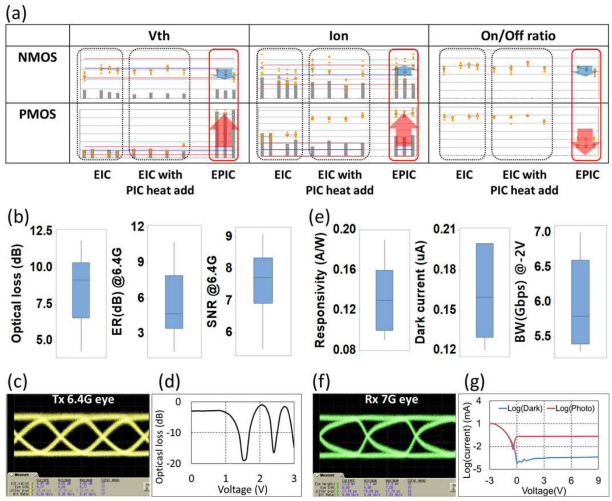

Fig. 6. Device-level feasibility from co-fabricated PIC and DRAM. (a) DRAM periphery transistor performance before and after the PIC-DRAM integration. (b) Overall performance of modulators integrated in DRAM. (c) 6.4G eye diagram with a modulator driven by an external driver. (d) Modulator DC performance. (e) Overall performance of PDs integrated in DRAM. The SNR was measured at bias voltage of −2V and SNR of 7. (f) 7G eye diagram with a PD driven by an external driver. (g) DC performance of PD.

and DRAM transistors were not very friendly to each other, but not very hostile either.

The grand vision was the DRAM optical interconnects with the on-chip PIC. Although the device-level feasibility was achieved, the system-level demonstration was significantly more complicated with packaging and control difficulties. Thus, we started with memory modules with off-chip optical memory buffers(OMBs), which were the periphery sections separated from the co-fabricated DRAM chip. The OMB consisted of the EIC co-fabricated with DRAM, and PIC fabricated from photonics-only processes with a larger size to accommodate a fiber array block for optical packaging. Fig. 7 summarizes the system-level feasibility achieved with the co-fabricated OMBs. In the demonstration, the optical memory link interconnected 1 memory controller and 4 memory modules in a single memory channel, which was not possible with a copper-based memory link around 2010. The memory controller was emulated by the field programmable gate array(FPGA)-based system shown in Fig. 7(b). The 1:4 multi-drop memory bus was emulated by an optical fiber splitter. The memory chip was 1600-MT/s double-data-rate3(DDR3) DRAM. The OMBs were in between the controller and 4 DRAM modules delivering the high-speed data optically without the aforementioned speed-capacity trade-off. The electro-photonic conversion was from 8 × 1.6 Gbps electrical signals to 2 × 6.4 Gbps optical signals bi-directionally. Fig. 7(c) shows that 32-bit data patterns were written to the DRAM, the controller sent the read command to the DRAM, and the return data were verified at the controller. Details of the system feasibility can be found in the previous reports [22], [24].

D. Lessons Learned

A decade has passed since the DRAM integration attempt around 2010, and 5 key lessons have been learned from the

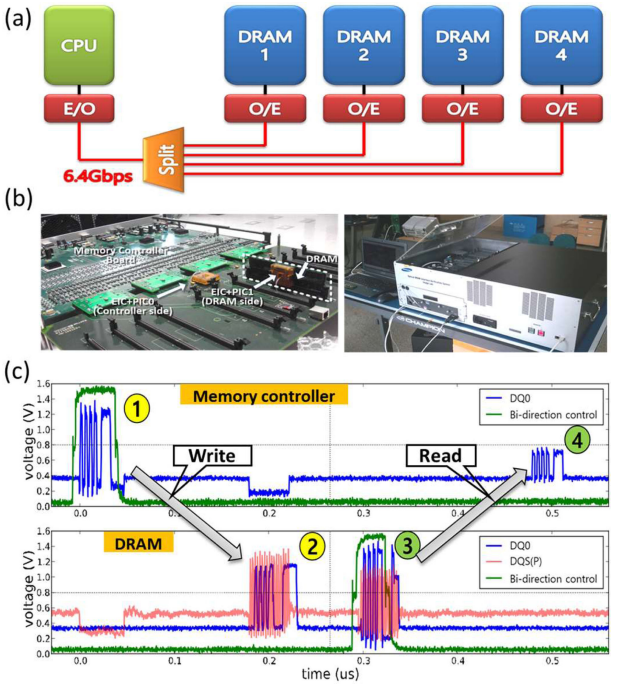

Fig. 7. System-level feasibility of DRAM optical interconnects. (a) Link configuration of the DRAM interconnect for 4 DDR3 DIMMs/channel. (b) Demonstration system. (c) Oscilloscope traces for data and clock signals to and from DRAM.

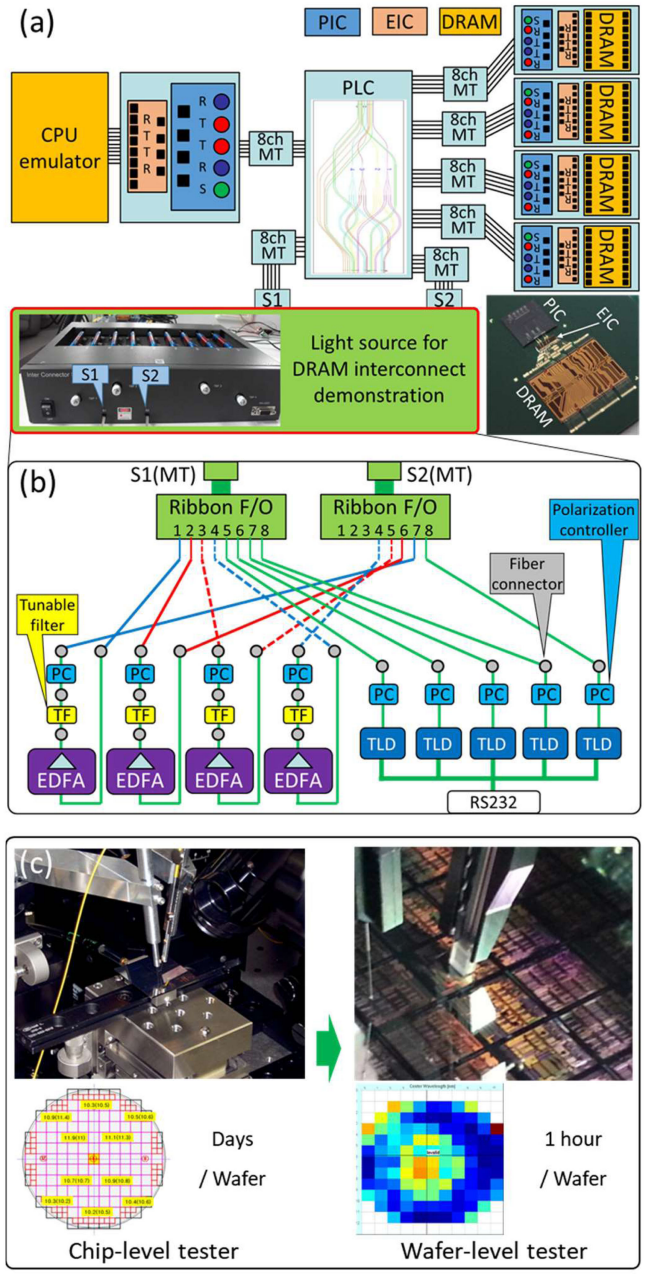

Fig. 8. Challenging issues confronted in DRAM interconnect development. (a) Illustration of the external light source feeding the photonic I/Os of the DRAM interconnect. The PLC was a custom silica-based planar lightwave circuit for optical routing. (b) Internal structure of the external light source. (c) Chip-level and wafer-level in-house testers built for Si photonics.

experience. The first one was about the light source. In 2010, we built the custom external light source as shown in Fig. 8(a) and (b). Since there were 1 processor and 4 memory modules, the light source had 5 wavelength-tunable laser diodes(TLDs) against PIC deviations. There were also 4 optical amplifiers to compensate PIC optical losses at that time. Therefore, there were 9 polarization controllers, messy optical routing, and many ribbon fiber connections. The resultant size of the external light source was 31 $\times$ 27 $\times$ 7 cm, which was considered impractical for future DRAM applications. This experience made authors realize that the light source better goes on-chip especially for low-end products like DRAMs, and it became the rationale for the on-chip laser development in Section III. The second lesson was about the industrial eco-system. Since there were little eco-systems available for Si photonics around 2010, we tried to internally build the development environments for simulation, test, and packaging which turned out to be very challenging and inefficient. For example, the wafer-level tester had been internally developed to reduce the test time of Si-photonics wafers as shown in Fig. 8(c). The tester was decent, but often limited beyond initial research activities. This gave authors the second lesson that the electro-photonic integrated eco-system is critical for PICs and EPICs. The third lesson was about timing for volume applications. The DRAM-related efforts made authors learn that the application timing of integrated photonics in volume is likely to depend on the CMOS evolution rather than on photonics itself. The fourth lesson was about application itself. It turned out that replacing existing electrical options with photonics is very challenging, and photonics should be inevitable in the target applications. The fifth lesson was about scalability. CMOS-like scalability is needed to go along with CMOS. From the conventional shrinkage perspective, photonics has the fundamental scalability limit imposed by its wavelength, so that it is required to secure scalabilities in other dimensions such as wavelength division multiplexing(WDM).

III. III/V-On-BS Platform

Starting with the basic devices originally developed for the DRAM integration, the BS platform has been continuously upgraded by adding new devices, and finally transitioned to the

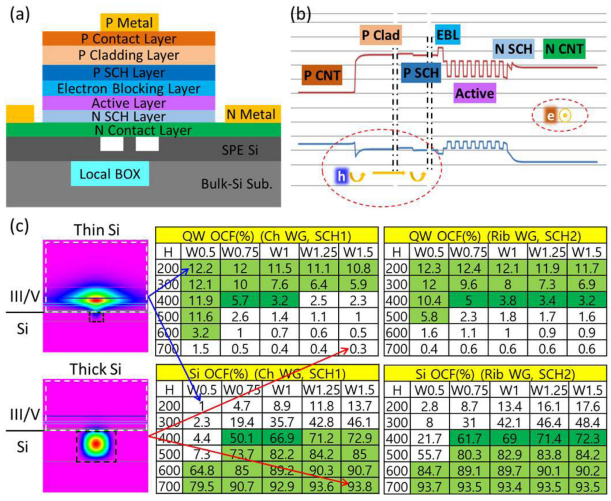

Fig. 9. BS platform cross-section. (a) Vertical structure of BS platform. (b) Exemplary band diagram of the III/V layers. (c) OCF dependence on WG width(W), WG height(H), and III/V structure. The width and height are in μm and in nm, respectively.

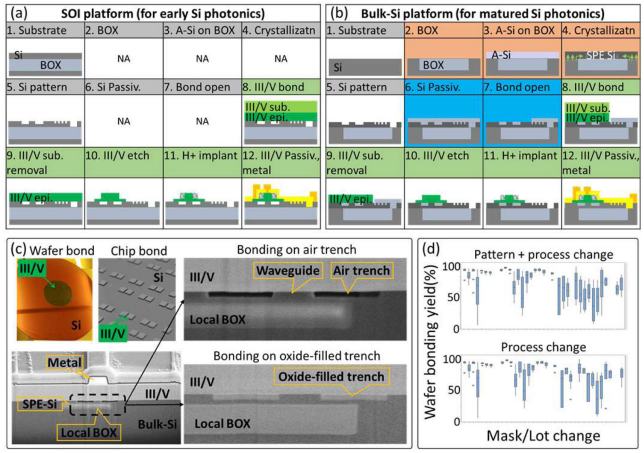

Fig. 10. Process flow and bonding process of III/V-on-BS platform. (a) Process flow of III/V-on-SOI platform. (b) Process flow of III/V-on-BS platform. (c) III/V-on-BS bonding interface. (d) III/V-on-BS bonding yield status.

III/V-on-BS platform with the on-chip laser and amplifier. In Section III, we summarize the vertical structure, process flow, up-to-date device performances, and thermal analyses of the III/V-on-BS platform

A. *Vertical Structure of III/V-On-BS Platform*

In the III/V-on-Si devices, the optical mode resides in the III/V-Si interface, where the III/V section amplifies or absorbs the mode and the Si section filters or reflects the mode. In the vertical structure, the key parameters are the thicknesses of the various III/V and Si layers as illustrated in Fig. 9(a). The III/V structure is basically an inverted separate confined hetero-structure(SCH) including the multiple-quantum-well(MQW)-based active layer, electron blocking layer, cladding layer, and contact layers. The exemplary band diagram of the III/V layers is shown in Fig. 9(b). In the III/V-on-Si platform, the III/V-Si co-design is critical, so that the Si thickness should be optimized according to the III/V structure and vice versa. Despite the challenging process development of crystallization, the BS platform provides a flexible Si thickness, which has been especially effective in the III/V-Si co-design. Fig. 9(c) illustrates the optical confinement factors(OCFs) depending on the WG width, WG height, and the III/V SCH. The QW and Si OCFs indicate the optical mode distribution over the III/V and Si sections, respectively. Since the optimal mode distribution depends on devices, the Si thickness of the platform should be carefully designed in consideration of key devices and coupling loss between III/V-on-Si and Si-only devices. In most PICs, top device priorities are usually on lasers or amplifiers. The Si thickness of the III/V-on-BS platform in Samsung has been 350 nm through design-process-test iterations [33].

B. *Process of III/V-On-BS Platform*

Fig. 10(a) and (b) compare the process flows of the III/V-on-SOI and III/V-on-BS platforms to disclose the added steps for the BS platform. The underclad and crystallization differences in the step 2, 3, and 4 have been discussed in Section II, and the differences in the step 6 and 7 are from the wafer bonding for early research and the chip bonding for matured production. For the chip bonding, the patterned Si surface should be protected by the passivation in the step 6, and the bonding regions should be selectively open in the step 7. Fig. 10(c) shows the fabricated bonding interfaces. Note that it is the direct bonding without any intermediary layer between III/V and Si. The bonding on the air trench has been used for research, and the bonding on the oxide-filled trench has been also tried to prepare future production. Fig. 10(d) shows the poor bonding yields on the BS platform so far. The bonding yield has been unstable yet, and been sensitive to pattern and process changes, presumably because the surface flatness of the SPE Si has been worse than that of SOI Si, which remains to be improved by further process developments. The pattern-dependent yield instability may imply that the flatness of the patterned silicon prior to the SPE process affects the bonding yield. Further process details can be found in the previous reports [33], [34], [37].

C. *Performance of III/V-On-BS Platform*

Fig. 11 summarizes the performances of the 12 devices in the III/V-on-BS platform so far. The first 4 devices are III/V-on-BS devices, and the other 8 devices are BS devices. Overall, the BS device performances are approaching the SOI device performances [26]–[31]. However, the BS WG loss is relatively higher than that of the SOI WG, because of the imperfect crystallinity of the SPE Si. In addition, the nonlinearities of the BS WG could be of concern for high-power applications, and remain to be analyzed further. Fortunately, the WG loss and nonlinearity can be reduced with rib WGs. The electrical resistance also marginally increases due to the imperfect crystallinity of the SPE Si. However, the resistance increase and its impact to the device speed have been insignificant as shown in the 25-Gbps lasers, modulators, and photodiodes successfully developed on

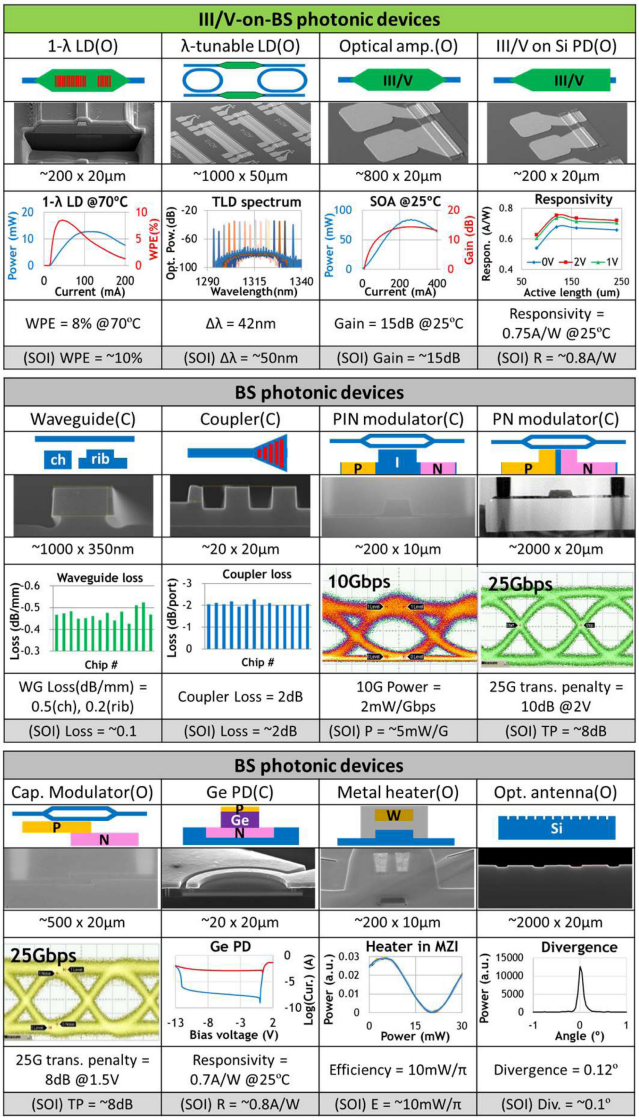

Fig. 11. Performance summary of III/V-on-BS platform. The operating wavelength band of each device is indicated. The O and C means the wavelength bands around 1.31 μm and 1.55 μm. The fourth row is typical device size. The sixth and seventh rows are the key performances of BS and SOI devices. The SOI performances are not from the state of art results, but from devices with similar structures.

the BS platform. Details on the Si-only BS devices can be found in the previous reports [13], [14], and this section focuses on the III/V-on-BS devices, which have been recently added to the BS device library after the DRAM integration. The operating wavelength band of the III/V-on-BS devices has been the O band. This wavelength has been originally chosen for short-range Datacom applications, where low-cost uncooled packaging is preferred. The O band is also well suited for the LiDAR applications in Section IV, where the eye safety and ambient light rejection are critical.

The 1-λ LD is a distributed feedback(DFB) laser featuring wall plug efficiency(WPE) of 8% at 70 °C, side mode suppression ratio(SMSR) of 45 dB, direct modulation up to 25 Gbps at 17 °C, and mean time to failure(MTTF) of 46,000 hours at 70 °C. The TLD is based on the Vernier effect in a dual-ring cavity, and it features wide tuning range of 42 nm and SMSR of 30 dB. The 60-nm tuning range has been also reported by the same TLD design on the III/V-on-SOI platform [48]. The optical amplifier is basically the gain section embedded in the TLD, and it features optical gain of 15 dB at an input power of 4 dBm and maximum output power of 19 dBm. Further analysis on noise figure and spectral ripple remains. The III/V-on-Si PD is a reverse-biased optical amplifier with optimized length and width of the Si WG, and it features responsivity of 0.75 A/W and dark current of 150 nA at bias voltage of −1 V. Further analysis on the modulation bandwidth remains. Details of the III/V-on-BS devices can be found in the previous reports [33], [34]. The last missing key device for the library is the optical isolator, which allows the optical transmission in only one direction and prevents unwanted optical reflections [35]. From an industry point of view, the III/V-on-BS device library is still immature. This is mostly due to the low yields of the process, lack of numerical models for III/V-on-Si devices, uncertain material database for III/V, and overall immaturity in the III/V eco-system. The III/V-on-Si technology is a promising approach to raise the production scale of III/V to the Si level, but industry-scale efforts should be made to reduce the industrial maturity gap between III/V and Si.

D. Thermal Analysis on III/V-On-BS Platform

The DFB Laser converts electrical energy to optical energy with typical efficiencies around 10% and the remaining 90% of the energy is wasted as heat, so heat dissipation is critical for the laser. In the SOI, the global BOX blocks heat flow from the laser to the substrate. On the other hand, the local BOX in the BS allows efficient heat flow to the substrate, allowing the laser operates at higher optical power levels. This thermal advantage originates from the 100-times higher thermal conductivity of crystalline Si compared to oxide [32]. Fig. 12(a) shows a thermal simulation confirming that the operating temperature is lower in the BS platform than in the SOI in the same operating condition. This thermal advantage was quantified by the thermal impedance, that was measured by the thermal wavelength shift of the on-chip laser as shown in Fig. 12(b). In the BS platform, the thermal impedance was measured to be about 40% lower than in the SOI, and Fig. 12(c) shows that this translates to 52% higher optical powers at 70 °C. Details of the thermal analyses can be found in the previous reports [36]–[38]. Overall, the III/V-on-BS platform has the optical disadvantage of the higher WG loss, but has the thermal advantage of the lower thermal impedance, providing competitive advantage over the SOI platform in temperature-sensitive applications.

IV. SOLID-STATE LIDAR

From the lessons learned from the DRAM experience in Section II, it was recognized that small-scale commercialization of legacy-free applications could be a prerequisite for future commercialization of large-scale legacy-driven applications by bridging the industry maturity gap between the PIC and EIC. In Section IV, we summarize the motivation, single-chip OPA

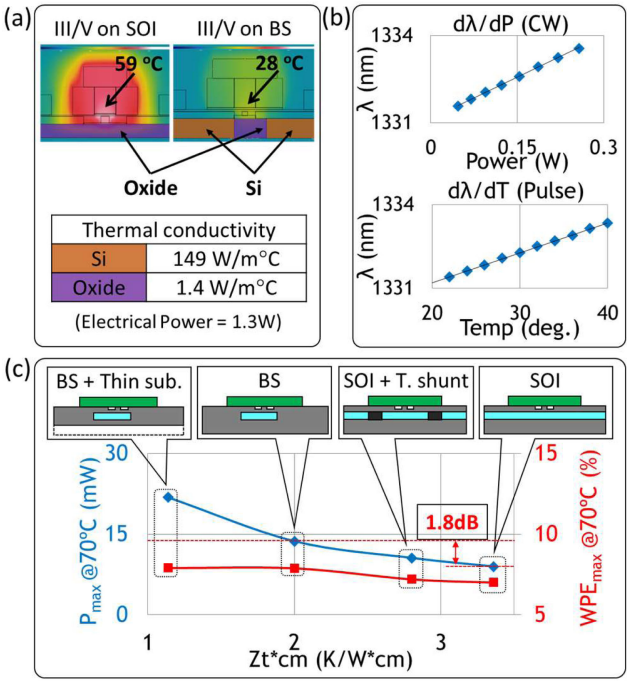

Fig. 12. Thermal analyses. (a) Thermal simulation. (b) Thermal impedance measurements. The wavelength shifts over power and temperature were measured by continuous and pulsed operations, respectively. (c) Thermal analysis with BS data and SOI simulation.

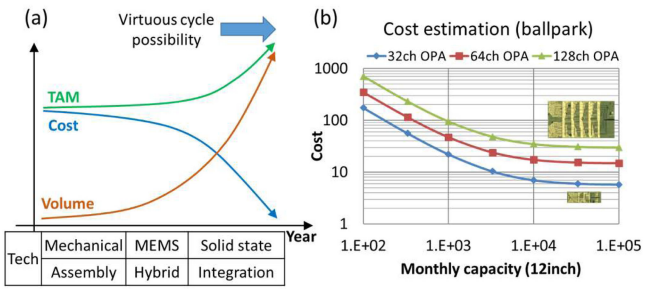

Fig. 13. Motivation of solid-state LiDAR. (a) Possible scenario of LiDAR evolution. (b) Cost-volume estimation for LiDAR chip.

architecture, chip-level and module-level performance, and outlook of the Si-photonics-based solid-state LiDAR.

A. Motivation of Solid-State LiDAR

Among legacy-free opportunities, the solid-state LiDAR appears destined for PICs, because it has been delayed by the cost and manufacturability that Si photonics was born for [39]–[47]. Fig. 13 illustrates the cost reduction capability of the Si-photonics-based LiDAR. From the cost reduction by simplifying the complex assembly with the PICs, the virtuous cycle of volume and cost may begin and infrastructure investments in the PICs may be justified. Fig 13(b) is the OPA cost estimation over volume with an assumption that a new 12-inch III/V-on-Si fabrication line is dedicated for the OPA production. In this estimation, the main cost factors are volume, chip size, and

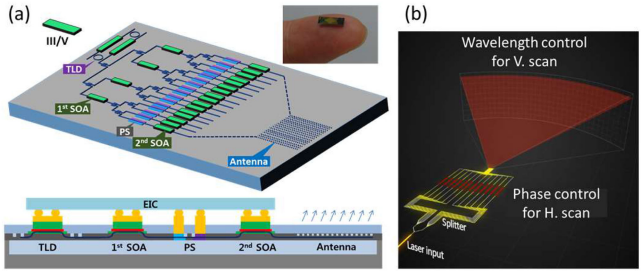

Fig. 14. (a) OPA architecture. (b) Principle of solid-state beam scan.

III/V material cost. When the volume is not high enough, mixed production at depreciated facilities might be considered.

B. Single-Chip OPA Architecture

There have been various architectures competing for LiDAR applications without clear commercial winners yet, and multiple architectures may co-exist depending on applications [47]. The LiDAR wavelength has been also unsettled, because the eye safety and ambient light rejection prefer longer wavelengths, and the industry eco-system and high-temperature requirement prefer shorter ones. In the III/V-on-BS platform in Section III, the only available wavelength is 1.3 μm at the moment, and we believe this wavelength is also well suited for LiDAR as it strikes the right balance of the wavelength issues. Fig. 14 shows the III/V-on-Si-based OPA architecture and beam-scanning principle. From the radio detection and ranging(RADAR) benchmark, the OPA and pulse time-of-flight(TOF) scheme have been chosen for initial development. The OPA includes 1 TLD, 36 semiconductor optical amplifiers(SOAs), 32 phase shifters(PSs), and 32 optical antennas. The combination of the TLD and 1 dimensional(D) OPA realizes the horizontal scan by the phase control over the OPA and the vertical scan by the wavelength control over the TLD. The antenna spacing is either periodic, random, or chirped. Details of the LiDAR chip design can be found in the previous reports [48]–[53].

The III/V-on-BS platform is well suited for the high-power OPA thanks to its low thermal impedance. However, the III/V-on-BS OPA implementation has been challenging due to its low device yield. Fig. 15(a) shows the imperfect performance of the III/V-on-BS OPA without the on-chip TLD. The OPA's line-shaped beam pattern was supposed to focus on a single point via phase control as shown in Fig. 15(c), but did not achieve a single point as only some of the 32 channels survived. Fig. 15(b) shows the beam pattern from the III/V-on-BS OPA with the on-chip TLD, where the multiple horizontal lines indicate that the TLD operated in a multi-mode with poor mode selectivity. While struggling with this yield challenge, the BS process became unavailable, and the III/V-on-BS platform was inevitably transferred to the SOI platform. Confronting the process environment change, the III/V-on-BS device library was converted to the III/V-on-SOI one by skipping the BS-related process steps and mask layers. For example, the mask change of the TLD test structure is illustrated in Fig. 15(d). It should be stressed that this conversion is one way only, and not vice versa.

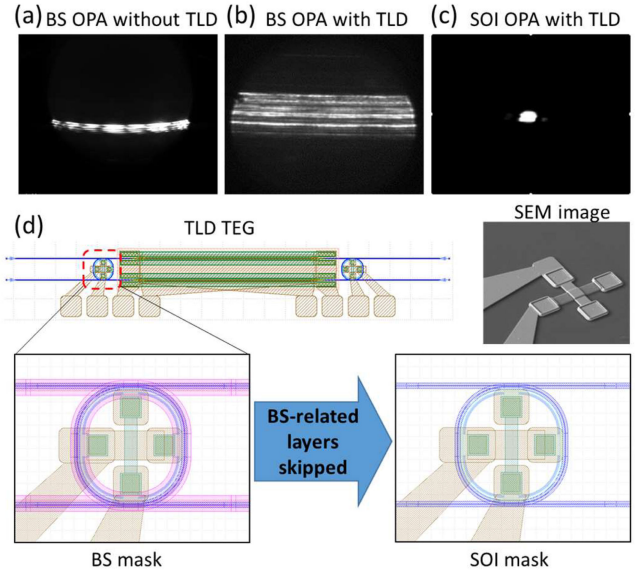

Fig. 15. (a) Imperfect beam pattern of BS OPA without on-chip TLD. (b) Imperfect beam pattern of BS OPA with on-chip TLD. (c) Beam pattern of SOI OPA with on-chip TLD. (d) Mask conversion from III/V-on-BS platform to SOI platform.

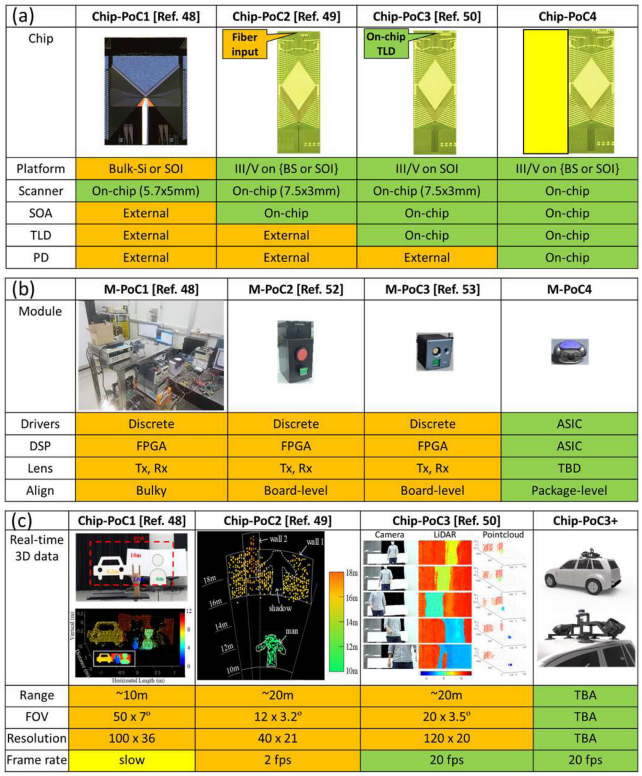

Fig. 16. Chip-level and module-level progresses. (a) Chip-level progress. (b) Module-level progress. (c) LiDAR performance progress.

C. LiDAR Progress

Fig. 16 summarizes the chip-level and module-level progresses so far. The photonic integration is ongoing toward the single chip as shown in Fig. 16(a). In the proof of concept1(POC1), the LiDAR chip was Si-only, and the SOA, TLD, PD were all external, bulky, slow, and expensive [48]. In the POC2, it became III/V-on-Si, and the SOAs were on-chip [49]. In POC3, the SOAs and TLD were on-chip [50]. The POC4 having everything on-chip is under development. The LiDAR module is getting smaller as shown in Fig. 16(b), but the module progress will be expedited after the LiDAR chip settles down. In the module POC1, it was a set-up rather than a module [48]–[50]. In the module POC2, it became the module in a table-top size [51]. In the module POC3, it became a palm-top size [53]. The module POC4 may adopt application-specific ICs(ASICs) to serve as a commercial prototype.

The imaging performance of the LiDAR module cannot compare to that of the mechanical LiDAR products yet, but meaningful progresses have been made as shown in Fig. 16(c). In the POC1, the 3D image had a relatively good resolution and field of view(FOV) thanks to a relatively large antenna count of 128, but its frame rate was slow due to its weak optical power requiring heavy accumulation of repeated measurements. In the POC2, the 3D real-time imaging had the frame rate of 2 fps, which was limited by the slow external TLD having mechanical tuning mechanism inside. Whereas the detection range was enhanced by the on-chip SOAs, the FOV was reduced by small antenna count of 32 and narrow wavelength window of the grating coupler for connecting the external TLD to the chip. In the POC3, the 3D real-time imaging frame rate was 20 fps thanks to the on-chip TLD, and the frame rate was limited by a signal accumulation count. Then, real-road trials having the modules on top of a real vehicle are ongoing. The detection ranges have been up to 20 m mainly due to limited OPA output powers, and range extension is ongoing as the device yield improves in the OPA. It should be emphasized that the outdoor range is hardly degraded compared to indoors, thanks to the wavelength of 1.3 μm. Progresses on the module architecture including the receiver and signal processing will be published elsewhere [53].

The commercialization of OPA-based LiDAR has many challenges in terms of scan speed, scan angle, frame rate, range, power consumption, and etc. As most of the challenges are interrelated, it is expected that the frequency modulated continuous wave(FMCW)-based range extension or multi-beam-based frame rate enhancement could address some of the challenges [47]. The system-level solutions such as 3D-2D fusion could be adopted as well [53]. In those efforts, the opportunities and challenges of the BS platform will be the high-temperature advantages thanks to the low thermal impedance, and the low device yields of the SPE Si, respectively.

D. LiDAR Outlook

Good references to anticipate the LiDAR technology evolution are RADAR and Telecom, each sharing a similar purpose and common enabling technology as LiDAR, respectively. Fig. 17(a) illustrates implications from the RADAR and Telecom evolutions. The RADAR started from early 20th century with the pulse scheme, but ended up with the FMCW scheme [54]. It was mainly due to the burden of the radio frequency(RF) power amplifier development. When the Telecom started from

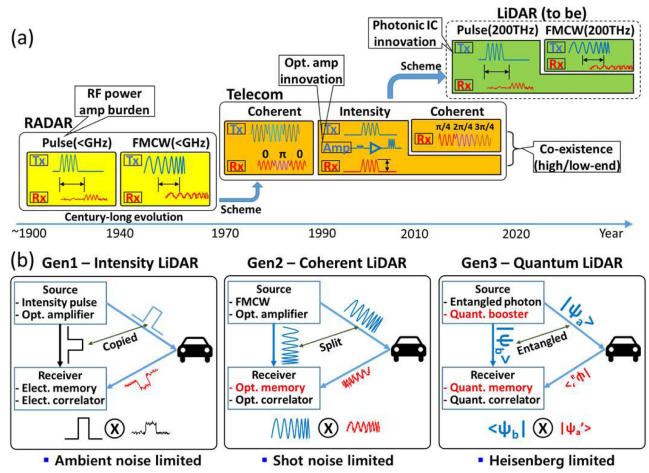

Fig. 17. (a) Implications from RADAR and Telecom evolutions. (b) Long-term LiDAR evolution outlook.

1970s, the coherent scheme was initially active, partially due to the RADAR influence. Then, it shifted to the intensity scheme, because of the well-known innovation of Erbium-doped fiber amplifiers(EDFAs) [55]. However, the coherent scheme came back for better performances, and they currently co-exist. For the LiDAR, the pulse scheme is currently ahead, and the lead may get prolonged if the on-chip amplifier is matured, but eventually it is more likely that the pulse and FMCW co-exist again. If this is true, it is important to make the platform prepared for both of the pulse and FMCW. So far, the III/V-on-BS(SOI) platform seems to provide all the necessary devices for the pulse scheme except the isolator, but this is not the case for the FMCW scheme, where FMCW-grade LDs with a narrow linewidth of around 100 KHz remain to be added. Fig. 17(b) illustrates the long-term LiDAR outlook consisting of the 3 generations(Gens). The Gen1 is the intensity LiDAR, and its up-to-date progresses are presented in this paper. The Gen2 is the coherent or FMCW LiDAR, and there have been several industrial frontiers with decent feasibilities mostly with assembly approaches. The Gen3 could be the quantum LiDAR, and some academic frontiers are discussing its possibilities. It seems that the III/V-on-Si platform takes industry at least to the Gen2, and it would be very interesting if it could lead us to the Gen3 in the future.

V. Future Application Possibility

The transistor revolution and volume-cost virtuous cycle of the CMOS technology have shaped the landscape of the modern electronics. The photonic version of the transistor revolution and virtuous cycle hold the potential to fundamentally change the landscape of the modern photonics, and probably extend to re-shape the landscape of the modern electronics as well. However, this requires a killer application where integrated photonics can overcome the high barriers to entry for industry-scale investments: the well-known chicken and egg situation. When industries are trapped in this situation, often breakthroughs have come from non-commercial drivers, which could also apply to the III/V-on-BS platform as well, especially in the high-power

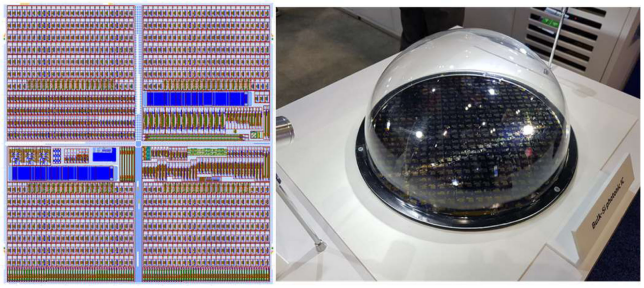

Fig. 18. Typical reticle and 12-inch wafer of BS platform.

laser applications [56]. In the well-known coherent beam combining(CBC) approach to the high-power lasers, scaling to a larger number of lasers with stable phase controls is required [57]. Fig. 18 shows the typical reticle and 12-inch wafer of the BS platform. The exemplary reticle contains ∼1200 LDs, and there are ∼120 reticles on the wafer, giving a total of ∼144,000 LDs on the wafer. For simplicity, we may assume that a single LD or SOA produces an optical power of ∼100 mW like the III/V-on-BS SOA in Fig. 11. If all LDs or SOAs on a single wafer can be coherently synchronized to combine all optical beams on a single point, the optical output can ideally reach KW-class power. This level of CBC has been elusive for fiber-based systems due to non-uniformity and fluctuation in optical path length. However, the large-scale CBC might be achievable with the Si-WG-based OPAs where the optical path lengths are uniform and stable even on the optical wavelength scale. The high-power optical beam combined with the solid-state high-speed steering may find future applications in the non-commercial sector. Note that higher device densities are possible using vertical cavity surface emitting lasers(VCSELs), but they are not suitable for the CBC. The nonlinearity in the light-matter interaction typically places upper limits on the optical powers, but it can be avoided in the distributed architecture of the OPA. Other key challenges are thermal management, linewidth for long-range coherence, and control complexity over a large number of LDs or SOAs. The low thermal impedance of the III/V-on-BS platform certainly facilitates the thermal management, and the linewidth feasibility of sub-KHz and controls over 8192 devices have been recently reported in Si photonics [58], [45]. It will be interesting to see how these opportunities unfold as industry advances with the III/V-on-Si technologies.

References

[1] R. Soref, "The past, present, and future of silicon photonics," *IEEE J. Sel. Topics Quantum Electron.*, vol. 12, no. 6, pp. 1678–1687, Nov./Dec. 2006.
[2] R. Won, "Integrating silicon photonics," *Nature Photon.*, vol. 4, pp. 498–499, 2010.
[3] Y. A. Vlasov, "Silicon CMOS-integrated nano-photonics for computer and data communications beyond 100G," *IEEE Commun. Mag.*, vol. 50, no. 2, pp. s67–s72, Feb. 2012.
[4] A. Rickman, "The commercialization of silicon photonics," *Nature Photon.*, vol. 8, no. 8, pp. 579–582, 2014.
[5] A. H. Atabaki *et al.*, "Integrating photonics with silicon nanoelectronics for the next generation of systems on a chip," *Nature*, vol. 556, no. 7701, pp. 349–354, 2018.
[6] J. E. Bowers, "Heterogeneous photonic integration on silicon," in *Proc. Eur. Conf. Opt. Commun.*, 2018, pp. 1–3.

[7] C. Doerr and L. Chen, "Silicon photonics in optical coherent systems," *Proc. IEEE*, vol. 106, no. 12, pp. 2291–2301, Dec. 2018.
[8] J. M. Ramirez *et al.*, "III-V-on-silicon integration: From hybrid devices to heterogeneous photonic integrated circuits," *IEEE J. Sel. Topics Quantum Electron.*, vol. 26, no. 2, Mar./Apr. 2020, Art. no. 6100213.
[9] N. Margalit *et al.*, "Perspective on the future of silicon photonics and electronics," *Appl. Phys. Lett.*, vol. 118, no. 22, 2021, Art. no. 220501.
[10] G. E. Moore, "Cramming more components onto integrated circuits," *Electronics*, vol. 38, no. 8, Apr. 1965, Art. no. 114.
[11] J. S. Kilby, "Invention of the integrated circuit," *IEEE Trans. Electron Devices*, vol. 23, no. 7, pp. 648–654, Jul. 1976.
[12] K. Kim, "From the future Si technology perspective: Challenges and opportunities," in *Proc. IEEE Int. Electron Devices Meeting*, 2010, pp. 1.1.1–1.1.9.
[13] D. Shin *et al.*, "Mach-Zehnder silicon modulator on bulk silicon substrate; toward DRAM optical interface," in *Proc. 7th IEEE Int. Conf. Group IV Photon.*, 2010, pp. 210–212.
[14] H. Ji *et al.*, "Bulk silicon photonic wire for one-chip integrated optical interconnection," in *Proc. 7th IEEE Int. Conf. Group IV Photon.*, 2010, pp. 96–98.
[15] H. Ji *et al.*, "Optical interface platform for DRAM integration," in *Proc. Opt. Fiber Commun. Conf. Expo. Nat. Fiber Optic Engineers Conf.*, 2011, pp. 1–3.
[16] K. Lee *et al.*, "10Gb/s silicon modulator based on bulk-silicon platform for DRAM optical interface," in *Proc. Opt. Fiber Commun. Conf. Expo. Nat. Fiber Optic Engineers Conf.*, 2011, pp. 1–3.
[17] J. Pyo *et al.*, "10 Gb/s, 1x4 optical link for DRAM interconnect," in *Proc. 8th IEEE Int. Conf. Group IV Photon.*, 2011, pp. 368–370.
[18] K. Ha *et al.*, "Si-based optical I/O for optical memory interface," in *Proc. SPIE 8267, Optoelectron. Interconnects XII*, 2012, Art. no. 82670F.
[19] D. Shin *et al.*, "Integration of silicon photonics into DRAM process," in *Proc. Opt. Fiber Commun. Conf. Expo. Nat. Fiber Optic Engineers Conf.*, 2013, pp. 1–3.
[20] J. Shin *et al.*, "Epitaxial growth technology for optical interconnect based on bulk-Si platform," in *Proc. 10th IEEE Int. Conf. Group IV Photon.*, 2013, pp. 3–4.
[21] B. Lee *et al.*, "Integration of photonic circuits with electronics on bulk-Si platform," in *Proc. 10th IEEE Int. Conf. Group IV Photon.*, 2013, pp. 1–2.
[22] H. Byun *et al.*, "FPGA-based DDR3 DRAM interface using bulk-Si optical interconnects," in *Proc. 10th IEEE Int. Conf. Group IV Photon.*, 2013, pp. 5–6.
[23] H. Ji *et al.*, "Box-less waveguide Ge PD for bulk-Si based silicon photonic platform," in *Proc. Opt. Fiber Commun. Conf., OSA Tech. Dig.*, 2014, Paper Th4C.2.
[24] H. Byun *et al.*, "Bulk-Si photonics technology for DRAM interface," *Photon. Res.*, vol. 2, no. 3, pp. A25–A33, 2014.
[25] D. Knoll *et al.*, "Substrate design and thermal budget tuning for integration of photonic components in a high-performance SiGe:C BiCMOS process," *ECS Trans.*, vol. 50, no. 9, pp. 297–303, 2012.
[26] J. C. Hulme, J. K. Doylend, and J. E. Bowers, "Widely tunable Vernier ring laser on hybrid silicon," *Opt. Exp.*, vol. 21, no. 17, pp. 19718–19722, 2013.
[27] D. Liang and J. E. Bowers, "Recent progress in lasers on silicon," *Nature Photon.*, vol. 4, no. 1, pp. 511–517, 2010.
[28] H. Park *et al.*, "Device and integration technology for silicon photonic transmitters," *IEEE J. Sel. Topics Quantum Electron.*, 17, vol. no. 3, pp. 671–688, May/Jun. 2011.
[29] M. J. R. Heck *et al.*, "Hybrid silicon photonic integrated circuit technology," *IEEE J. Sel. Topics Quantum Electron.*, vol. 19, no. 4, Jul./Aug. 2013, Art. no. 6100117.
[30] S. Keyvaninia *et al.*, "Heterogeneously integrated III-V/silicon distributed feedback lasers," *Opt. Lett.*, vol. 38, no. 24, pp. 5434–5437, 2014.
[31] L. A. Coldren, S. W. Corzine, and M. L. Mashanovitch, *Diode Lasers and Photonic Integrated Circuits*, 2nd ed. Hoboken, NJ, USA: Wiley, 2012.
[32] A. McConnell, S. Uma, and K. Goodson, "Thermal conductivity of doped polysilicon layers," *J. Microelectromechan. Syst.*, vol. 10, no. 3, pp. 360–369, 2001.
[33] D. Shin *et al.*, "O-band DFB laser heterogeneously integrated on bulk-silicon platform," *Opt. Exp.*, vol. 26, no. 11, pp. 14768–14774, 2018.
[34] D. Shin *et al.*, "Heterogeneously integrated light sources for bulk-silicon platform," in *Proc. IEEE Int. Electron Devices Meeting*, 2018, pp. 23.6.1–23.6.4.
[35] D. Shin *et al.*, "Optical isolator and photonic integrated circuit including the same," US 17/357503.
[36] D. Shin and K. Ha, "Building better lasers on low-cost silicon," *Compound Semicond.*, Jun. 2019.
[37] J. Cha *et al.*, "Heterogeneous integration of O-band LDs on bulk-Si platform," in *Proc. 24th Optoelectron. Commun. Conf. Int. Conf. Photon. Switching Comput.*, 2019, pp. 1–3.
[38] D. Shin *et al.*, "III/V-on-bulk-Si technology for commercially viable photonics-integrated VLSI," in *Proc. IEEE Symp. VLSI Technol.*, 2020, pp. 1–2.
[39] J. Sun *et al.*, "Large-scale nanophotonic phased array," *Nature*, vol. 493, no. 7431, pp. 195–199, 2013.
[40] J. C. Hulme *et al.*, "Fully integrated hybrid silicon two dimensional beam scanner," *Opt. Exp.*, vol. 23, no. 5, pp. 5861–5874, 2015.
[41] D. N. Hutchison *et al.*, "High-resolution aliasing-free optical beam steering," *Optica*, vol. 3, no. 8, pp. 887–890, 2016.
[42] C. V. Poulton *et al.*, "Coherent solid-state LIDAR with silicon photonic optical phased arrays," *Opt. Lett.*, vol. 42, no. 20, pp. 4091–4094, 2017.
[43] T. Komljenovic *et al.*, "Sparse aperiodic arrays for optical beam forming and LIDAR," *Opt. Exp.*, vol. 25, no. 3, pp. 2511–2528, 2017.
[44] S. Chung, H. Abediasl, and H. Hashemi, "A monolithically integrated large-scale optical phased array in Silicon-on-Insulator CMOS," *IEEE J. Solid-State Circuits*, vol. 53, no. 1, pp. 275–296, Jan. 2018.
[45] C. V. Poulton *et al.*, "8192-element optical phased array with 100° steering range and flip-chip CMOS," in *Proc. Conf. Lasers Electro-Opt., OSA Tech. Dig.*, 2020, Paper JTh4A.3.
[46] C. V. Poulton *et al.*, "Long-range LiDAR and free-space data communication with high-performance optical phased arrays," *IEEE J. Sel. Topics Quantum Electron.*, vol. 25, no. 5, Sept./Oct. 2019, Art. no. 7700108.
[47] J. K. Doylend and S. Gupta, "An overview of silicon photonics for LIDAR," *Proc. SPIE*, vol. 11285, 2020, Art. no. 112850J.
[48] C. Shin *et al.*, "A 10-m LiDAR system using an aperiodic spatially-chirped optical phased array," in *Proc. Conf. Lasers Electro-Opt., OSA Tech. Dig.*, 2021, paper STu4D.2.
[49] H. Byun *et al.*, "A gain-enhanced silicon-photonic optical phased array with integrated O-band amplifiers for 40-m ranging and 3D scan," in *Proc. Conf. Lasers Electro-Opt.*, 2020, pp. 1–2.
[50] J. Lee *et al.*, "Single-chip beam scanner with integrated light source for real-time light detection and ranging," in *Proc. IEEE Int. Electron Devices Meeting*, 2020, pp. 7.2.1–7.2.4.
[51] D. Shin *et al.*, "III/V-on-bulk-Si platform: Born for DRAM, transplanted to LiDAR," in *Proc. Eur. Conf. Opt. Commun.*, 2021, pp. 1–3.
[52] H. Byun *et al.*, "Single-chip beam scanner LiDAR module for 20-m imaging," in *Proc. IEEE Int. Electron Devices Meeting*, 2021, pp. 14732–14745.
[53] D. Shin *et al.*, "Commoditizing the uncommoditized: Chip-scale LiDAR," in *Proc. SPIE Photon. West, Opt. Interconnects XXII*, 2022, pp. 12007–12012.
[54] T. K. Sarkar and M. S. Palma, "A history of the evolution of RADAR," in *Proc. 44th Eur. Microw. Conf.*, 2014, pp. 734–737.
[55] K. Kikuchi, "History of coherent optical communication and challenges for the future," in *Proc. Dig. IEEE/LEOS Summer Topical Meetings*, 2008, pp. 107–108.
[56] DARPA, *Lasers for Universal Microscale Opt. Syst.*, [Online]. Available: https://www.darpa.mil/program/lasers-for-universal-microscale-optical-systems
[57] T. Y. Fan, "Laser beam combining for high-power, high-radiance sources," in *IEEE J. Sel. Topics Quantum Electron.*, vol. 11, no. 3, pp. 567–577, May/Jun. 2005.
[58] M. A. Tran, D. Huang, and J. E. Bowers, "Tutorial on narrow linewidth tunable semiconductor lasers using Si/III-V heterogeneous integration," *APL Photon.*, vol. 4, no. 11, 2019, Art. no. 111101.

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