Monolithically Integrated THz Photodiodes With CPW-to-WR3 E-Plane Transitions for Photodiodes Packages With WR3-Outputs

Sumer Makhlouf, Sebastian Dülme, Marcel Grzeslo, Jose Luis Fernández Estévez, Vitaly Rymanov, Jörg Lackmann, and Andreas Stöhr, *Senior Member, IEEE*

***Abstract*—An indium phosphide (InP)-based E-plane transition for monolithically integrating terahertz photodiodes with standard rectangular waveguide (WR)-outputs is presented for all standard WR-frequency bands from 0.22 THz to 2.2 THz, i.e., from WR3 to WR0.51. The integration concept comprises a modified uni-travelling carrier photodiode (MUTC-PD) chip, an E-plane transition and a stepped impedance low-pass filter (LPF), which are all monolithically integrated on an InP substrate. The E-plane transition converts the quasi-TEM coplanar waveguide (CPW) mode of the MUTC-PD output to the dominant TE_{10} mode of the WR. To our knowledge, this is the first frequency-scalable monolithic integration concept that enables packaging of photodiodes with standard WR-outputs up to 2.2 THz. The recommended thickness of the InP substrate and the proposed E-plane transitions' design parameters are investigated by numerical analysis to achieve minimum insertion loss (IL) and a wide operational bandwidth (BW). The presented optimized transitions exhibit a maximum IL of 1.4 dB, a return loss (RL) better than 10 dB and a minimum 1 dB IL BW of 92.23% for all WR-bands up to 2.2 THz. To prove the proposed monolithic integration concept, a MUTC-PD is integrated with a CPW-to-WR3 E-plane transition (220-320 GHz) on a 95 μm-thick InP substrate. At 300 GHz, the maximum achieved RF output power of the fabricated MUTC-PD chip is −12.4 dBm at a photocurrent of 18.5 mA. For experimental characterization, the MUTC-PD chip with the integrated E-plane transition has been mounted on a 1 mm-thick soda-lime glass substrate as carrier and it has been manually aligned within a WR3 together with an adjustable back-short. Due to non-perfect alignment of the chip and the back-short as well as the additional losses and substrate modes due to the thick glass carrier, the calculated average IL is increased to 5.3 dB. Experimentally, an average IL of 8.6 dB is measured within the WR3-band from 220 GHz to 320 GHz. Integration of the chip in a real package without misalignment and without the glass carrier is expected to improve the IL by ∼4.8 dB.**

***Index Terms*—E-plane transitions, integrated optoelectronics, microwave photonics, monolithic integration, photodiodes, terahertz radiation.**

I. Introduction

TERAHERTZ photodiodes (THz-PDs) modules that feature standard rectangular waveguide (WR)-outputs have been widely utilized for building up THz photonic systems for various applications such as communications [1], radio astronomy [2], spectroscopy and imaging [3]. The key advantages of THz-PDs modules over electronic-based sources, such as solid-state oscillators [4] and backward wave oscillators (BWOs) [5], are their broad operational bandwidth (BW) and the ability to generate low phase noise signals from optical combs using PDs (zeta phase noise).

Telecom wavelengths of 1.3 μm and 1.55 μm are often preferred for PDs operation because of the dispersion and loss characteristics of standard single-mode optical fibers and the availability of a vast number of additional active and passive optical components such as optical amplifiers. Operation at telecom wavelengths requires growing the THz-PDs epitaxial layer stack on indium phosphide (InP) substrates for lattice matching. Furthermore, THz-PDs are usually fabricated with planar outputs such as coplanar waveguides (CPWs) to facilitate integration, e.g., with other microwave components such as amplifiers or antennas.

To package THz-PDs chips in a WR-module, it is essential to establish good electrical connectivity, i.e., mode conversion and impedance matching, between the coplanar outputs of THz-PDs and the WRs. THz transitions are used for that purpose. Generally, THz transitions can be either hybridly or monolithically integrated with the THz-PDs.

In hybrid integration approaches, the PDs and the transitions are fabricated on different substrates before being integrated by means of an electrical interconnect technology, such as wire-bonds or flip-chip bonds. Usually, the transitions are fabricated on relatively low-dielectric laminates such as quartz [6], to achieve low electrical losses. This also allows optimizing the PD and the transition individually. However, for hybrid integration an impedance transformer is required for matching the characteristic impedances of the PD and the transition. Furthermore,

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state-of-the-art electrical interconnects typically become very lossy at operational frequencies higher than 100 GHz and often excite unwanted substrate modes [7].

The inductance of wire-bonds is about 1 nH/mm, which can not be neglected even at frequencies lower than 100 GHz [8]. To keep the inductance of the wire-bonds at minimum values within the THz domain, their length has to be minimized. However, realizing the desired length of wire-bonds can be impossible due to the fabrication tolerances at THz frequencies. For example, in [9], a split-block THz-PD module with a WR3-output (220-320 GHz) was developed using two radial E-plane transitions that were based on a 50 μm-thick quartz substrate and connected to an amplifier chip employing two wire-bonds. Due to the high inductance of the wire-bonds within the WR3-band, the packaged amplifier module suffered from additional insertion loss (IL) of 2.5 dB and comparably narrow operational BW [9].

Moreover, flip-chip bonding technique was investigated to hybridly connect two chips at THz frequencies [10]–[11]. Here, the bonding process is carried out through gold bump balls that provide electrical connectivity between bonding pads, which are placed on each substrate. However, bonding technique's main drawback at frequencies above 100 GHz is the excitement of substrate modes that arise from placing the bonding pads directly on the substrate without a shield layer [12]. To avoid the excitation of the substrate modes, either the substrate thickness has to be reduced, or a metal shield layer has to be considered. However, thinning down the substrates weaken their mechanical strength dramatically at THz frequencies, which can cause damaging the substrate during the bonding process, where the recommended substrate thickness is 50 μm at 300 GHz [13], 25 μm at 650 GHz [14] and 18 μm at 1 THz [15]. On the other hand, although using a metal shield layer prevents the excitation of the substrate modes without the need for thinning down the substrate, it significantly increases the reflection because of the associated high capacitance that occurs between the metal shield layer and the bonding pads. For example, flip-chip technique was used for bonding a monolithic microwave integrated circuit (MMIC) on the top of a polyimide substrate for operation within the WR3-band [11]. Despite thinning down the polyimide substrate to 25 μm and drilling via holes on it for suppressing the substrate modes, following currents from the bonding pads to the substrate ground plane were still existed.

On the other hand, in the monolithic integration approach, the transitions are realized either together with the PDs on the same InP-substrate [16]–[19] or on a very thin low dielectric membrane layer [20], thus eliminating the need for electrical interconnects and impedance transformers. However, realizing transitions on InP substrate is very challenging because of the comparably high dielectric constant of InP and additional fabrication limitations such as difficulty to fabricate metallized via holes or air-bridges.

Recently, first InP-based CPW-to-WR transitions for monolithic integration were proposed. In [16], a planar transition based on a double-slot antenna structure was presented for the WR3-band. However, the simulated S-parameters of the proposed transition revealed a high IL and a much narrower operational BW than for transitions on low-permittivity substrates. Furthermore, dipole antennas were investigated as potential CPW-to-WR transitions at THz frequencies, due to their low-loss structure [17]–[19]. In [17] and [18], endfire dipole antenna transitions were realized on 50 μm-thick InP substrates for operating within the WR3-band and beyond it (340-380 GHz), respectively. In addition to thinning the InP substrate, dense via holes were drilled to suppress the undesired substrate modes. Furthermore, in [18], air-bridges were employed to increase the operational BW of the transition. Although the proposed InP-based dipole transition in [19] eliminates the need for via holes or air-bridges by considering a balun structure to provide wide operational BW within the WR3-band, the realization of that transition was not possible because of the frangibility of the 50 μm-thick InP substrate.

This paper presents a frequency-scalable InP-based CPW-to-WR E-plane transition for monolithic integration with THz-PDs and developing THz-PD modules featuring WR-outputs for operation up to 2.2 THz. As a proof of concept, a monolithically integrated E-plane CPW-to-WR3 transition with a modified uni-travelling carrier photodiode (MUTC-PD) is fabricated, diced, and experimentally characterized. The developed transition and the PD are fabricated together on a 95 μm-thick InP substrate without the need for an impedance transformer, thanks to the monolithic integration. These initial results demonstrate the potential of the realized monolithic integration concept for developing hermetic and relatively simple THz-PDs packages featuring WR-outputs.

The manuscript is organized as follows, Section II discusses the packaging concept of a monolithically integrated CPW-to-WR E-plane transition with a THz-PD in a PD module featuring WR-output. Section III explains the operating principle of the CPW-to-WR E-plane transition and presents the obtained numerical values of its design parameters in addition to the numerically achieved results from 0.22 THz up to 2.2 THz. Section IV addresses the fabrication technology and the experimental measurements of the developed MUTC-PD and the monolithically integrated CPW-to-WR E-plane transition within the WR3-band.

II. Packaging Concept

Fig. 1 shows a schematic view of the monolithic integration concept of an InP-based THz-PD with a standard WR using split-block packaging technology. The packaging concept is based on integrating the PD chip and the stepped-impedance low-pass filter (LPF) with the E-plane transition on the same InP substrate, i.e., monolithically. The optically-generated RF signal is coupled from the PD chip output into the WR via a monolithically integrated CPW-to-WR E-plane transition that is inserted into the WR through an opened window in its broad-wall with the corresponding back-short. Furthermore, the stepped-impedance LPF works as an RF-choke that prevents the leakage of the RF signal into the DC circuity and passes the DC current into the

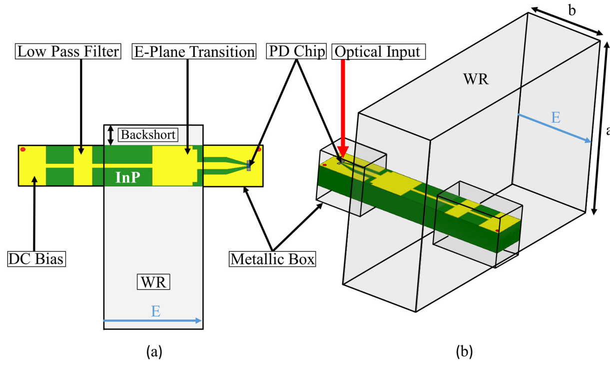

Fig. 1. Schematic of the proposed packaging concept for integrating THz-PDs with WR-waveguides: (a) top view, and (b) lateral view. In the right figure, *a* and *b* represent the height and the width of a standard WR-rectangular waveguide, respectively.

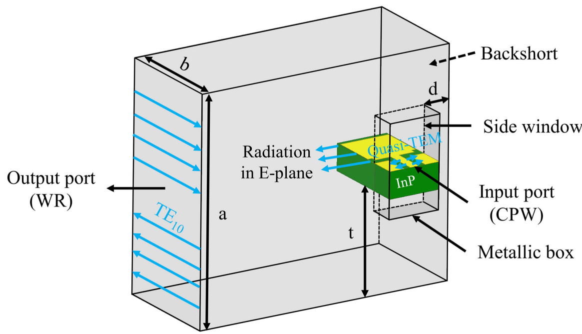

Fig. 2. Electromagnetic field distribution of the stepped CPW-to-WR E-plane transition, which is placed at height *t* and back-short depth *d* from the WR3 walls.

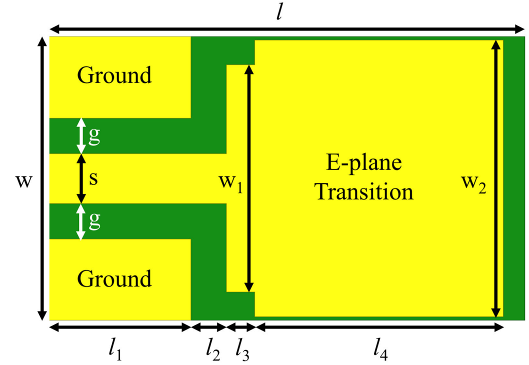

Fig. 3. Proposed CPW-to-WR E-plane transition.

TABLE I
DESIGN PARAMETERS OF THE CPW-TO-WR E-PLANE TRANSITION

Symbol	Parameter
w	InP substrate width
l	InP substrate length
g	coplanar waveguide gap
s	coplanar waveguide signal
w_1	stepped impedance microstrip line width
w_2	E-plane probe width
l_1	coplanar waveguide length
l_2	microstrip line length
l_3	stepped impedance microstrip line length
l_4	E-plane probe length
t	height from bottom WR wall
d	back-short depth

PD chip, which is required to set the optimum operating point of the PD.

III. TERAHERTZ CPW-TO-WR E-PLANE TRANSITION

To investigate the potential of exploiting the proposed E-plane transition for developing THz-PDs packages with WR-outputs at the THz domain, we first designed the transition and then numerically analyzed its electrical performance up to 2.2 THz.

A. Operating Principle

Fig. 2 illustrates the working principle of the proposed CPW-to-WR E-plane transition. The transition is inserted into the WR and aligned with the E-field propagation direction through a window that is opened in the broad-wall of the corresponding WR at height t and back-short depth d from its bottom-wall and sidewall, respectively. As previously mentioned, THz-PDs are typically grown on InP substrate and fabricated with 50 Ω CPW structures. In contrast, the WR's characteristic impedance equals the free space impedance of ∼377 Ω. Furthermore, CPW structures support the quasi-TEM mode as a dominant mode, while the dominant mode of WRs is the TE_{10} mode. Thus, for coupling the signal efficiently from the PD to the WR-output, the transition has to match the impedance of the CPW structure to the impedance of the WR, in addition, to convert the quasi-TEM mode of the CPW to the TE_{10} mode of the WR. Here, it is important to optimize the dimensions of the opened side window for preventing the reflection from the opposite WR wall toward the inserted E-plane transition. Furthermore, the back-short tunes the impedance of the E-plane transition with the frequency to achieve wide operational BW [21].

The entire structure of the proposed CPW-to-WR E-plane transition is shown in Fig. 3. Since the rationale for the proposed E-plane transition is to enable monolithic integration with THz-PDs, first a CPW structure is considered to provide straightforward integration with the CPW of the PD. The gap width g and signal width s of the CPW are calculated to achieve a characteristic impedance of ∼50 Ω. Thus, the quasi-TEM mode generated at the CPW of the PD maintains confined in the same CPW of the transition. Then, the mode keeps propagating through a very short MSL l_2 of the same width of the CPW signal width s that ends up with a stepped impedance MSL l_3 of an extended width w_1 to increase the MSL impedance gradually for matching the WR impedance. After that, the quasi-TEM mode is radiated through an E-plane antenna of length l_4 and width w_2 in the E-field direction of the WR, where the TE_{10} dominant mode of the WR is excited. The electromagnetic field distribution of the CPW-to-WR E-plane transition is shown in Fig. 2.

B. Design Parameters

The description of the design parameters of the CPW-to-WR E-plane transition is listed in Table I. The most critical design dimensions are the substrate width w, the back-short depth d,

TABLE II
DESIGN PARAMETERS OF CPW-TO-WR E-PLANE TRANSITION FROM 0.22 THZ UP TO 2.2 THZ

Waveguide Standard	Frequency Range (THz)	Substrate Thickness (μm)	50 Ω CPW G-S-G (μm)	w (μm)	l (μm)	w_1 (μm)	w_2 (μm)	l_1 (μm)	l_2 (μm)	l_3 (μm)	l_4 (μm)	d (μm)	t (μm)
WR3	0.22-0.32	95	25-33-25	200	335	160	195	100	25	20	175	100.5	382.5
WR2.2	0.32-0.5	50	7-10-7	100	250	50	65	90	30	4	110	140	254.5
WR1.5	0.5-0.75	25	5-7-5	50	175	18	25	90	15	2	60	87	178
WR1.0	0.75-1.1	15	5-6-5	30	150	13.3	28	90	15	2	34	65	119.5
WR0.65	1.1-1.7	10	5-5.2-5	18	130	6	16	90	10	2	20	52	77.5
WR0.51	1.4-2.2	5	3.4-3-3.4	12	125	7.3	11.5	90	10	2	20	50.2	62.5

the E-probe length l_4 and width w_2 that depend basically on the effective dielectric constant ε_{eff} of the substrate, i.e., the substrate thickness h and the operational frequency. These parameters have essential influence on the electrical performance and the impedance of the E-plane transition as a function of the frequency.

The substrate thickness has to be carefully selected to minimize the dispersion of non-homogeneous CPWs and microstrip lines (MSL) transmission lines. High dispersion causes a non-linear propagation constant, and that results in different group velocities as a function of the radiated frequency, i.e., group delay [22]. In this context, low dispersion values can be attained at a h/λ_{eff} below 20% [22].

Based on the previous discussion, the design parameters of the E-plane transition are optimized to achieve maximum mode conversion and impedance matching within all THz-bands of the standard THz WRs that fulfill the aspect ratio of a 1/2 height/width starting from 0.22 THz up to 2.2 THz.

C. Numerical Analysis

The S-parameters of the proposed CPW-to-WR E-plane transition are numerically analyzed starting from 0.22 THz up to 2.2 THz, i.e., from WR3 to WR0.51 waveguide standards by using ANSYS Electronics Desktop software. First, the substrate thickness h was chosen according to the operational frequency band to fulfill the previously mentioned dispersion condition. Next, the CPW dimensions, i.e., s and g were accordingly calculated to provide a characteristic impedance of 50 Ω. Next, the most crucial parameters w, d, l_4, and w_2 were optimized.

In the simulation, "driven modal solution type" was selected, and the input port (CPW) and output port (WR) were set to "wave port" excitation under the dominant mode. Furthermore, the permittivity $\varepsilon_{\text{r}} = 12.4$ and the dielectric loss tangent $\tan\delta = 0.0012$ of the InP substrates were considered. The boundary conditions were set to "radiation" for both input and output ports. The numerical values of the design parameters are listed in Table II. Here, it is noteworthy that the selected thickness of the InP substrate for operating within the WR3-band was 95 μm, rather than the recommended thickness of 50 μm in [13]. This offers better mechanical strength and thus facilitates the fabrication and dicing process.

Even the very thin substrate thickness required for THz operation could be fabricated in III/V technology using a substrate-transfer process. In this technology, two mechanical carriers are utilized. The first one is used to grind and polish the InP substrate to the required thickness. Then, the grinded and polished InP substrate is thermo-compressed over a benzocyclobutene (BCB) bonding layer onto a Rohacell 71 HF substrate that serves as a second mechanical carrier. After that, the first mechanical layer is removed. This process allows the layer thickness of the InP substrate to be reduced to a few μm, while still maintaining the mechanical robustness required for packaging. Since the dielectric constant of the Rohacell 71 HF substrate is very close to the dielectric constant of the air ($\varepsilon_r \approx \varepsilon_0 = 1$), its influence on the electrical performance of the proposed transitions is negligible [23].

Fig. 4 shows the numerically analyzed insertion loss (IL) and reflection loss (RL) of the CPW-to-WR E-probe transition up to 2.2 THz. The RL at the CPW-input port (S_{11}) is less than 10 dB, and the corresponding 3 dB BW with respect to the IL from CPW-input port to WR-output port (S_{21}) is located beyond the predefined frequency bands for all standard WRs from 0.22 THz up to 2.2 THz. Furthermore, the minimum and maximum IL are found to be less than 1 dB and 1.5 dB for the entire simulated WR-bands, respectively. Moreover, the minimum achieved 1 dB coupling BW is 34.15% of the center frequency within the WR3-band, i.e., 92.23% of the WR3-band. Whereas the maximum one is 43.9% of the center frequency within the WR2.2-band, i.e., within the entire frequency range (320-500 GHz). The numerically analyzed results of the proposed E-plane transition and the effective dielectric constant ε_{eff}, as well as the h/λ_{eff} ratios for each WR-frequency band, are summarized in Table III.

The simulated electrical performance of the CPW-to-WR E-plane transition has demonstrated low-loss electrical performance over wide operational BW within the entirety of WR-bands. Therefore, as a proof of concept, a CPW-to-WR3 E-plane transition is monolithically integrated with a THz-PD and experimentally characterized.

IV. CPW-TO-WR3 E-PLANE TRANSITION

For experimental characterization, InP-based vertical 1.55 μm modified uni-travelling carrier photodiodes (MUTC-PDs) are fabricated with and without the integrated CPW-to-WR3 E-plane transition.

A. Fabrication

A cross section of the MUTC-PD layer structure including the metallization stacks for the contacts is illustrated in Fig. 5. Furthermore, the semiconductor material, the thickness and the doping ratio of each layer of the MUTC-PD epitaxial layers are presented in Table IV. The epitaxial layers of the MUTC-PD

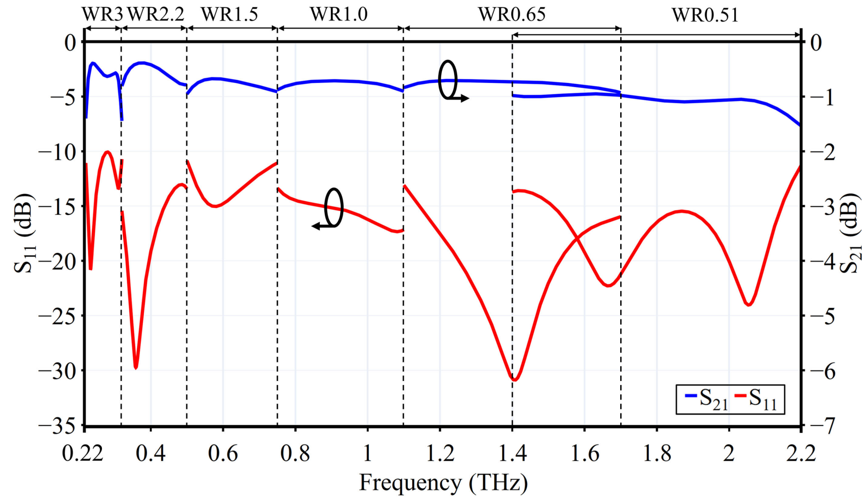

Fig. 4. Numerical analysis of the CPW-to-WR E-plane transition up to 2.2 THz (WR3-WR0.51).

TABLE III
NUMERICAL ANALYSIS OF CPW-TO-WR E-PLANE TRANSITION FROM 0.22 THZ UP TO 2.2 THZ

Waveguide Standard	Frequency Range (THz)	$\varepsilon_{\mathrm{eff}}$	h/λ_{eff}	1 dB BW	Max. Group Delay (ps)	Min. IL (dB)	Max. IL (dB)	Max. RL (dB)
WR3	0.22-0.32	6.86	22.40%	34.15%	11.5	0.39	1.44	10.0
WR2.2	0.32-0.5	6.75	17.73%	43.90%	6.3	0.38	0.80	13.0
WR1.5	0.5-0.75	6.80	13.58%	40.00%	5.9	0.67	0.95	10.8
WR1.0	0.75-1.1	6.93	12.19%	37.83%	5.4	0.74	0.93	13.0
WR0.65	1.1-1.7	7.13	12.50%	42.85%	4.0	0.70	0.92	13.0
WR0.51	1.4-2.2	7.31	8.06%	38.33%	3.6	0.94	1.40	11.8

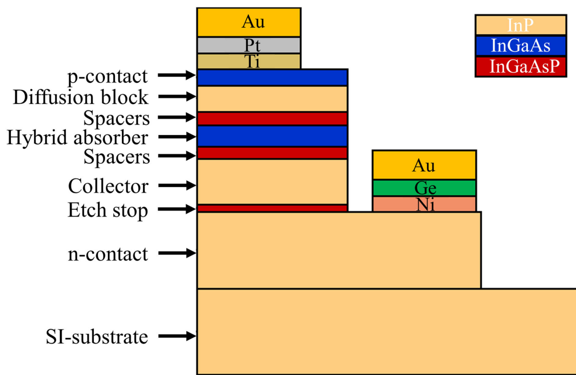

Fig. 5. Schematic cross-section of the layer structure stack of the fabricated MUTC-PD.

TABLE IV
EPITAXIAL LAYERS OF THE FABRICATED MUTC-PD

Material	Thickness (nm)	Doping (cm^{-3})	Function
InGaAs	30	Zn: $2 \cdot 10^{19}$	p-contact layer
InP	150	Zn: $2 \cdot 10^{18}$	Diffusion blocker
InGaAs	50	Zn: $2 \cdot 10^{18}$ -$2 \cdot 10^{17}$	Undepleted absorber
InGaAs	50	n.i.d	Depleted absorber
InGaAs	10	Zn: $4 \cdot 10^{17}$	p-cliff
InP	10	Si: $7 \cdot 10^{17}$	n-cliff
InP	40	Si: $1 \cdot 10^{17}$	Compensated collector 1
InP	40	Si: $5 \cdot 10^{16}$	Compensated collector 2
InP	40	n.i.d	Collector
InP	20	Si: $1 \cdot 10^{18}$	Sub-collector
InGaAsP Q1.25	30	Si: $1 \cdot 10^{18}$	Etch-stop
InP	1000	Si: $> 1 \cdot 10^{19}$	n-contact layer
InP	300	n.i.d	Buffer
InP	100000	Fe-compensated	Substrate

were grown on an iron doped semi-insulating (SI) InP substrate. The hybrid absorber of the MUTC-PDs consists of depleted and undepleted thin InGaAs layers. Non-uniformly doped and undoped InP layers were used as a collector. In addition, highly doped n- and p-cliff layers, as well as InGaAsP spacer layers, were incorporated for a precise E-field management in the carrier transport region. Furthermore, to enable low contact resistances, highly doped InGaAs and InP layers were used as p- and n-contact layers, respectively. For MUTC-PD fabrication, selective chemical wet etching was employed for the p- and n-mesa. Furthermore, Ti/Pt/Au and Ni/Ge/Au layers were deposited to achieve ohmic p- and n-contacts with low contact resistances, respectively. The CPW-pads and the E-plane transition were realized in an additional metallization step. Finally, the InP substrate was lapped down to a thickness of 95 µm and the fabricated chips were diced by means of a micro diamond wafer scriber.

For measuring the output power of the photodiodes and the IL of the E-plane transition, MUTC-PDs without and with integrated E-plane transition were fabricated as can be seen in Figs. 6 and 7, respectively.

B. Experimental Results

First, the MUTC-PDs without E-plane transition were characterized by using a 1.55 µm optical heterodyne setup with free-running external cavity lasers, which allowed to tune the

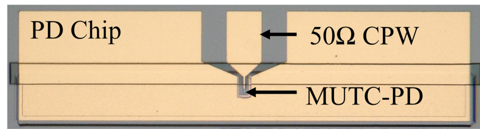

Fig. 6. Micrograph of the fabricated MUTC-PD chip with a 50 Ω CPW output.

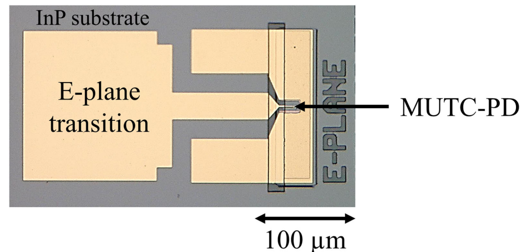

Fig. 7. Micrograph of the fabricated MUTC-PD with a monolithically integrated E-plane transition.

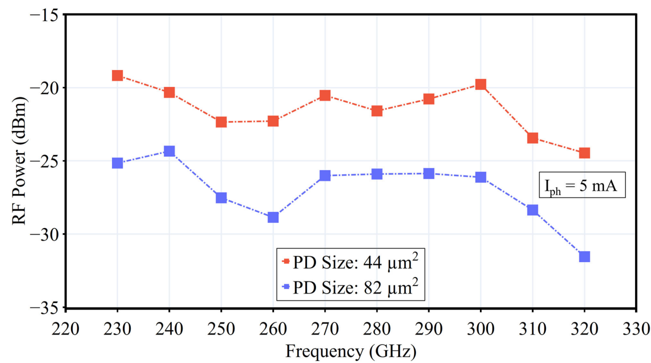

Fig. 8. Measured RF output power of fabricated MUTC-PDs for two different areas of 82 µm^2 and 44 µm^2.

beat signal over the entire WR3-band. The vertical MUTC-PDs were top illuminated using a lensed fiber. The generated output power was measured using an RF-probe with a WR3-output directly connected to a calibrated WR3-Schottky barrier diode (SBD). Fig. 8 shows the measured frequency response of the MUTC-PD chips within the WR3-band at 5 mA photocurrent for two different PD mesa diameters corresponding to an area of 44 µm² and 82 µm². The smaller MUTC-PD shows ∼5 dB higher output power, which is traced back to the improved RC-time limitation. Generally, the relative output power of the fabricated MUTC-PDs can be traced back to an increased contact resistance that emerged at the p-semiconductor, leading to additional transmission losses at higher frequencies. Moreover, the large area of the MUTC-PDs resulted in an increased capacitance and thus a more dominant RC-limitation. Since the MUTC-PDs are vertically illuminated, they exhibit a relatively low responsivity of about 0.07 A/W. However, the maximum achievable output power at 300 GHz was measured for the 44 µm² MUTC-PD. As can be seen from Fig. 9, the maximum output power is −12.4 dBm at a photocurrent of 18.5 mA. The 1dB-supression is at a photocurrent of ∼10 mA.

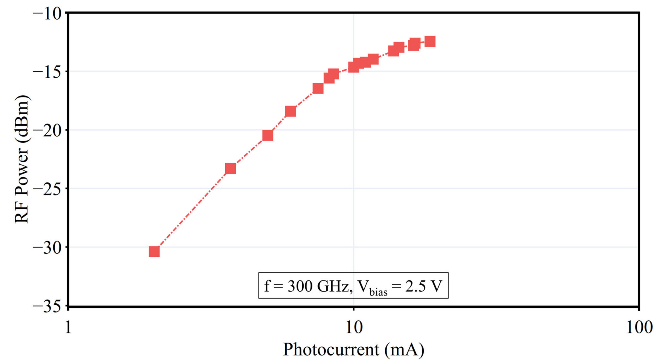

Fig. 9. High power measurement of the fabricated MUTC-PD with mesa diameter of 44 µm^2 at 300 GHz.

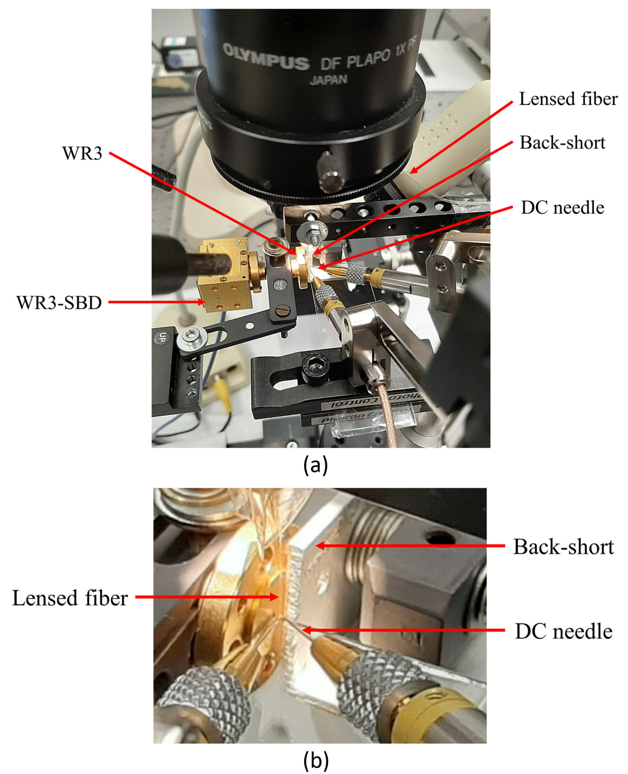

Fig. 10. (a) Photograph of the measurement setup and (b) an enlarged view of the lensed fiber, the dc needles and the back-short.

For measuring the IL of the monolithically integrated transition, the MUTC-PD with the E-plan transition was mounted on a soda-lime glass plate using wax and manually placed in front of the flange of a commercial WR3. Also, the back-short (metal plate) was manually adjusted at the other side of the chip, as demonstrated in Fig. 10. In order not to damage the chip, the distance between the chip and the flange of the WR3 could not be reduced to below 20 µm. In addition, the distance between the back-short and the chip was about 200 µm instead of 100 µm which would be optimum for this case.

For comparison, the measured RF output power and the relative frequency response of an 82 µm² MUTC-PD with and without the integrated CPW-to-WR3 E-plane transition are

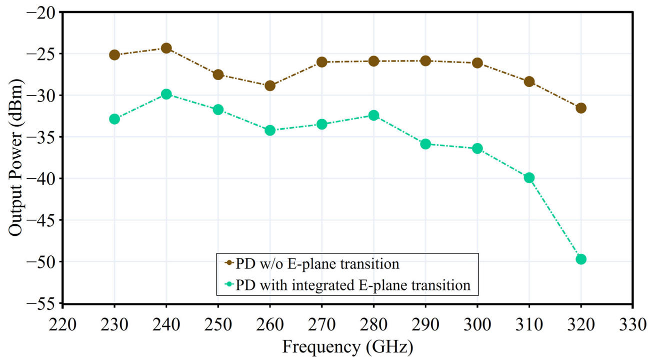

Fig. 11. Measured RF output power of the fabricated 82 μm² MUTC-PD without and with the monolithically integrated E-plane transition.

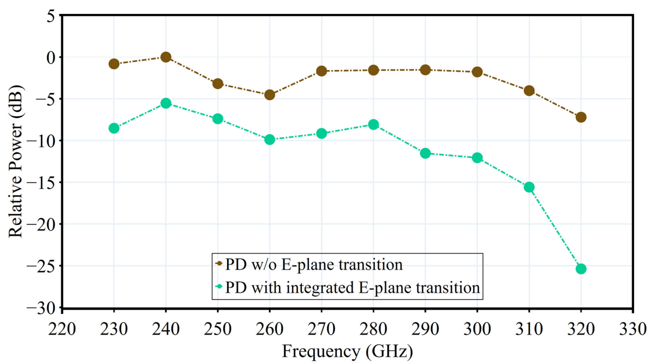

Fig. 12. Measured relative RF output power of the fabricated 82 μm² MUTC-PD without and with the monolithically integrated E-plane transition.

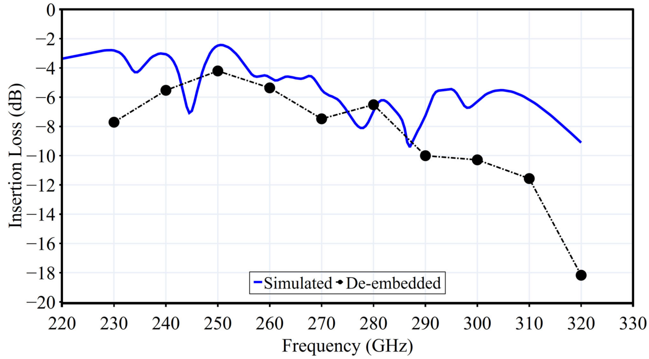

Fig. 13. Simulated and de-embedded insertion loss of the monolithically integrated E-plane transition with the 82 μm² MUTC-PD.

shown in Figs. 11 and 12, respectively. The maximum achieved output power is found to be −29.86 dBm and −24.33 dBm at a frequency of 240 GHz for an 82 μm² MUTC-PD with and without the monolithically integrated E-plane transition, respectively. Based on comparing the output power of the 82 μm² MUTC-PD with and without the monolithically integrated E-plane transition, the resulting IL of the monolithically integrated E-plane transition is de-embedded and shown in Fig. 13.

To study the impact of the non-perfectly aligned chip with the WR3-waveguide and back-short and the additional losses due to the soda-lime glass carrier, the measurement conditions were simulated using Ansys Electronics Desktop. In the simulation, the 1 mm-thick soda-lime glass plate with a dielectric constant of $\varepsilon_\mathrm{r} = 7.2$ and a dielectric loss of $\tan\delta = 0.007$ was considered [24]. Also, the exact position of the chip and the back-short with respect to the WR3 were considered. The resulted IL is also shown in Fig. 12. As can be seen, the minimum measured IL is 4.2 dB at 250 GHz and the average measured IL is 8.6 dB.

TABLE V
COMPARISON OF CPW-TO-WR3 TRANSITIONS

Freq. (GHz)	Subs.	Thick. (μm)	Coupling Approach	Realization Approach	IL (dB)	Ref.
220-325	quartz	50	E-plane	Back-to-Back	1.25	[10]
260-320	InP	50	Endfire	Back-to-Back	1	[18]
340-380	InP	50	Endfire	Back-to-Back	1	[19]
220-320	InP	95	E-plane	Monol. integ. with THz-PD	8.6	This work

Overall, there is reasonably good agreement between the simulated IL and the measured IL for the frequencies between 240 GHz and 290 GHz. However, for the frequencies towards the frequency band's edges, the losses increase, which can be traced back to increased mode conversion losses caused by the non-perfectly alignment of the chip with the WR3 and the back-short and the non-perfect lapping and dicing process.

To estimate the packaging tolerances, we carried out a parametric simulation using Ansys Desktop Electronics to reveal the individual impacts of a gap between the PD chip and the back-short as well as between the PD chip and the WR3 flange. In case of no gap between the PD chip and the WR3 flange (optimum case), this simulation revealed an increased IL of 0.1 dB per 10 μm additional gap between the PD chip and the back-short. As for the gap between the PD chip and the WR3 flange for an optimum distance to the back-short of 100 μm, the simulation shows an average increased IL of 1 dB for gaps between 2 μm to 20 μm. In our case, i.e., for a gap between PD and WR3 flange and PD and back-short of 20 μm and 200 μm, respectively, the IL is increased by 2.8 dB according to the simulations.

Although the resulted IL in this work is higher compared to previous works reported in Table V, we point out that they only reported on back-to-back measurements of transitions without photodiodes. We expect improvements by optimizing the packaging process.

V. CONCLUSION

This manuscript presented a monolithic integration concept for packaging indium phosphide (InP)-based terahertz photodiodes (THz-PDs) that feature 50 Ω coplanar waveguide (CPW) outputs with standard rectangular waveguides (WRs) from 0.22 THz to 2.2 THz. The approach is based on CPW-to-WR E-plane transitions that match the CPW impedance to the WR impedance at a given frequency band and in addition, convert the quasi-TEM mode of the CPW to the dominant TE_{10} mode of the WR.

To our knowledge, this is the first frequency-scalable monolithic integration concept for packaging THz-PDs with standard WRs. Numerically, the concept was found to exhibit a low

insertion loss (IL) below 1.4 dB, a good return loss (RL) better than 10 dB, and a 1 dB IL bandwidth wider than 93% for all WR-bands up to 2.2 THz. Besides frequency-scalability, the proposed monolithic integration approach is technologically feasible. It does not require any metallized via holes nor any electrical interconnect technology or impedance transformers.

As a proof of concept, an E-plane transition was monolithically integrated with an InP-based modified uni-travelling carrier photodiode (MUTC-PD) for operation within the WR3-band (220–320 GHz). At 300 GHz, the fabricated 44 μm^2 MUTC-PD delivered a maximum RF output power of -12.4 dBm at a photocurrent of 18.5 mA. To measure the IL of the E-plane transition, the fabricated chip was first mounted on a soda-lime glass carrier before manually aligning it together with the WR3 and the back-short. Due to a setup-related misalignment of the chip as well as the additional losses of the soda-lime glass carrier, the average simulated IL was found to be 5.3 dB which is approximately 4.8 dB higher than for the optimum case. Experimentally, the average IL was found to be 8.6 dB within the WR3-band. Therefore, for a real package, we expect an improvement of the IL by approximately 4.8 dB. Further improvements are expected from optimizing the lapping and dicing of the chips.

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