# Compact Optical TX and RX Macros for Computercom Monolithically Integrated in 45 nm CMOS

Marco Eppenberger, Mattia Bonomi, David Moor, Marco Mueller, Bertold Ian Bitachon, Thomas Burger, and Luca Alloatti

***Abstract*—As the reach of optical communications continues to shrink, photonics is moving from rack-to-rack datacom links to centimeter-scale in-computer applications (computercom) where different architectures are needed. Integrated optical microring resonators (MRRs) are emerging as an attractive choice for fulfilling the more stringent area and efficiency requirements: They offer scaling by wavelength division multiplexing (WDM) and high bandwidth densities. In this paper we present compact electro-optical transmit (TX) and receive (RX) macros for computercom monolithically integrated in 45 nm CMOS. They operate with MRR modulators and photodetectors and include all necessary electronics and optics to enable optical links between on-chip data sources and sinks. A most compact implementation for thermal stabilization was enabled by sensing the optical device's bias currents in the driving electronics instead of using external operating point sensing optics. Using a field-effect transistor as heating element — as is possible in monolithic integration platforms — further reduces area and power necessary for thermal control. The TX macro is shown to work for data rates up to 16 Gb/s with a 5.5 dB extinction ratio (ER) and 2.4 dB insertion loss (IL). The RX macro demonstrates a sensitivity of 71 $\mu A_{pp}$ at 12 Gb/s for a BER $\leq 10^{-10}$. An intra-chip link built with the macros achieves $\leq$2.35 pJ/b electrical efficiency and a BER $\leq 10^{-10}$ at 10 Gb/s. Both macros are realized within 0.0073 mm$^2$ which amounts to 1.4 Tb/s/mm$^2$ bandwidth density per macro.**

***Index Terms*—High performance computing, integrated optics, optical RX, optical TX, ring modulator, ring photodiode, thermal management of optics.**

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## I. Introduction

EFFICIENT and compact optical transceivers are key for interconnecting future high-performance computing (HPC) systems [1]. Replacing the ubiquitous copper-based interconnects by optical data transmission promises a viable path to meet the future I/O capacity, energy efficiency, and density requirements at computercom distances [2]–[4]. Exploiting tight co-integration of optics and electronics together with computing data sources and sinks allows to realize circuits with lowest power consumption and highest bandwidth densities [5], [6]. This means that computercom optics and the required driving and receiving electronics ideally are integrated in a common module. Recent research has therefore focused on co-integrating silicon photonic devices with electronic components [7]. Various groups have shown either 2D/2.5D integration [8]–[11], 3D integration [12]–[20] or monolithic integration [21]–[27] to be possible.

The bandwidth density (the bandwidth available per silicon area used in units of Tb/s/mm$^2$) can serve as a metric for the "level of integration". This metric is relevant for e.g., HPC systems where high bandwidth densities lower the total cost per transmitted bit [28]. Wavelength-division-multiplexing (WDM) systems built with microring resonators (MRR) have emerged as a promising way for reaching high bandwidth densities and energy efficiencies [29]. Note that the calculation of bandwidth densities of such systems should include not only drivers and receiving amplifiers, but also serializer (SER) and deserializers (DES) which are necessary to translate between line rate ($\geq$10 Gb/s) and the clock rate of computing resources (max. $\sim$5 GHz), but also all other necessary components like thermal stabilization circuits for MRRs or some form of clock phase correction. Subsequently, we estimate the total silicon area used to implement active optics, SER, DES, receiving amplifiers, transmit drivers, and thermal controller for some representative publications from given data, figures and die shots. Structures that are not strictly necessary for computercom (e.g., phase-locked loops and clock and data recovery circuits) have not been included.

Different solutions relying on MRRs with co-integrated systems (so-called 3D integration schemes) have already been shown. So for instance, transmit drivers and receiving amplifier electronics have been flip-chip bonded to silicon photonic integrated circuits (IC) in [14], [15]. These solutions achieve

$\geq$1 Tb/s/mm$^2$, however without including SER and DES. Also, a PAM4 transmitter for maximum single-carrier data-rate transmission has been shown. This requires pre-distortion for MRR modulators. This way a bandwidth density of 0.4 Tb/s/mm$^2$ has been achieved for the transmitter [17].

Among the monolithic integration platforms, the "zero-change" CMOS method naturally enables high densities by bringing photonics into the electronic CMOS nodes and hence closest to data sources and sinks. A first chip-to-chip demonstration was shown in [21] at 2.5 Gb/s with broadband photodiodes and thermally stabilized MRR modulators. The technology has been further refined in the following years: The first ring-to-ring operation was shown in a four-lambda WDM demonstration at 8 Gb/s/lambda scaling to 0.1 Tb/s/mm$^2$ but for datacom applications with less stringent density requirements [23]. Two implementations have already demonstrated 40 Gb/s transmitters and have shown the potential for compactness: PAM4 signaling via an optical DAC was shown to scale to 1.0 Tb/s/mm$^2$ [30], and NRZ to 3.0 Tb/s/mm$^2$ [31]. A highly sensitive (9 $\mu A_{pp}$ at $10^{-12}$ BER) single-lambda receiver was subsequently fit into 1.0 Tb/s/mm$^2$ [32].

If a system should be suitable for computercom, it must be simultaneously completely transparent to the electronics, easy to use, low power, with high bandwidth density and operate within one globally synchronous zone [2]. So, it must include all the necessary electronics for digital-to-digital communication (including SER, DES, thermal controllers, clock phase correction). However, the challenge of how to integrate full end-to-end optical transmission systems compactly with all electronics remains to this day.

In this paper, we propose transmit (TX) and receive (RX) WDM-capable macros realized in the 45 nm "zero-change" CMOS node for computercom applications. They offer end-to-end data transmission, including all necessary optics and electronics, within just a 0.015 mm$^2$ area. For minimum area usage, we employ a novel analog thermal control loop which does not need external sensing optics, and a field-effect transistor for heating (heater FET.) The macros operate on externally supplied synchronous clocks and are self-contained, i.e., can be freely placed anywhere on the chip without extra logic or area and as long as they are attached to an optical waveguide. We show the TX macro's operation up to 16 Gb/s and the RX macro's up to 12 Gb/s. An end-to-end link operating both for intra-chip transmission at 10 Gb/s is demonstrated with a total electrical efficiency of 2.35 pJ/b and total area of 0.015 mm$^2$ resulting in a per-macro density of 1.4 Tb/s/mm$^2$ (0.7 Tb/s/mm$^2$ for TX and RX combined.)

In [33], we reported on the 10 Gb/s intra-chip link realized with the macros. In this paper, we elaborate on the macro architecture with more details (concentrating on the thermal stabilization method and circuit) and additionally discuss individual macro characterization measurements.

## II. Macro Concept and Design

In this section, we describe the hardware architecture of the transmit and receive macros. All given quantities are design values, unless stated otherwise.

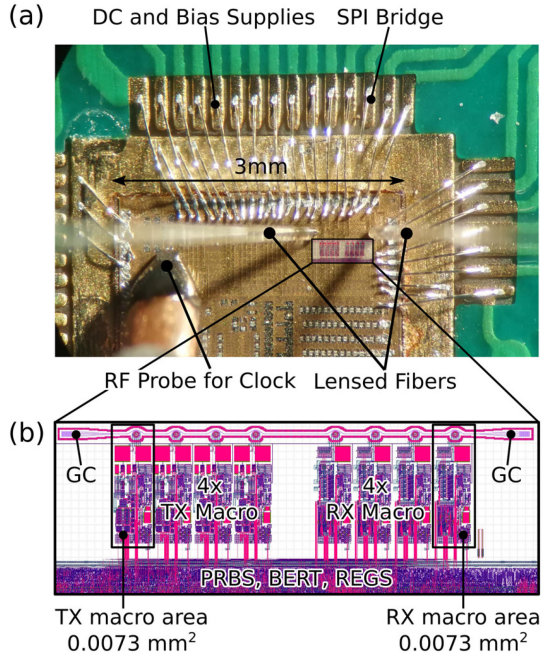


Fig. 1. (a) Microscope photograph of the "zero-change" CMOS 45 nm electronic-photonic system with the proposed macros embedded. The chip is fixed in the laboratory test mount. (b) Layout shot of a 4-lambda WDM macro realized with the proposed TX (left) and RX (right) macros. The macros optically connect on a common bus-waveguide (top) and electrically to digital logic for link quality evaluation (bottom). To realize a full link only 0.015 mm$^2$ of silicon area is needed. GC is grating coupler. PRBS is pseudo random bit sequence generator, BERT is online bit error rate tester, REGS is control registers. Figure adapted from [33].

Each macro comprises all optics and electronics necessary for computercom links: the optical devices, the respective electronic frontends (drivers, amplifiers), thermal control circuit, SER and DES. To reduce costs and increase bandwidth density of each macro, the main design goal of all included parts was to minimize footprint.

Fig. 1(a) shows a micrograph of the realized on-chip WDM transmission and reception blocks in 45 nm "zero-change" CMOS technology on the laboratory test mount. Fig. 1(b) shows the layout of an assembled WDM transmitter with four transmitter macros (TX macros) on the left, and a WDM receiver with four receiver macros (RX macros) on the right. The intended channel spacing ($\approx$3.5 nm) is a quarter of the free spectral range.

### A. Optical Devices

Silicon photonic MRRs as modulators (MRM) and photodiodes (MRPD) have shown to be power- and area-efficient [29]. Due to their wavelength selectivity, MRR based devices are naturally well suited in wavelength division multiplexed transmission schemes without additional filtering [34], [35]. However, MRR devices need to be tightly thermally controlled [36].

Fig. 2(a) and (b) show the layout of the MRM and MRPD. Both MRR cavities have 5 µm radius and are fabricated in the crystalline silicon (cSi) layer, utilize a whispering gallery mode, and are accessed by photonic bus waveguides. Pn-junctions in the silicon functionalize both cavities. Metal layers i) connect

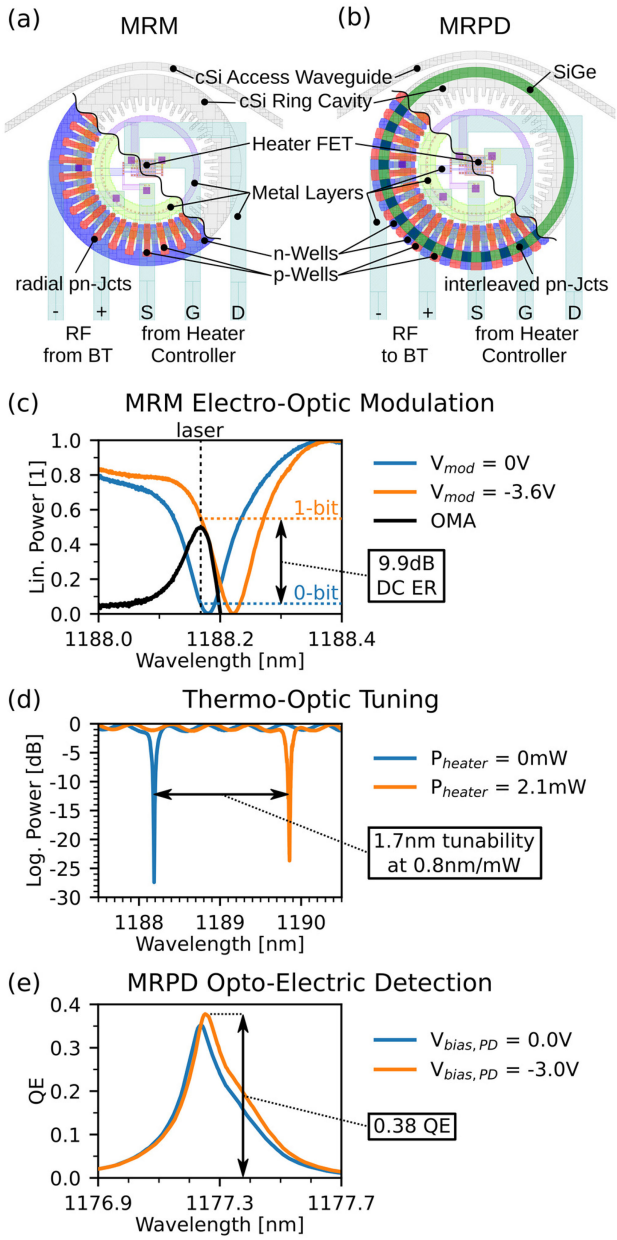


Fig. 2. (a) Layout of the MRM. Radial pn-junctions modulate the passing light with the plasma dispersion effect in doped silicon. (b) Layout of the MRPD. Interleaved pn-junctions collect the generated carriers in the SiGe pocket. In (a) and (b), the heater FET for thermal control is in the center of the microrings. (c) Measured linear transmission spectrum of the MRM showing 11.4 pm/V electro-optic tuning efficiency and 9.9 dB ER at DC. (d) Measured, log scaled transmission spectrum of the MRM showing the effect of the heater. (e) Measured QE of the MRPD with a maximum of 0.38 at 3 V reverse bias. MRM is microring modulator, MRPD is microring photodiode, FET is field effect transistor, cSi is crystalline silicon, S,G,D are labels for source, drain and gate connections of the heater FET, BT is bias-tee, OMA is optical modulation amplitude, ER is extinction ratio, QE is quantum efficiency.

the pn-junctions with the bias-tee (BT) for the RF signals, ii) connect the heater FET to its controller, and iii) serve as heat spreader around the FET. We stabilize both cavities, in closed-loop feedback, see Section IV.

A report on standalone operation of the MRM can be found in ref. [37]. The MRM achieves modulation by using the plasma-dispersion effect in radial pn-junctions in doped silicon [38]. The MRM cavity exhibits a loaded Q-factor of ∼13900, a full-width-half-max (FWHM) value of 18.2 GHz, a cavity depth of 26.5 dB, and a free spectral range (FSR) of 14.7 nm (quantities from Lorentzian fit to measurements.) Its operating principle is shown in Fig. 2(c): The cavity's resonance wavelength shifts depending on the reverse voltage applied over the radial pn-junctions hereby intensity modulating light. We measured a tuning efficiency of 11.4 pm/V at DC (9.9 dB DC ER). We measured the MRM's pn-jct capacitance to be ∼13 fF at the relevant reverse bias of −1.8 V.

The measured effect of the FET heater is shown in Fig. 2(d). By utilizing the thermo-optic effect of silicon, it allows to thermally tune the resonance wavelength over 1.7 nm at 0.8 nm/mW of heater power. In contrast to the plasma-dispersion effect, the thermal tuning is much slower (kHz) but has a much larger tuning range.

The MRPD used in this work is adapted from ref. [39]. It uses the silicon germanium alloy (SiGe) available in the node, normally used to increase the hole mobility in p-channel FETs, to enhance optical absorption inside the cavity [40]. The cavity exhibits a loaded Q ∼8200, 30.6 GHz FWHM, 18.6 dB depth, 13.9 nm FSR (quantities from Lorentzian fit to measurements.) Interleaved pn-junctions extract carriers generated by indirect bandgap absorption in the SiGe [41]. The MRPD has a maximum internal quantum efficiency (QE) of 0.38 at the relevant −3 V reverse bias, Fig. 2(e), and a bandwidth of 4.5 GHz. The available SiGe alloy composition shows reduced optical absorption above 1200 nm, hence we operate this photodiode around 1190 nm to maximize the QE [40]. This photodiode is the bandwidth limiting element of the presented system. Note that this limitation is not platform inherent, as faster but larger MRR-based photodiodes have been demonstrated in the same node [42].

The chip is optically interfaced from the back end of line (BEOL) side. Grating couplers (GC) (−4.5 dB, [43]) are used to couple light between the photonic bus waveguides and lensed fibers. The GC and the waveguides are realized in the undoped cSi layer. The losses of the waveguides have been reported in an earlier study as −3.7 dB/cm [44].

### *B. Transmit and Receive Data Paths*

Fig. 3(a) and (c) depict the layout of the TX macro and the corresponding block diagram. Its data path first includes a 20:1 SER, which provides clock-domain crossing between digital clock and RF-derived clock. The SER output is fed to a differential, double-voltage (d2vdd) driver: A pair of stacked transistors in cascode configuration output up to a 3.6 $V_{\mathrm{diff,pp}}$ signal for maximizing the optical modulation and are AC coupled to the MRM with a BT [9], c.f. Fig. 5(a).

AC coupling enables the driving-voltage-independent optimization of the bias voltage applied to the MRM. We designed the BT for a comparably high cutoff frequency at ∼85 MHz to save area of the necessary capacitors, which enables transmission of a PRBS-7 signal at 10 Gb/s. While AC coupling is an advantage in research for making the same electronics compatible with different MRM devices, DC coupling allows to reduce area even further by not needing capacitances in the BT, as e.g., in [15].

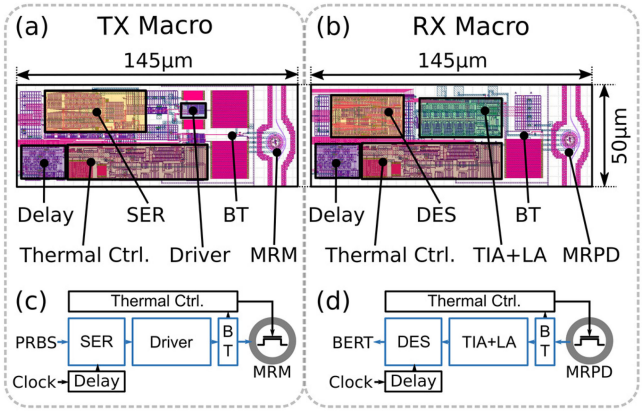


Fig. 3. (a) Layout shot of the proposed TX macro with its corresponding (c) block diagram. (b) Layout shot of the RX macro with its (d) block diagram. Both macros fit to a silicon area of 50 µm × 145 µm which equals 0.0073 mm$^2$ each. SER is serializer, BT is bias-tee, MRM is microring modulator, DES is deserializer, TIA is transimpedance amplifier, LA is limiting amplifier, MRPD is microring photodiode.

Fig. 3(b) and (d) depict the layout of the RX macro and its block diagram. In the receiving data path, we also use AC coupling with ∼85 MHz cutoff on the MRPD anode for the same reasons as above, c.f. Fig. 5(b). After the BT, a transimpedance amplifier (TIA) — small signal gain 1.73 kΩ, 3 dB bandwidth 17.1 GHz — follows. The TIA is a single-ended common-gate feedforward design analog to [45] but without peaking inductors for reaching the design goal of lowest area. For the same reason, no decision-feedback-equalization was used either, which, together with the bandwidth requirement and photodiode capacitance, resulted in the comparably low transimpedance gain. The TIA followed by five stages of differential limiting amplifiers (LA) — each with a small signal gain of 1.87 and 19.7 GHz 3 dB bandwidth — and a differential to single-ended inverter to make the voltage signal rail-to-rail. The 1-0-decision boundary can be adjusted with a 6-bit DAC in steps of 3 µA (referred to TIA input.) The DES finally deserializes and conditions the timing on its output.

Fig 3 also shows the analog thermal control loop parts (Thermal Ctrl.), see Section IV.

### C. Digital Backend

We mimic real data sources and sinks such as a processor by including a pseudo-random bit sequence generator (PRBS) feeding each TX macro and a corresponding bit-error rate tester (BERT) after each RX macro. The PRBS and BERT can evaluate the optical link quality for transmitted 7, or 31 PRBS data with optional 8b10b coding [46] applied. The BERT operates in real-time, is self-synchronizing below 12.5% BER, and includes 32-bit error counter registers. External Python software controls the on-chip APB3 bus and all configuration registers via an SPI bridge [47].

### D. Clocking

Computercom links benefit from working within globally synchronous environments: There is no need for an area and power consuming clock and data recovery circuit. In such circuits one high-speed RF clock is generated for a whole computing system and optically transmitted to each chip: A scheme which ultimately promises lowest overall power consumption for computing [2]. What remains is an absolute but constant delay in the serial link, which is influenced by process variations in the electronics and the phase of the incoming RF clock. A clock phase correction must therefore be included.

We use an off-chip global clock source and feed it with RF probes to on-chip, 50 Ω terminated distribution lines. Each RF macro taps the transmission line, using it as a double-edge (DDR) clock. A factor-10 clock division circuit taps the distribution line as well, and feeds all digital circuits, operating on positive-edge clocking. Hence, the SER/DES implements a ratio of 1:20. For the clock phase correction, we include a static time delay inside each macro. This delay line, marked Delay in Fig. 3 (c) and (d), is integrated after the RF clock tap, and is realized with multiplexed inverters [48] with a 4-bit select signal and 55 ps range (i.e., 110 ps range for the full link to cover a whole bit period at 10 Gb/s.)

## III. Zero-Change CMOS Technology and Fabrication

The electronic-photonic macros are fabricated in the GFUS 45RFSOI CMOS technology. The process allows to manufacture electronic and photonic devices in the same silicon layer hence achieving monolithic integration, Fig. 4(a). Adding photonic structures to the used CMOS node has been reported first in [44]. We use the same method as in [21] to achieve manufacturable layouts of the photonics [49]. This method has been demonstrated to work multiple times in the past [21], [23], [30]–[32], [50]–[52].

In Fig. 4(a), we illustrate the cross section of the monolithic integration of electronics and photonics in this SOI platform. It shows how passive optics (e.g., ① waveguides) and active optics (e.g., ② MRR cavities) are realized in the same crystalline Si layer as ③ electronic transistors. E-field magnitudes for 1180 nm wavelength light are overlaid on the optics showing the fundamental propagating modes: a TE-like mode in a straight waveguide and a whispering gallery mode in the MRR cavity. The distances between the depicted devices are not drawn to scale but note that the horizontal spacing between active optical devices and electronics can be as low as 10 µm.

Since this SOI technology has originally been developed for electronics, the buried oxide (BOX) layer is comparably thin (<200 nm.) Hence, we post-process the prefabricated dies to prevent light leaking into the underlying silicon substrate. First, the substrate was ground to ∼50 µm thickness by a commercial service. Second, a single UV-lithography step followed by an $XeF_2$-etch step was performed inhouse. The BOX layer served as an etch-stop. With this process, the substrate is selectively released around the optical waveguides and devices but stays intact below electronic transistors. Furthermore, it has been shown that substrate removal enhances the efficiency of thermal tuning of MRR cavities [53]. This process was carried out on a chip-scale, but selective substrate removal is generally well up-scalable to wafer-scale and commercially available [54]. Fig. 4(b) shows a microscope image of the chip's bottom side after the etching step with the optics laid open. After the substrate release, the

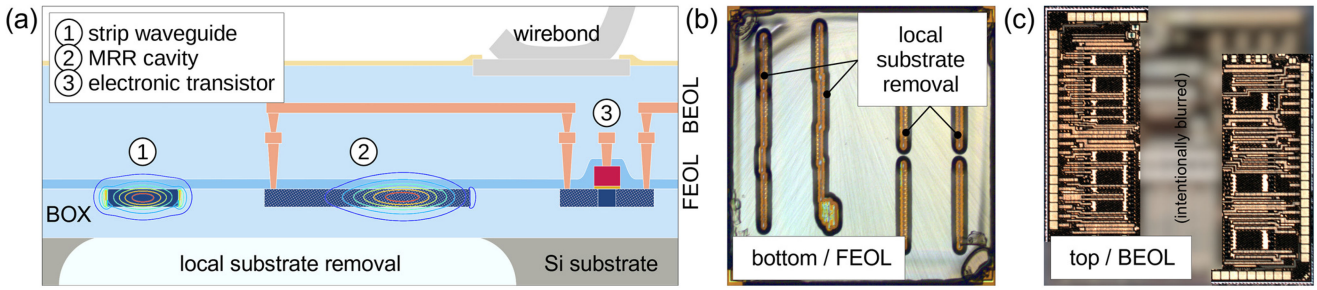


Fig. 4. (a) Illustration of cross section of the 45 nm "zero-change" SOI CMOS monolithic co-integration technology. ① Optical passive and ② active devices are realized in the same crystalline silicon layer as ③ electronic transistors. The substrate is locally removed underneath the optical devices. E-field magnitude contours at 1180 nm light are overlaid on the optical devices. Dimensions are not to scale. (b) Micrograph of bottom (substrate) side of die with visible openings where the substrate was removed locally. (c) Micrograph of top (pads) side. SOI is silicon on insulator, BOX is buried oxide, FEOL is front-end-of-line (the device layers of a CMOS process), BEOL is back-end-of-line (the metal interconnect layers of a CMOS process).

die was glued onto a carrier printed circuit board (PCB) with index-matching adhesive (NOA 81) to fill the etched holes. Wire bonds are used to connect external power and bias supplies to the chip. Fig. 4(c) shows a microscope image of the chip's top side before wire bonding.

## IV. MRR Thermal Stabilization

The resonance wavelength of the MRR cavities varies from device to device with exact the same design parameters, due to inevitable process variations in doping dosage and waveguide geometries. Furthermore, silicon MRRs exhibit a strong thermo-optic effect [36], [55]. These factors impact the performance of both the MRMs and MRPDs, by shifting the resonance wavelengths, hence influencing their operating point (OP). To operate such devices reliably in realistic applications, MRR resonance wavelengths are actively controlled using built-in resistors used as ohmic heaters [56] and a closed feedback loop [9], [57].

In this work, we propose to use a Heater FET together with an all-analog control loop locking on the bias current $I_{\mathrm{bias}}$ through the MRR's pn-junctions, Fig. 5(a) and (b). Existing solutions rely on resistive heaters which require a linear regulator [14], [17], [50], [57]. However, such linear regulators waste power as heat in their regulation transistors [58]. By replacing the resistive heater by a much more efficient FET heater controlled through its gate voltage, we leverage the availability of transistors and photonic devices in the same silicon layer and hence bypass the need for a lossy linear regulator stage. In case of using resistors as heating elements, care must be taken to linearize the control loop, e.g., with square-root compression, as e.g., done in [17]. Using a heater FET is then advantageous, since the voltage-to-power output is already linear. We use a short channel device mostly operated in velocity-saturation hence the emitted power is mostly linear with the gate voltage, Fig. 5(c). The maximum FET heater output power in our work is limited to a comparably low $\sim$2.2 mW, but this limit can be raised by using higher-power thick-oxide transistors available in the technology.

Moreover, we implement the complete control loop in the analog domain, which removes any analog-to-digital converters (ADC) or digital-to-analog converters (DAC) from the signal path and hence eliminates quantization noise and reduces chip area and power consumption. Furthermore, the proposed method does not use any additional photodiode to sense the OP but reuses the existing pn-junctions in the optical devices. Thus, the same circuit can thermally stabilize both MRM and MRPD reducing design and optimization effort.

Our closed feedback loop locks the MRR bias current $I_{\mathrm{bias}}$ to a given reference. The average of $I_{\mathrm{bias}}$ is proportional to the average laser power absorbed in the device's cavity. In the MRM, carriers are generated in defect states and via two-photon absorption (as e.g., reported in [59]), in the MRPD mainly due to the SiGe indirect bandgap absorption. The $I_{\mathrm{bias}}$ is therefore a measure on how "far into the resonance dip" a MRR device is operated, also called the device's OP. Specifically, operating an MRR far away from resonance results in little $I_{\mathrm{bias}}$, where close to resonance results in larger $I_{\mathrm{bias}}$. However, it is indiscernible from the bias current alone whether the laser power or the MRR resonance wavelength changed. For the control loop to only have $I_{\mathrm{bias}}$ as sensed variable, we must make sure that the incident optical power to the chip remains constant. Furthermore, this averaging thermal stabilization method requires DC-free data to operate [17], which is a very common requirement for optical communication channels. As we use AC coupling for attaching the optical devices, this poses no additional constraint anyhow.

The control loop implements a proportional-integral controller with analog electronics, Fig. 5(a): A trans-conductance amplifier (TCA) translates the voltage from the shunt resistor $\mathrm{R_T}$ in the BT to a current with a selectable gain (2-bit signal "prediv") covering 1.5 orders of magnitude. This is needed because bias currents in MRMs can be much lower than the average currents in MRPDs due to their different carrier generation processes. A 6-bit current digital-to-analog converter (IDAC) subtracts a reference current from the TCA output. A 5-bit variable gain TIA amplifies the resulting error current ($\mathrm{i_{err}}$) and sets the loop's gain. The following integrator stage is another amplifier with a Miller-connected capacitance (LPF). This allows to push the low-pass frequency pole to an extremely low frequency (below 2 Hz) despite the limited capacitance area available. This consideration is necessary to achieve high DC gain while maintaining stability. After the integrator an amplifier (AMP) makes the control signal rail-to-rail to fully exploit the heater range.

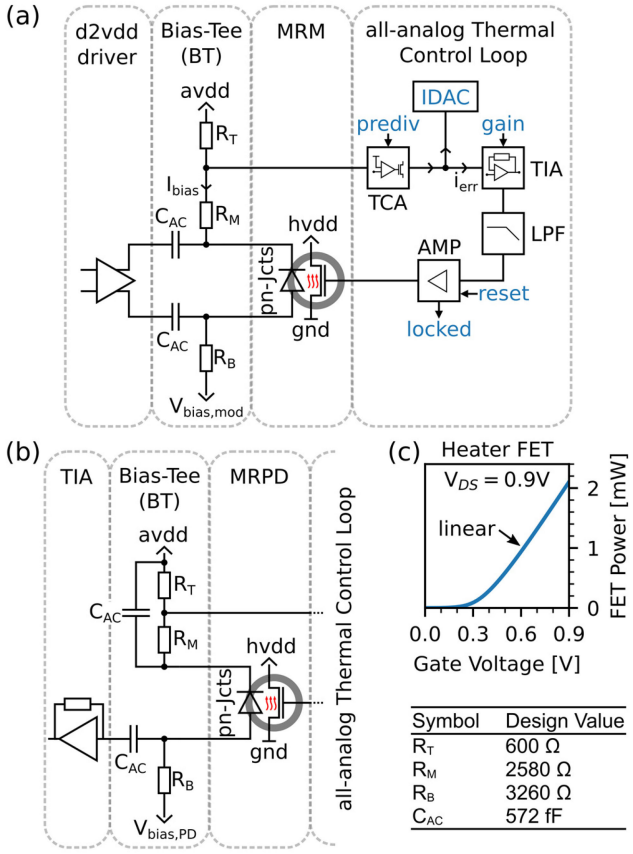


Fig. 5. (a) Driver, bias-tee, MRM, and circuit of the used analog thermal control loop. The MRM is AC coupled to the driver via a bias-tee with 85 MHz cutoff frequency. The bias current $I_{\mathrm{bias}}$ through the optical device is sensed and used to control the heater FET power via a closed-loop controller. A current DAC (IDAC) sets the operating point of the device. (b) Single-ended bias-tee structure for AC coupling the MRPD to the TIA with 85 MHz cutoff frequency. The same control loop architecture as for the MRM is used. (c) Simulated linear relationship between heater FET gate voltage and heater power output. TCA is transconductance amplifier, LPF is low-pass filter, AMP is amplifier, IDAC is current digital-to-analog converter.

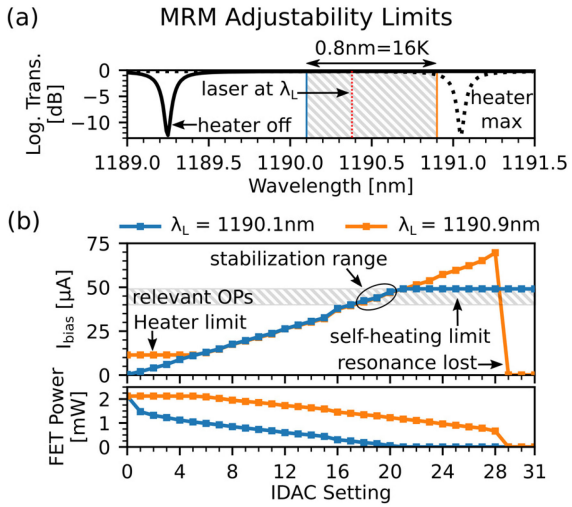


Fig. 6. (a) Illustration of the allowed laser wavelength range (shaded gray) within which an operating point (OP) can be guaranteed. This operation range is between the unheated MRM resonance (bold IL spectrum line) and the maximally heated MRM resonance (dotted IL spectrum line.) The allowed range is 0.8 nm corresponding to 16 K over which the thermal controller could stabilize the MRM. (b) Measured bias current $I_{\mathrm{bias}}$ and heater FET power in the MRM for increasing control-loop reference IDAC setpoints for the minimum (1190.1 nm) and maximum (1190.9 nm) laser wavelength $\lambda_{\mathrm{L}}$. Depending on the offset, the adjustability is either limited by the maximum heater power or by the laser self-heating. The relevant bias currents of 40 μA to 50 μA, are reached for any $\lambda_{\mathrm{L}}$ in the range specified in (a).

Based on our MRM's geometry, the control loop keeps the OP of our MRM to an accuracy of 0.01 nm or equivalently 0.2 K, while guaranteeing a range of 1.8 nm or 36 K. This ensures less than 10% eye closure for the MRM. The time it takes for the heat to propagate from the heater FET to the MRR's cavity introduces a ∼10.8 kHz pole in the loop. To guarantee stability while maintaining the accuracy requirements we designed the loop gain bandwidth product at ∼4 kHz when the DC gain is set to 66 dB. This translates to a 20% to 80% risetime of the closed-loop system of 360 μs. Hence the system can react to sub-millisecond temperature changes as e.g., necessary for co-integration next to a CPU.

In Fig. 6(a), the tunability range of the proposed thermal controller is illustrated. For the MRM to be stabilized at the relevant OPs and laser power (see Section V), the laser wavelength can be within a range of 0.8 nm (shaded gray) above the unheated resonance wavelength (1189.25 nm) but below the maximally heated resonance wavelength. This range translates to temperature influences from the environment of 16 K range which could be compensated by the proposed thermal controller. The limited tuning range, together with the constant-input-power requirement, mandates a temperature regulated laser. As proposed in [52], such a laser could operate as a high-power external "optical power source" with high efficiencies: A 33% efficiency for 200 mW single-λ optical power has been demonstrated [60].

We measured these limits as follows, Fig. 6(b): Laser light is coupled to an MRM modulating 16G NRZ data with an in-fiber power of 5.7 dBm. The laser wavelength $\lambda_L$ is kept above the unheated MRM resonance wavelength. After initializing the control loop by briefly heating the MRM to the maximum, the MRM is stabilized on the right side of the laser wavelength by the control loop such that the absorbed light results in a bias current $\mathrm{I_{bias}}$. We then continuously increase the reference IDAC starting from 0, hereby pushing the MRM resonance further into the laser, and record $\mathrm{I_{bias}}$ and the heater power. We repeat this for $\lambda_{\mathrm{L}} = 1190.1\,\mathrm{nm}$ resp. $\lambda_{\mathrm{L}} = 1190.9\,\mathrm{nm}$. For the given laser power, our MRM operates best at $\mathrm{I_{bias}}$ between 40 μA to 50 μA (shaded gray) which can be reached with any $\lambda_{\mathrm{L}}$ in the given 0.8 nm range (IDAC ≈ 19.) If $\lambda_{\mathrm{L}}$ is too large, the maximum thermal power (2.2 mW) of the heater FET upper limits the tuning range and at one point the bias current cannot be reduced any further (Heater limit). On the other hand, if $\lambda_{\mathrm{L}}$ is too small, we observe a lower bound of the tunable range because of the self-heating of the MRR (self-heating limit): There, the heater FET is off already, but the MRR is held at a heated state with non-zero $\mathrm{I_{bias}}$ due to the laser self-heating effect.

The heater range could be extended as follows: Replacing the used FET with an equally sized thick-oxide transistor can increase the Heater limit. Our simulations show a 2.7-fold increase in maximum heating power and no design-rule issues when placing a thick-oxide transistor into an MRR device.

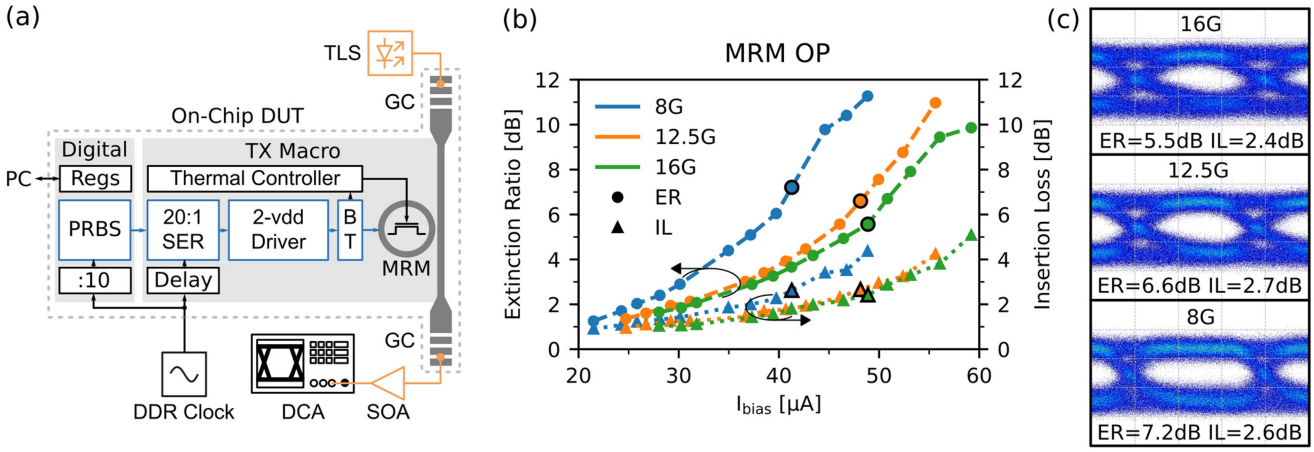


Fig. 7. TX macro characterization measurement. (a) Measurement setup. Digital logic supplies PRBS-7 data to the TX macro which modulates 1190 nm light coupled into the bus waveguide. The modulated eye is observed after coupling out of the chip and amplification. A global clock source supplies the double data rate (DDR) serial clock. (b) Extinction ratio and insertion loss curves versus stabilized average bias currents through the MRM. The thermal controller is used to stabilize the MRM at the bias current setpoint. (c) Wide-open eye diagrams are measured for serial line speeds of 8 Gb/s, 12.5 Gb/s and 16 Gb/s. The three eye-diagram operating points from (c) are marked black in (b). TLS is tunable laser source, DCA is digital communications analyzer, SOA is semiconductor optical amplifier, ER is extinction ratio, IL is insertion loss.

Using a more powerful FET does not influence the control loop performance, provided that the TIA gain inside the control loop is reduced to compensate for the increased FET gain. On the other side, less laser power reduces the self-heating limit.

Process variations for MRR resonance wavelengths are comparably low: Measured differences between two chips have a mean of 0.15 nm and std. dev. 0.95 nm (N = 7). The tuning range of 0.8 nm per MRR then results in an estimated 59% yield that two MRR's resonances can be tuned to the same laser wavelength. With the more powerful thick-oxide FET, a tuning range of up to 3.6 nm (MRR-matching yield 99.98%) could be reached, covering the intended FSR/4 WDM channel spacing.

## V. Data Modulation and Reception Experiments

In this section, we show the operation of the TX and RX macros individually and their ability to select their OPs. Then, data is transmitted and received end-to-end and intra-chip from TX macro to RX macro in a single-lambda optical link.

### A. TX Macro Characterization

We first characterize the TX Macro in a standalone fashion. Fig. 7(a) shows the measurement setup: We couple light to a test-site with a single TX macro attached on the optical access waveguide. We use a tunable laser source (TLS), by Sacher Laser, at the platform's operating wavelength of 1190.2 nm and 5.7 dBm in-fiber power before GC. We supply the DDR RF clock (DDR Clock) via an outside, low jitter clock generator (by Micram) and supply it to the chip's device under test (DUT) with 67 GHz RF probes (by FormFactor). The on-chip PRBS supplies PRBS-7 data to the TX macro. The TX macro modulates the laser light with the MRM, which is operated at -1.8 V bias and 3.4 $V_{diff,pp}$ differential peak-to-peak amplitude. The modulated light is coupled out, amplified with an 18 dB gain semiconductor optical amplifier (SOA), by Innolume, filtered with a 1-nm wide bandpass, and fed into a 52 GHz optical sampling oscilloscope (DCA), by Agilent. We modulate data at three different data rates (8 Gb/s, 12.5 Gb/s, 16 Gb/s.) The on-chip DUT is controlled via computer and SPI bridge (by Avnet).

Fig. 7(b) shows the dependence of extinction ratio (ER) and insertion loss (IL) on the biasing point and hence gives an impression on the MRM performance in different OPs. The IL is the ratio between off-resonance through optical power and 1-bit optical power. We use the thermal controller to stabilize the MRM at different bias currents $I_{bias}$ and record ER and IL. The three recorded eyes are shown in Fig. 7(c) and were taken for the OPs marked with a black border. For 16 Gb/s, we demonstrate an open eye with 5.5 dB ER at 2.4 dB IL. 12.5 Gb/s data modulation results in 6.6 dB ER and 2.7 dB IL, and 8 Gb/s in 7.2 dB ER at 2.6 dB IL.

We estimate that for the lowest, most self-heating critical eye at 8G, that the MRM experiences a 0.42 mW change in thermal load per bit. By simulation, we estimate that a 1 mW thermal load change results in 10% eye closure after ~1 ns. Thus, we estimate the maximum run length of consecutive 1 s or 0 s to 19 for a 10% eye closure of the 8G eye. As the AC-coupling mandates a PRBS-7 pattern with maximum seven consecutive 1s, the presented TX macro is not self-heating limited.

### B. RX Macro Characterization

We also characterize the RX macro standalone: Fig. 8(a) shows the measurement setup. Laser light at 1193.4 nm from the TLS is NRZ modulated with an external 15 GHz Mach Zehnder modulator (MZM), by JDSU. The modulating 8 Gb/s and 12 Gb/s signals are generated by a 20 GHz arbitrary waveform generator operating on PRBS-7 data (NRZ source), by Keysight, and amplified (RF Amp), by SHF. Due to the excess loss of the MZM at the operating wavelength, we amplify the optical signal with the SOA before feeding it to the chip. At this stage, the signal has 13 dB ER measured with the optical DCA at an average power of 7.4 dBm in-fiber before coupling, see inset

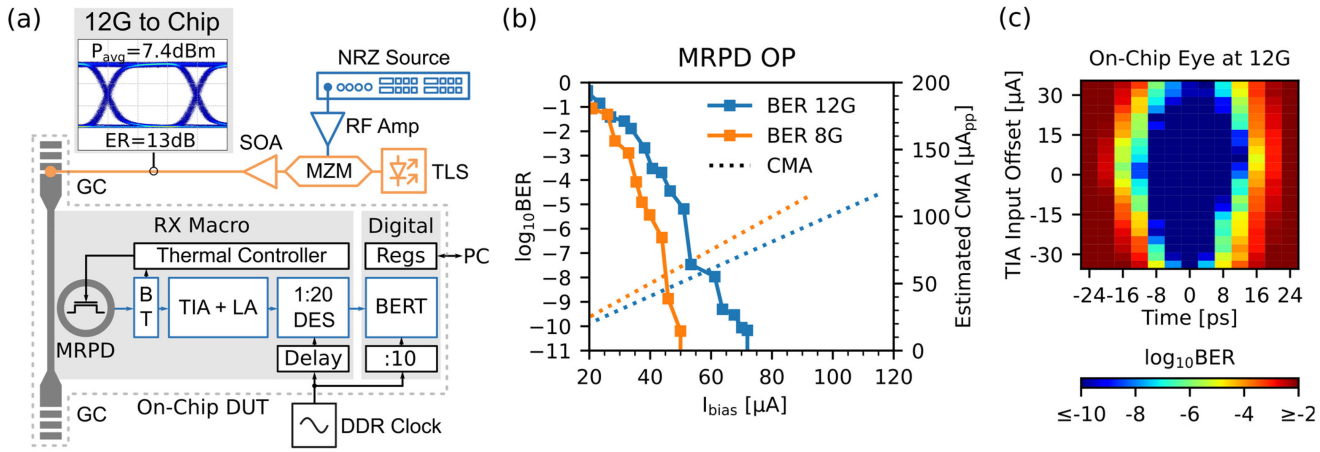


Fig. 8. RX macro characterization measurement. (a) Measurement setup. 1193 nm light is externally modulated with PRBS7 data and coupled into the chip and is received by the RX macro. The on-chip, real time BERT counts the received errors at the output of the RX macro. (b) Sensitivity analysis of the RX macro. The MRPD is stabilized at different bias currents using the thermal controller resulting in different received current modulation amplitudes (CMA) (dotted lines, right y-axis.) We estimate a sensitivity of 63 $\mu A_{pp}$ at 8 Gb/s and 71 $\mu A_{pp}$ at 12 Gb/s. (c) On-chip measured eye diagram at $I_{bias} = 86$ μA for 12 Gb/s PRBS-7 data exhibiting a 20 % UI margin at the $10^{-10}$ BER level. The y-axis is the offset current setting referred to the TIA-input. MZM is Mach-Zehnder modulator, CMA is current modulation amplitude.

in Fig. 8(a). The NRZ source is synchronized to the outside supplied DDR clock. We then receive the optical data streams with the MRPD and RX macro. The MRPD is biased at −3 V.

Fig. 8(b) shows the sensitivity plot of the receiver. We use the thermal controller to stabilize the MRPD at different OPs and record the bias currents $I_{bias}$ and the bit-error-rate (BER) with the on-chip BERT. We then estimate the current modulation amplitude (CMA) at the MRPD output by scaling the measured $I_{bias}$ by 1.8 (13 dB ER) and accounting for the S21 transfer function of the MRPD at the relevant frequencies (−3.4 dB at 4 GHz for 8 Gb/s, −5.1 dB at 6 GHz for 12 Gb/s). The CMA sensitivity (BER $\leq 10^{-10}$) hence is an estimated 63 $\mu A_{pp}$ at 8 Gb/s and 71 $\mu A_{pp}$ at 12 Gb/s. The MRPD's self-heating limit was at $I_{bias} = 93$ μA (8G) resp. 113 μA (12G) after which the bias currents could not be increased further due to the high optical powers. Fig. 8(c) shows the on-chip measured eye diagram for the 12 Gb/s case at $I_{bias} = 86$ μA. We measured the eye by varying the 1-0-decision-threshold and delay settings in the RX macro and recording the BERT output for each point. At 12 Gb/s, we measure a 20% unit-interval (UI) margin at the $10^{-10}$ BER level. Following the same analysis regarding self-heating pattern dependence as in Subsection A, we estimate a 0.39 mW thermal power change per bit at the MRPD for this eye and optical power. This limits the data pattern to 30 consecutive 1s or 0s for 10% eye closure.

### C. Intra-Chip Transmission

We demonstrate how the proposed TX and RX macros can be used for an intra-chip transmission, as e.g., in an optical network-on-chip [61]. For this, we use the experiment site shown in Fig. 1(b). This device has a slightly suboptimal design of the MRM, resulting in worse ER and IL compared to the device presented in Section A. We test only a single wavelength link from WDM transmitter to WDM receiver due to mismatches in some of the MRM and MRPD resonance wavelengths. The measurement setup is shown in Fig. 9(a). We use the TLS at 1183 nm with an in-fiber power of 5.4 dBm and couple it to the left GC of the WDM experiment. We thermally stabilize the MRM at the OP of $I_{bias} = 63$ μA and the MRPD at the OP of $I_{bias} = 109$ μA; the rest of the operating conditions are as stated above.

Fig. 9(b) shows the transmit eye. To measure this, we detune the MRPD completely out of resonance, so that all modulated light is coupled out to the off-chip eye measurement setup. We measure a transmit eye with a 6.8 dB ER at 10 Gb/s.

When tuning the MRPD to the OP, we receive the PRBS-7 data with a BER $< 10^{-10}$ with the RX macro. The same holds for PRBS-31 data if we enable the 8b10b codec which reduces the effective data rate to 8 Gb/s. The on-chip eye is shown in Fig. 9(c). The diagram shows the BER when varying the decision threshold and the time delay. At 10 Gb/s transmitted intra-chip, we measure a 16% unit-interval (UI) margin at the $10^{-10}$ BER level. Compared to the externally modulated case from Fig. 8(c), this intra-chip eye is more closed. Note that the eye opening could be significantly improved with a faster photodiode [42] and a better isolation of the power rails for the RX macro.

### D. Power and Area Efficiency

Next, we evaluate the power efficiency of the 10 Gb/s intra-chip link, the distribution thereof is shown in Fig. 10(a). All electrical power measurements have been done on an identical chip and found to be accurate to within 10% between chips. We measure a total power efficiency for the necessary electronics of 2.35 pJ/b, assuming worst-case heater FET powers are necessary, and 1.91 pJ/b for best case (no heating.) The driver (1.7 V, 0.71 pJ/b) is on a separate rail, as is the TIA + LA (0.9 V, 0.43 pJ/b), and they were measured directly. The SER (1.0 V, 0.43 pJ/b) and the DES (1.0 V, 0.34 pJ/b) use a common voltage rail with the rest of the digital circuit, they could not be measured separately. They were estimated by measuring total power on the 1.0 V rail for a varying number of switched-on or -off macros on the chip and least-squares solving the resulting system of equations for dynamic and leakage power of the individual

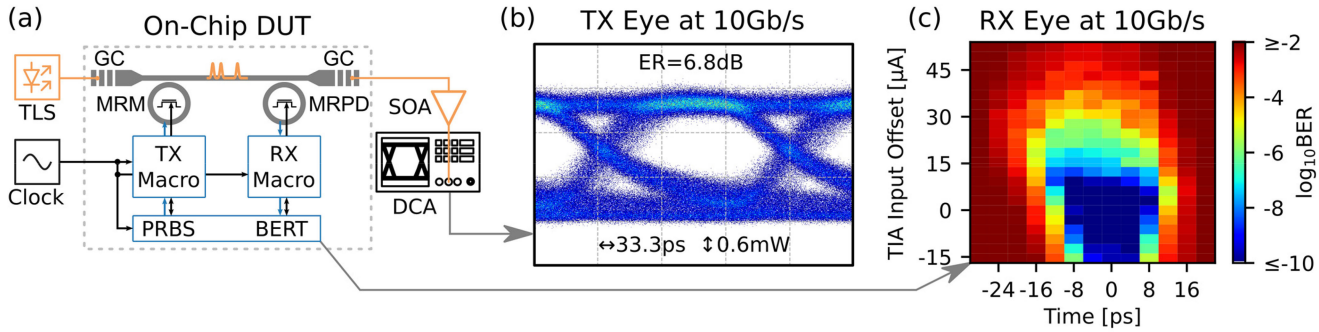


Fig. 9. Intra-chip link demonstration. (a) Measurement setup. Continuous-wave 1183 nm light is coupled into the bus waveguide, modulated with the TX macro at 10 Gb/s, then received with the RX macro. The PRBS7 data is generated with the PRBS and independently error checked with the BERT. (b) Off-chip measured eye diagram generated with the TX macro. To detect the eye the MRPD has been detuned to allow all light to pass. (c) Intra-chip transmission, on-chip measured eye diagram for 10 Gb/s. The MRM operates at 63 µA and the MRPD at 109 µA bias current. An intra-chip BER $<10^{-10}$ is achieved. DUT is device under test.

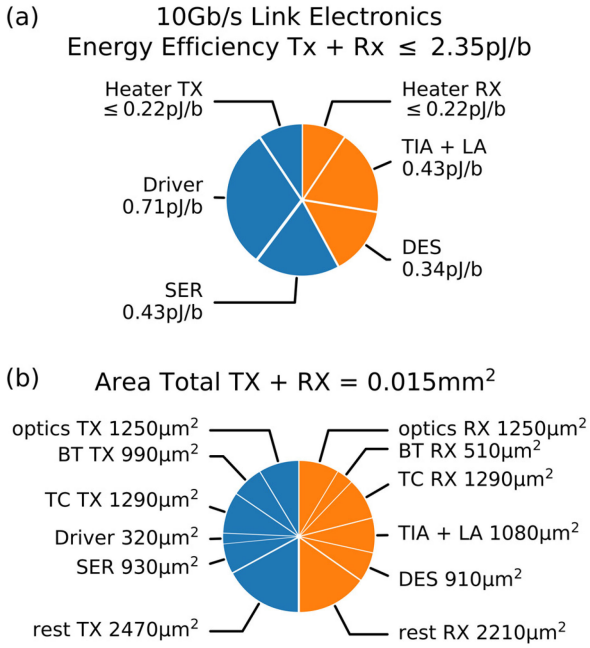


Fig. 10. (a) Power distribution for 10 Gb/s operation (a) of TX (blue) and RX (orange) macro. The heater power is assumed to be worst case, i.e., the maximum of 2.2 mW that the heater FET can output. (b) Silicon area distribution of TX (blue) and RX (orange) macro. The area for the optics is not the pure silicon area used but includes the necessary spacing between optical waveguides. TC is thermal controller.

parts. The system of equations was extended with simulation results to achieve a more accurate model. The thermal controller electronics are omitted as they use a negligible amount of power ($\leq$140 µW, resulting in $\leq$14 fJ/b.) Incorporating the optical powers one finds for the in-fiber power of 5.4 dBm an additional 0.35 pJ/b or an additional 1.1 pJ/b, assuming 33% wall plug efficiency [60]. It is important to note that we assume the serial clock as externally supplied and its energy contribution tends to zero in the limit of many used laser wavelengths. Distributing a global clock is beneficial for computercom systems: A PLL for 20 GHz could otherwise add 14.4 mW of power [31] or 1.4 pJ/b if used only for a single channel.

Fig. 10(b) shows the area distribution of the two macros. Both macros together occupy 0.015 mm$^2$ of silicon area. Notice that the bias-tee (BT) of the receiver uses less area, as only the anode of the MRPD is AC coupled. The thermal controller (TC) is the same circuit in both, TX and RX. The rest terms mainly include decoupling capacitances. As the macros are WDM ready, the GCs (80 µm $\times$ 15 µm) and bus waveguides are the only necessary passive optics. Their contribution to the bandwidth density tends to zero in the limit of many used laser wavelengths, hence they are omitted in the calculation.

The bandwidth density of each macro for the 10 Gb/s link scales to 1.4 Tb/s/mm$^2$ or 0.7 Tb/s/mm$^2$ for both macros. Operating the TX macro at the maximum of 16 Gb/s corresponds to a TX-only bandwidth density of 2.2 Tb/s/mm$^2$. Operating the RX macro at the maximum of 12 Gb/s to a RX-only bandwidth density of 1.7 Tb/s/mm$^2$. Note that these numbers are for complete and working computercom macros, as they do not need any further electronics to operate the link. They can be abutted or placed next to other electronics or passive optics without additional spacing necessary to realize WDM transmission.

## VI. Conclusion

The presented work proposes the design of compact TX and RX macros for operation in intra-chip links. We have shown the macros individual transmit (up to 16 Gb/s) and receive capabilities (up to 12 Gb/s) and their operation in a 10 Gb/s intra-chip link at a BER $< 10^{-10}$. The intra chip link consumes 2.35 pJ/b electrical energy for worst-case heating, and 1.91 pJ/b in the best case. The total silicon area for TX and RX is just 0.015 mm$^2$ which includes all necessary electronics for the data paths and thermal control. The compact implementation of the thermal controller is enabled by re-using the optical device's pn-junctions for average light detection and a heater FET to tune the optical cavities to the optimum operation point. The results show that bandwidth density of up to 1.4 Tb/s/mm$^2$ can be obtained with 10 Gb/s links. The macros were individually demonstrated at 16 Gb/s transmission (scaling to 2.2 Tb/s/mm$^2$) and at 12 Gb/s reception (scaling to 1.7 Tb/s/mm$^2$.)

A compact computercom optical data link has been presented with MRR based TX and RX macros. Due to the use of optical

cavities for modulation and detection, WDM operation can be enabled by careful resonance wavelength engineering. The proposed macros are a step towards high-density and low-power communications, immediately linking data source and sink without a need to go off-chip for integration of further optics.

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