500-Gb/s/λ Operation of Ultra-Low Power and Low-Temperature-Dependence InP-Based High-Bandwidth Coherent Driver Modulator

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Abstract—For 64-Gbaud operation and beyond, we developed a power efficient high-bandwidth coherent driver modulator composed of a linear four-channel ultra-low power CMOS driver IC and an InP-based dual-polarization IQ modulator. The CMOS driver was fabricated in 65-nm CMOS technology and showed power dissipation of <1 W owing to the use of an open-drain configuration and a stacked current-mode architecture. Moreover, by optimizing the temperature of the thermoelectric cooler that controls the modulator operating temperature, the coherent driver modulator achieved consumed power of <2.5 W at case temperatures of -5 to 75 °C and <2.8 W under -5 to 85 °C. As far as we know, this is the lowest power dissipation for a coherent driver modulator with an InP modulator chip. In addition, by employing a circuit that suppresses temperature dependence of RF characteristics in the CMOS driver, we achieved the 3-dB electro-optical bandwidth of >44 GHz and the variation of 2.0 GHz under the 25° to 85 °C condition. Furthermore, we obtained good back-to-back bit-error-rate performance in up to dual polarization 80-Gbaud 16-QAM modulation.

Index Terms—CMOS technology, Digital coherent, Driver circuits, Electrooptic modulators, Indium phosphide, Power dissipation, Quadrature amplitude modulation.

I. INTRODUCTION

DIGITAL coherent optical transmission systems [1] with higher baud-rate and higher-order optical quadrature amplitude modulation (QAM) are required to deal with the exponential growth of global IP traffic [2]. A high-bandwidth coherent driver modulator (HB-CDM) [3], [4], which supports symbol rates of up to 64 Gbaud, is an attractive device for achieving an optical transmitter for 400 Gb/s per lambda and beyond. To enhance the electro-optical (EO) bandwidth, it is necessary to not only extend the bandwidth of each component but also reduce the connection loss. From this point of view, the CDM configuration is effective in reducing the RF loss because the driver IC and modulator are co-designed and assembled next to each other in one package. Many reported InP-based modulators employ this configuration [5]–[8]. We have already confirmed a 3-dB EO bandwidth of over 67 GHz and operates up to 128 Gbaud in a driver modulator sub-assembly without an RF package, and this configuration is suitable for transmission at higher speeds [5].

Furthermore, a transmitter with a smaller footprint and lower power consumption is necessary to fabricate a small form factor pluggable transceiver such as CFP2-DCO. For example, considering the breakdown of the power dissipation of the components of a CFP2-DCO transceiver, such that of digital signal processors, a laser diode, and an optical receiver, the power budget for HB-CDM should be less than 2.5 W. Reducing the driver power and the power consumption of the thermoelectric cooler (TEC) are essential for achieving a CDM with low power consumption. Since the driver and modulator are assembled next to each other in the CDM configuration, we can use an open-collector or open-drain driver, which can reduce the footprint and the power consumption of the driver [6]. In addition, the driver power depends on an output swing voltage, and thus the half-wave voltage (V_π) of the modulator should be low to reduce the power of the driver further. An InP-based modulator can provide both high bandwidth and low drive voltage [9]–[11], and we believe an InP modulator is a suitable device for use in combination with a low-power driver. On the other hand, since an InP modulator utilizes not only the Pockels effect but also the quantum-confined Stark effect as an optical modulation mechanism [12], it needs a TEC for controlling the modulator temperature. Hence, to achieve a low-power HB-CDM, it is also important to reduce the TEC's power consumption by supressing the heat inflow to the TEC. In other words, a low-power-consumption driver is also effective in reducing the power consumed by the TEC.

In this paper, we report an ultralow power dissipation HB-CDM for 64-Gbaud operation and beyond. We developed a

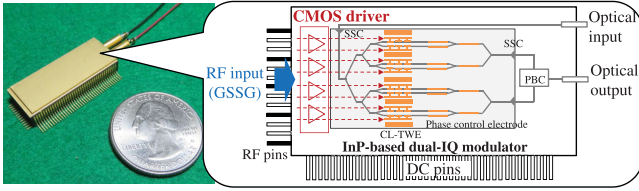Fig. 1. Image and schematic diagram of fabricated HB-CDM.

Fig. 2. (a) Image and (b) diagram of fabricated CMOS driver.

linear modulator driver for an InP modulator in 65-nm CMOS [13]. With its stacked current mode architecture [14] and an open-drain structure, our CMOS driver achieves more than a 48-GHz 3-dB electrical bandwidth and consumes less than 1 W in four-channel operation [15]. Moreover, we compensate for temperature-dependent variation of the bandwidth and gain by utilizing a power supply circuit that contains two types of resistors with different temperature gradients and a voltage regulator circuit [15]. By integrating the low-power CMOS driver and the low-V_π InP modulator in one package so that the distance between chip edges was less than 50 μm and optimizing the operating temperature of the modulator, the HB-CDM with consumes 2.5 W or less at case temperatures from −5 to 75 °C and less than 2.8 W from −5 to 85 °C. In addition, the 3-dB EO bandwidth is more than 44 GHz, which is high enough for operation at more than 64 Gbaud, and the variation of the EO bandwidth is 2.0 GHz at case temperatures from 25 to 85 °C. We demonstrated up to 80-Gbaud DP-16QAM operations capable of 500-Gb/s capacity per wavelength. As far as we know, this is the most power efficient HB-CDM for 64 Gbaud and beyond.

II. DESIGN OF HB-CDM

Fig. 1 shows an image and schematic diagram of the fabricated HB-CDM. The mechanical size is 12 × 30 × 5.5 mm³ and the DC and RF lead pins have a surface mount configuration. The HB-CDM comprises a CMOS driver IC and an InP-based modulator with a capacitively loaded traveling-wave electrode (CL-TWE) based on a differential GSSG configuration. It has three monitor photo diodes for bias control. The driver and the modulator chip are assembled in the package so that the chip edge distance is 50 μm or less to reduce the RF loss and footprint of the HB-CDM. Concretely, the wire length connecting the driver and the modulator is less than 200 μm, and double ultra-low loop wires are used to obtain the wire inductance of 100 pH or less. The modulator and the optical components such as lenses and a polarization beam combiner (PBC) are mounted on a TEC to keep the operating temperature constant. On the other hand, the driver is attached on a metal block that is outside of the TEC to suppress TEC's power consumption.

A. CMOS Driver

Fig. 2 shows an image and a block diagram of the linear driver. The four-channel driver chip is 2.0 × 3.4 mm² in size. The output voltage swing of the driver was more than 1.6-V_{ppd} for a linear operation where the total harmonic distortion (THD) at 10 GHz was up to 3%. The driver was designed so that the output swing
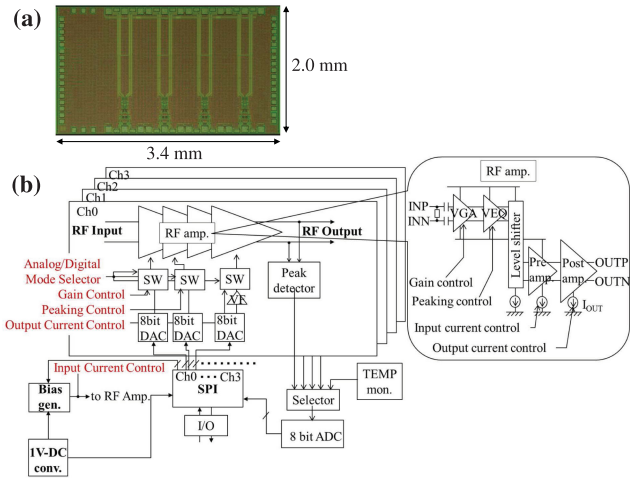
voltage become more than V_π of the modulator to achieve over 50% modulation depth for a sufficient output optical power and transmission characteristics in QAM operations. On the other hand, for a limiting operation, it is possible to obtain a 2-V_π swing voltage in QPSK operations. We used 65-nm CMOS technology to reduce power dissipation. Since the threshold voltage of a CMOS transistor is lower than that of a bipolar transistor, the CMOS transistors are effective for achieving an ultralow power driver. For the circuit architecture, we employed a stacked current mode architecture and an open-drain configuration to reduce power consumption [14]. The driver contains four amplifiers, and it should be operated with multiple supply voltages to reduce power consumption. The stacked current mode architecture generates optimal supply voltages for each amplifier stage from a single supply voltage internally without an external DC-DC converter. This stacked current-reuse architecture reduces power consumption by 30%. Furthermore, the driver uses an open-drain amplifier as a post-amplifier, which can ideally double the driver efficiency compared with an amplifier with load resistors for impedance matching [6]. While the open-drain configuration has power consumption benefits, it has no load resistors and is very sensitive to impedance mismatch. Thus, the driver and modulator should be assembled next to each other in one package to suppress signal reflections and losses. In order to minimize the degradation of RF characteristics, it is desirable to suppress the wire inductance between the driver and the modulator to 100 pH or less.

We properly designed the driver to compensate for the RF characteristics of the modulator chip, the package, and connection wires. We used the 3D inductor peaking techniques for all the stages of the amplifier to obtain a higher bandwidth with keeping a small footprint [16]. In addition, to suppress changes in the RF characteristics due to operating temperature, we utilized two types of resistors with different temperature gradients and a bias generator. The resistors contribute to compensating for a gain reduction due to the decrease in the mutual conductance of transistors at higher temperatures, and the bias generator outputs a higher voltage and increases a current at higher temperatures

to keep the gain constant. To suppress the temperature-related variation of the bandwidth, we used load resistors with a low temperature dependence. From the functional point of view, a serial peripheral interface (SPI) was integrated in the driver [15]. Via the SPI, we can control the gain and peaking level and read the peak amplitude and temperature. By controlling the current value of the internal power supply circuit via the SPI for each chip, we can suppress variations in characteristics caused by process dispersion.

B. InP Modulator

For the InP-based dual-IQ modulator chip, we employed a CL-TWE based on a differential GSSG configuration, as shown in Fig. 1 [5]. The modulator chip size has a length of 9.1 mm and a width of 3.3 mm. Generally, V_π and the EO bandwidth are in a trade-off relationship; however, the CL-TWE supports a higher EO bandwidth without a large increase in V_π. A modulator with a differential electrode is suitable for achieving an effective connection between it and the driver [17]. An InGaAlAs/InAlAs multiple quantum well (MQW) was utilized for an optical waveguide intrinsic core. Since the conduction band offset of the InGaAlAs-based MQW structure is larger than that of the InGaAsP-based MQW, a sharper band edge in an absorption spectra are obtained with the InGaAlAs-based MQW. This sharper band edge achieves higher modulation efficiency and low V_π with lower absorption loss [12], [18]. Moreover, the CL-TWE length was designed to be 3.2 mm to obtain both high bandwidth and low V_π. Thanks to this design, the modulator chip provides both an EO 3-dB bandwidth of more than 40 GHz and V_π of 1.5 V. In addition, the GSSG configuration helps in reducing crosstalk between channels. In the optical waveguide design, we integrated a vertically tapered optical spot-size converter (VT-SSC) [19] into the input and output waveguides to expand the mode field of the waveguides and reduce coupling loss between them and the optical fibers. The SSC also helps to improve lens assembly tolerance and reduce assembly cost. Furthermore, to achieve low optical propagation loss, we utilize a wide deep ridge waveguide that can propagate not only the lateral 0th mode but also the 1st and 2nd modes. The wide deep ridge waveguide is used in all waveguide sections such as modulation and passive sections. While the propagation loss can be reduced, if a higher-order mode is excited, it propagates and degrades the optical characteristics. Therefore, it is very important to prevent the excitation of higher modes. Here, the VT-SSC works as a mode filter that suppresses the excitation of the higher modes. It is also important to control the width of the multimode interference (MMI) waveguide used as an optical coupler to prevent excitation of higher modes. In particular, the waveguide fabrication process is strictly controlled so that the MMI waveguide width become the target value ± 0.05 μm. These configurations ensure good optical characteristics without adding mode filters that increases the insertion loss. From the viewpoint of power dissipation, we chose an EO phase controller to adjust the optical phase of the modulator because the other choice, a heater-type phase controller, consumes more power.
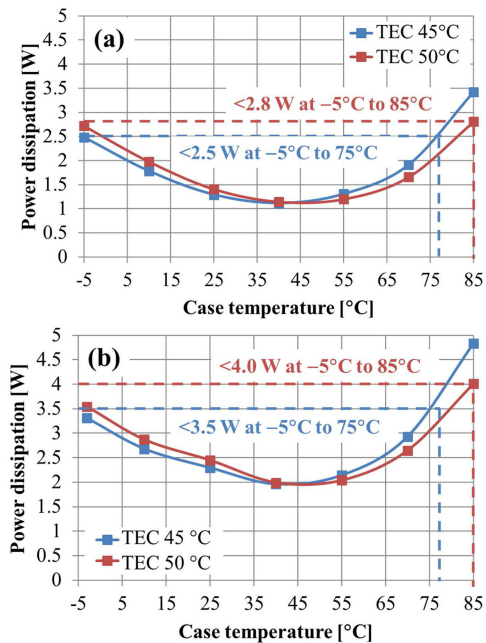

Fig. 3.   Power dissipation of the HB-CDM with (a) CMOS driver and (b) SiGe driver.

III. EXPERIMENTAL RESULTS

A. Power Consumption

Fig. 3 shows the total power consumed by the fabricated HB-CDM with (a) the CMOS driver and (b) a commercial SiGe driver when the TEC is set to 45 °C or 50 °C under the case temperature condition of −5 to 85 °C. The total power consumption of the HB-CDM includes the power of the driver IC, the TEC, termination resistors, and the modulator bias. The power of the CMOS driver is less than 1 W under the −5 °C to 85 °C case temperature condition [15], which is less than half that of the commercial SiGe driver (2 W) for 64 Gbaud. The power reduction of the driver is also effective in decreasing heat flow into the TEC and reducing the consumed power of the TEC. To the best of our knowledge, this driver has the smallest power dissipation for digital coherent transmitters with 400-Gb/s/λ or more. Regarding the total power reduction of this HB-CDM, the modulator operating temperature was set to 45 °C for the case temperature of −5 °C to 75 °C and to 50 °C for −5 °C to 85 °C to minimize the consumed power of the TEC. Thanks to the low-power driver and optimizing the operating temperature depending on the required case temperature range, we achieved ultralow power of less than 2.5 W under the −5 °C to 75 °C condition and less than 2.8 W under the −5 °C to 85 °C condition. The standardized specification of a HB-CDM is 4.5-W or less the case temperature range from −5 to 75 °C [3], and our HB-CDM is about 2.0-W lower than the specification. Moreover, the HB-CDM with the CMOS driver meets the power consumption specifications at case temperatures exceeding 85 °C. This suggests that both low power consumption and operation at higher temperature can be achieved by reducing the power dissipation of the driver. Furthermore, as can be seen from a
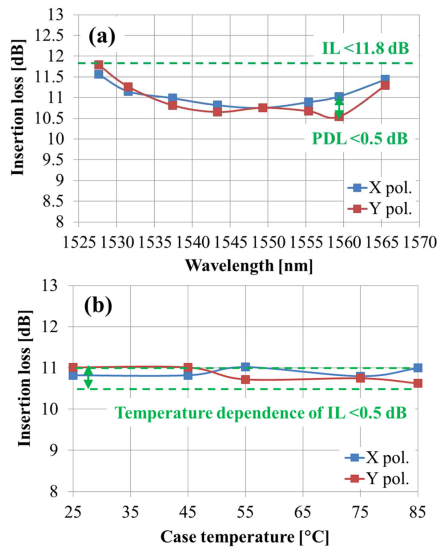
Fig. 4. Insertion loss of the HB-CDM (a) over C-band at case temperature 25 °C and (b) temperature dependence at 1550 nm.

Fig. 5. Temperature variation of small-signal EO response of the HB-CDM (a) with CMOS driver and (b) SiGe driver.

comparison between Fig. 3(a) and (b), the consumed power of the HB-CDM with the CMOS driver is 1.0 W less than that of the HB-CDM with the SiGe driver under the −5 °C to 75 °C condition and 1.2-W less under the −5 °C to 85 °C condition. In particular, at 85 °C, where the power consumption becomes severe, the power difference in the HB-CDM is larger than the difference in the driver itself. This indicates that by employing the CMOS driver, we succeeded in suppressing heat inflow to the TEC and reducing not only the power consumption of the driver but also that of the TEC.

B. Insertion Loss

Fig. 4 shows the wavelength and temperature dependence of the insertion loss (IL) of the fabricated HB-CDM with the CMOS driver when the TEC is set to 45 °C. The IL was less than 11.8 dB per polarization over the C-band at the maximum transmission, and the polarization dependent loss (PDL) was <0.5 dB. The temperature dependence of the IL at 1550 nm is less than 0.5 dB in the case temperature range of 25 to 85 °C. This is because all the optical components, such as the modulator chip, lens, and optical fibers, are mounted on a TEC and their relative position is maintained even when the case temperature changes. The IL of the modulator chip at maximum transmission condition was less than 5 dB over the C-band without optical coupling loss owing to the wide optical waveguide. The optical coupling loss between the modulator chip and input/output fibers was estimated to be about 2 dB/facet from the IL of the HB-CDM and the fiber-to-fiber measurement of the modulator chip. By controlling the higher-order modes with the wide waveguide, we achieved the extinction ratio of more than 25 dB over the C-band of the child Mach-Zehnder interferometer of the modulator.

C. Small-Signal EO Response

To measure the EO response, the HB-CDM was soldered to an evaluation board. The evaluation board has micro sub-miniature
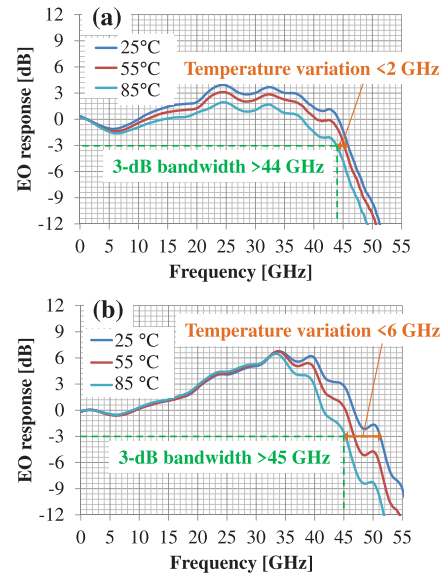
push-on (SMP) connectors for RF signal input and a military (MIL) standard connector for DC control. Fig. 5(a) and (b) show the temperature dependence of the small-signal EO response of the HB-CDM with the CMOS and SiGe driver, respectively. The measurements were performed in the 25 to 85 °C case temperature condition and the TEC was set to 45 °C. The EO response curves are normalized at 1 GHz with 3% smoothing and include the loss of the evaluation board. The EO 3-dB bandwidth of the CMOS and SiGe drivers were higher than 44 and 45 GHz, respectively. These are sufficient bandwidths for 64-Gbaud operations. It was confirmed that the HB-CDM with the CMOS driver achieved not only the low power but also good RF characteristics similar to those of the SiGe driver. Since it is difficult to compensate for the temperature dependence of the EO response adaptively with a digital signal processor (DSP), it is desirable that the temperature variation be small. In our HB-CDM with the CMOS driver, the temperature variation in the EO 3-dB bandwidth is suppressed to less than 2.0 dB as shown in Fig. 5(a). This is about half the value of the HB-CDM with the SiGe driver as shown in Fig. 5(b). This indicates that the resistors and circuit for reducing temperature variation of the driver characteristics [15] is effective.

D. IQ Modulations

Fig. 6 shows the experimental setup for IQ modulations. The signal light source was an external cavity laser (ECL) with a ∼30 kHz linewidth. The optical input wavelength and power were 1550 nm and +16 dBm, respectively. The RF signal source was a 120-GSa/s arbitrary waveform generator (AWG), and an optical modulation analyzer (OMA) with a 63-GHz bandwidth was used for signal characterization. The RF signals were input by connecting the AWG and our HB-CDM via an RF cable about 10-cm long. The added loss of this cable was about 2 dB
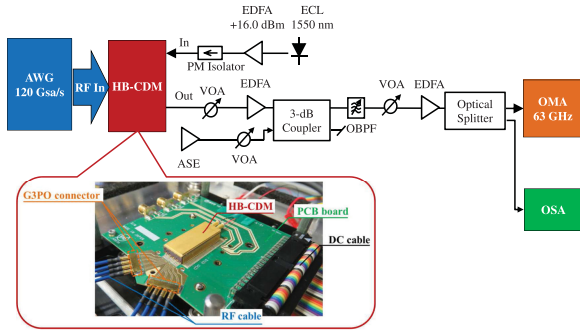
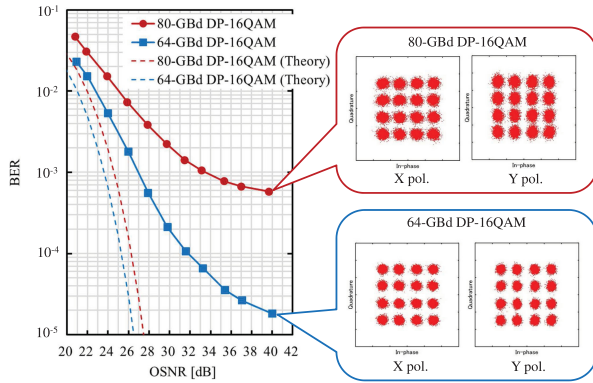Fig. 6.   Experimental setups for IQ modulations.

Fig. 7.   BER characteristics and constellation diagram of 80-Gbaud DP-16QAM and 64-Gbaud DP-16QAM.

at 40 GHz and degraded the E/O characteristics. Polarization de-multiplexing and signal equalization were conducted using a 31-tap T/2-spaced adaptive finite impulse response (FIR) filter with a butterfly configuration. An erbium-doped fiber amplifier (EDFA) and a variable optical attenuator (VOA) were implemented to adjust the optical signal power to maintain it a constant value. Noise loading was performed by using an amplified spontaneous emission (ASE) noise source followed by a VOA to control the optical signal-to-noise ratio (OSNR) for the bit error rate (BER) test. The optical output spectrum was measured by an optical spectrum analyzer (OSA) for the OSNR measurements. All measurements were performed without any FEC, pre-distortion, or pre-equalization. In this measurement, the TEC was set to 45 °C and case temperature was 25 °C.

Fig. 7 shows the BER performance and the constellations. The BER of 80-Gbaud DP-16QAM is shown by a red solid line and 64-Gbaud DP-16QAM is shown by a blue solid line. The OSNR was measured in a 0.1-nm reference noise bandwidth. The RF signals from the AWG were pulse-shaped using a root-raised-cosine (RRC) filter, and the roll-off factor and PRBS were 0.35 and 2^{15-1}, respectively. The modulator bias was set to obtain V_π of 1.5 V, and the output swing voltage of the driver was set to 0.6 V_{ppd} so that the modulation depth would be about 20% by controlling the driver gain value via the SPI. The measured BERs for the 80-Gbaud DP-16QAM and 64-Gbaud DP-16QAM were 5.79×10^{-4} and 1.82×10^{-5}, respectively, at an OSNR

of around 40 dB. The BERs are below the soft-decision forward error correction (SD-FEC) limit of 2.0×10^{-2} at OSNRs of more than 23 dB for 80-Gbaud DP-16QAM and 21 dB for 64-Gbaud 16-QAM. Moreover, the OSNR penalties determined from the theoretical curves at a BER of 2.0×10^{-2} were 2.5 dB for 80-Gbaud DP-16QAM and 1.5 dB for 64-Gbaud DP-16QAM. These results confirmed that the bandwidth of the HB-CDM with the CMOS driver is high enough for 64-Gbaud or faster baud rates of up to 80 Gbaud, which correspond to a net data rate of 500-Gb/s capacity per wavelength. Furthermore, the BER characteristics of our HB-CDM with the CMOS driver are equivalent to those of the HB-CDM with the SiGe driver [20]. We have succeeded in significantly reducing power consumption without degrading the high-speed operation characteristics.

IV. Conclusion

We have developed an ultralow-power-dissipation HB-CDM with low temperature dependence. The HB-CDM achieved low power (<2.5 W at −5 °C to 75 °C and <2.8 W at −5 °C to 85 °C), and high bandwidth (>44 GHz at 25 °C to 85 °C) with temperature variation (<2 GHz). Furthermore, we succeeded in up to 80-Gbaud 16-QAM modulations for 500-Gb/s capacity per wavelength. Our results reveal that the CMOS driver is a key device to reduce the power consumption of transmitters without degrading the high-speed operation. To our knowledge, the HB-CDM is the most power efficient HB-CDM used in digital coherent transmitters for 64-Gbaud or beyond.

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