Nonduplicate Polarization-Diversity 32 × 32 Silicon Photonics Switch Based on a SiN/Si Double-Layer Platform

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***Abstract*—We fabricate and characterize a polarization-diversity 32 × 32 silicon photonics switch by newly introducing SiN overpass waveguides onto our nonduplicate polarization-diversity path-independent insertion-loss switch. The SiN overpass waveguides are used to simplify the optical paths with a uniform path length between the edge couplers and the switch matrix and significantly reduce the number of waveguide intersections. The switch chip is fabricated using a 300-mm silicon-on-insulator wafer pilot line. The fabricated switch comprises more than 7,600 components, making this the largest ever complementary-metal-oxide-semiconductor-based silicon photonics circuit. The switch chip is electrically and optically packaged and evaluated for a sampled port connection with 32 paths, with an average on-chip loss of ∼35 dB and an average polarization-dependent loss of 3.2 dB where 75% of the measured paths exhibit a loss of less than 3 dB. The differential group delay is measured to be 1.7 ps. The performance can be further improved by optimizing the device design.**

***Index Terms*—Optical switches, photonic integrated circuits, silicon photonics, optical fiber coupling, strictly-non-blocking switches.**

I. Introduction

A STRICTLY nonblocking multiport optical switch will be a key enabler for handling a large amount of data flow in telecom and datacom applications with low electric power consumption [1]. The available technology platforms that can realize optical switches include 3D microelectronic mechanical systems [2], piezo-electric beam-steering [3], liquid crystal on silicon [4], silica planar-light wave circuits (PLCs) [5], and silicon photonics [6]. Among them, silicon photonics is a suitable technology platform owing to its highly efficient and reliable switching (with a microsecond switching time) and dense integration and suitability for mass production, which make it cost-effective. Moreover, some packaging technologies developed for electronic devices are available for large-scale silicon photonics switches with a high pin count. Previously, we reported a 32 (input ports) × 32 (output ports) path-independent insertion loss (PILOSS) silicon switch exhibiting a low fiber-to-fiber insertion loss (10.8 dB avg.) owing to advanced design and fabrication for a low on-chip loss and an extremely high-Δ silica PLC connector for a low fiber-to-chip coupling loss [6]. Our next challenge is to eliminate the polarization sensitivity of the switch. Silicon-based waveguides have an inherently tight optical confinement, resulting in a high sensitivity to geometry and hence a strong polarization dependency. There are two schemes to achieve polarization insensitivity: polarization-diversity and polarization insensitive structures. We believe the polarization-diversity scheme is a more realistic option, because it is extremely challenging to make silicon photonic components polarization insensitive given the low fabrication tolerance [7]. In a polarization-diversity scheme, two identical switch matrices are generally required to handle two orthogonally polarized components. This becomes a problem, particularly for high-radix switches, such as 32 × 32 ports, because the area and numbers of control pins and circuits required for the switch are twice those required for a single switch matrix. To avoid this problem, we proposed a novel "nonduplicate" polarization-diversity circuit based on the PILOSS topology [8]. The conventional PILOSS topology has N idle ports on the input and output sides for an $N \times N$ switch. In the nonduplicate polarization-diversity PILOSS topology, the fully and bidirectionally used idle ports have two PILOSS switches synchronously operating for the orthogonally polarized components in a single switch matrix. We previously demonstrated a nonduplicate polarization-insensitive 8 × 8 switch [8]. However, this diversity scheme has one drawback: excessive intersections on a particular path ($7N - 4$ intersections for an $N \times N$ switch) due to the embedded access waveguides in the switch matrix.

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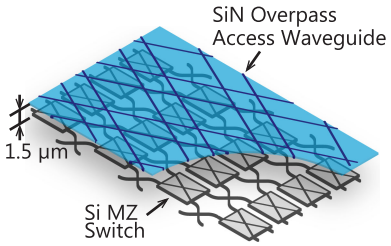

Fig. 1. Schematic of a SiN/Si double-layer platform. MZ: Mach Zehnder.

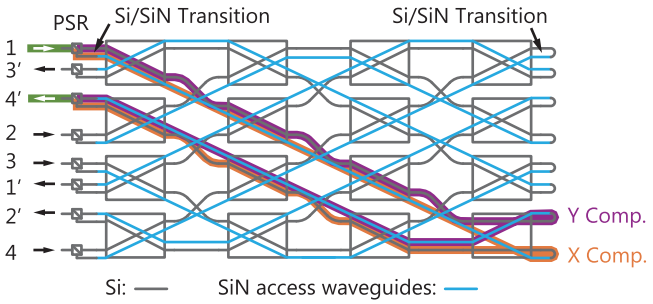

Fig. 2. Circuit diagram of the proposed polarization-diversity switch with a port count of 4 × 4. As an example, the path from input port 1 to output port 4' is highlighted. PSR: polarization splitter-rotator. X and Y component indicate the originally TE and TM modes, respectively.

In this study, we overcome this drawback and extend the port count to 32 × 32 [9]. We fabricate access waveguides in an SiN overpass layer (Fig. 1) [10], thus significantly reducing the number of intersections to $3N - 2$, and demonstrate the polarization -insensitive operation of the fabricated nonduplicate polarization -diversity 32 × 32 switch. The switch consists of more than 7,600 components, making this the largest ever complementary-metal-oxide-semiconductor (CMOS) -based silicon photonic circuit on a single chip. The switch chip is designed and fabricated, and its polarization characteristics are evaluated.

II. Switch Structure and Fabricated Device

To explain the structure and operation of the switch, a nonduplicate polarization-diversity 4 × 4 switch is depicted in Fig. 2. Each SiN overpass access waveguide connects one output port of each polarization splitter-rotator (PSR) with each corresponding right-side switch port with a fixed waveguide length. The PSR is based on adiabatic modal conversion and directional coupling [11]. The input transverse electric (TE)-like mode goes through the PSR without any changes. On the other hand, the input transverse magnetic (TM)-like mode is converted to a first higher-order TE mode with a tapered waveguide and is then coupled to the fundamental TE mode by directional coupling with an effective-index-matched waveguide. The PSR on the input port and the one on the output port are placed such that the input polarization is rotated by 90° (i.e., the TE (TM)-polarized input light is converted to a TM (TE)-polarized output light) to compensate for the polarization dependence of the edge couplers. A SiN/Si transfer coupler can exploit vertical directional coupling, which is described in Section III(A).

As an example, the path from port 1 to port 4' is highlighted in Fig. 2. The input light to port 1 is separated into X and Y components using the PSR, both of which are polarized to TE mode. The originally TE mode (X component) is first transferred to the SiN overpass waveguide by the SiN/Si transfer coupler, propagates through the waveguide, and reaches the SiN/Si transfer coupler on the right side of the switch matrix. X component is then transferred from the SiN layer to the Si layer and propagates through the Si switch matrix. On the other hand, the originally TM mode (Y component) first propagates through the Si switch matrix and reaches the SiN/Si transfer coupler. After getting transferred to the SiN layer, Y component propagates through the SiN overpass waveguide. X and Y component combine with another PSR on the output port 4', in which X (Y) component is converted into a TM (TE) mode.

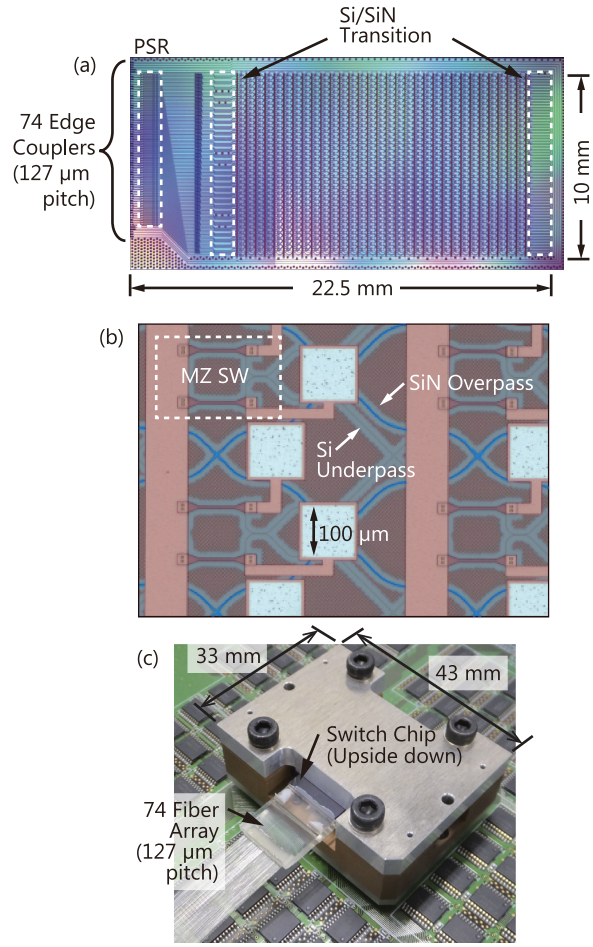

Fig. 3. (a) Microscopic image of the fabricated switch chip. (b) Magnified image of the switch chip. The blue lines indicate the SiN access waveguides. (c) Switch chip inserted into a land-grid-array socket placed on a printed circuit board with control electronics.

We fabricated the switch chip on a 300-mm silicon-on-insulator (SOI) wafer using our CMOS pilot line equipped with an immersion ArF scanner. The SiN overpass layer was deposited by plasma-enhanced chemical vapor deposition. Figs. 3(a) and (b) show the fabricated chip. The switch matrix footprint is 22.5 mm × 10 mm. The switch chip was flip-chip bonded to a ceramic interposer, which converts 0.18-mm pitch electrodes to a 0.5-mm pitch land grid array (LGA). A 74-port, 127-μm pitch, high-Δ optical fiber array was aligned with the inversely tapered edge couplers and fixed to the chip using a

refractive-index matched UV-cured glue. The assembled switch is inserted into an LGA socket placed on a control circuit board, as shown in Fig. 3(c). In this switch, it was difficult to clearly distinguish the two orthogonally polarized components inside the as-fabricated switch matrix and to set input polarizations for the TE and TM modes, thus preventing the automated element switch calibration from properly working. Therefore, we first aligned the input polarization to TM mode by monitoring the scattered light from the PSR with an IR camera, then manually calibrated the element switches. If the output ports of the PSR had in-line or tapped photodetectors, the input polarization could be set more properly, and we could better calibrate the element switches. Integration of photodetector is an ongoing effort.

The coupling loss between the high-Δ fibers and the edge couplers on the chip was estimated to be $\sim$10 dB/facet. As the inversely tapered edge couplers have polarization dependence, the edge couplers were designed such that the mode mismatch with the fiber mode is largely the same for the TE and TM modes (i.e., not the minimum for each mode). This made the coupling loss to be higher than that of single-polarization devices. Therefore, a polarization-independent edge coupler, such as a subwavelength structured edge coupler [12], was required to reduce the fiber-to-chip coupling loss in the on-chip polarization-diversity scheme. Moreover, there were other factors causing some additional coupling loss, including a large variation in the high-Δ fiber positions in the large port count fiber array and the surface roughness of the diced facet.

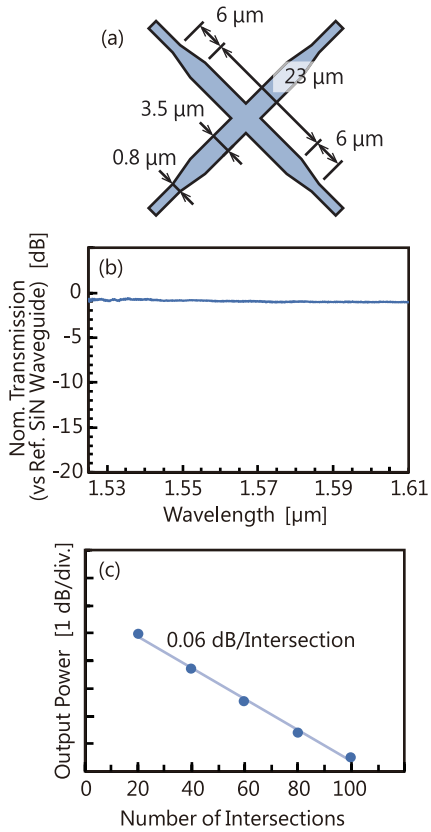

Fig. 4. (a) Schematic of SiN intersection. (b) Measured transmission spectrum. The vertical axis represents the transmission normalized with respect to output power of a reference SiN waveguide fabricated on the same chip. (c) Insertion loss of the test device at a wavelength of 1.55 μm.

III. Experimental Results and Discussion

A. SiN Devices

We prepared some test devices to evaluate the transmission characteristics of the SiN intersection and the SiN/Si transfer coupler. The propagation loss of the SiN waveguide (width: 0.8 μm, height: 0.4 μm) at a wavelength of 1.55 μm was 4.3 dB/cm. The propagation loss is mainly due to the absorption peak at a wavelength of approximately 1.52 μm; this peak is attributed to the vibrational modes of N-H bonding. Shifting the operating wavelength from the C band to the O or L bands is a realistic solution to significantly reduce the propagation loss.

Fig. 4(a) shows the structure of the SiN intersection. The intersection has a 3.5-μm-wide and 23-μm-long multimode interference structure, which is connected to the SiN waveguide with a 6-μm-long taper. Fig. 4(b) shows the measured transmission spectrum of the intersection. The intersection exhibits a very flat response over the C and L bands. The insertion loss of the intersection is 0.06 dB, as shown in Fig. 4(c). The loss can be reduced by employing an adiabatic structure [13].

Figs. 5(a) and (b) show the structure of the SiN/Si transfer coupler, which works as a vertical directional coupler. The SiN waveguide is slightly tapered to ensure the robustness of the coupling efficiency against waveguide width fluctuations. Fig. 5(c) shows the wavelength dependency of the transfer coupler, confirming that the 3-dB bandwidth covers the C and L bands. Fig. 5(d) shows the insertion loss of the transfer coupler at a wavelength of 1.55 μm. We found that a single transfer (i.e., Si $\rightarrow$ SiN $\rightarrow$ Si) causes a loss of 1.6 dB. We can reduce the transfer loss by providing feedback to the SiN width from the resulted structural dimensions in this fabrication, i.e., the SiN width in design is modified to compensate the difference from the resulted structural dimensions. Therefore, we believe that the SiN/Si double-layer platform is enough to realize a well-isolated two optical layers with low transfer loss [14].

B. Insertion Loss and Polarization Dependent Loss (PDL)

We evaluated the fiber-to-fiber insertion loss and the polarization dependent loss (PDL) of 32 sampled paths (1 (input)-1' (output), 2–2', 3–3', …, 32–32'). These port settings were selected to avoid some interference between the scattered input light and the light propagating through the switch matrix. In fact, we observed nonnegligible output power fluctuations in the path having adjacent input and output ports. As the high fiber-to-chip coupling loss (10 dB/facet) is the cause of this interference, a better optical coupling method should allow all input and output connections.

Fig. 6 shows the experimental setup. A linearly polarized light from a tunable laser diode is sent to the switch chip after polarization alignment with a polarization controller. The input light propagates through the switch in the manner described in Section II. While adjusting the input polarization using the polarization controller, we measured the maximum and minimum output powers and determined the PDL from their difference.

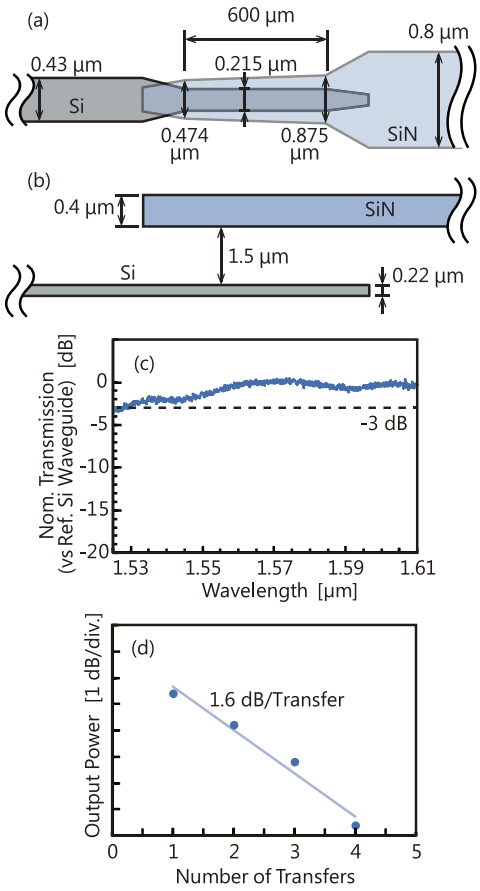

Fig. 5. (a) Top view and (b) side view of SiN/Si transfer coupler. (c) Measured transmission spectrum after single transfer (i.e., Si → SiN → Si). The vertical axis represents the transmission normalized with respect to output power of a reference Si waveguide on the identical chip. (d) Insertion loss of the test device at a wavelength of 1.55 μm.

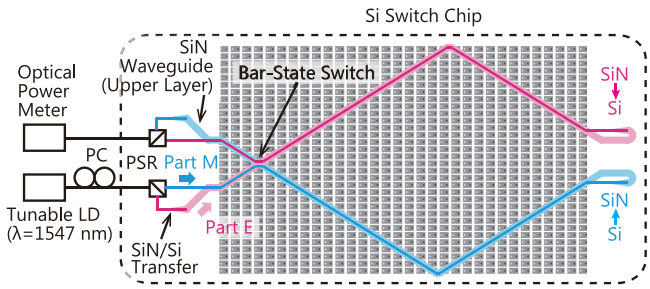

Fig. 6. Experimental setup for fiber-to-fiber insertion loss and polarization-dependent-loss measurements. PC: polarization controller. PSR: polarization splitter-rotator. Part E: originally TE mode. Part M: originally TM mode, which is converted to a TE mode on the chip.

Fig. 7 shows the measured fiber-to-fiber insertion loss of the sampled paths. The average and minimum on-chip losses are 35 and 27 dB, respectively. Table I summarizes the breakdown of the minimum insertion loss. A significant part of the insertion loss is due to the SiN overpass circuits; this loss, which, as discussed in subsection A, can be reduced by tuning the device design to the O or L bands. There is also some room to reduce the losses due to the SiN/Si transfer couplers and PSRs. Moreover,

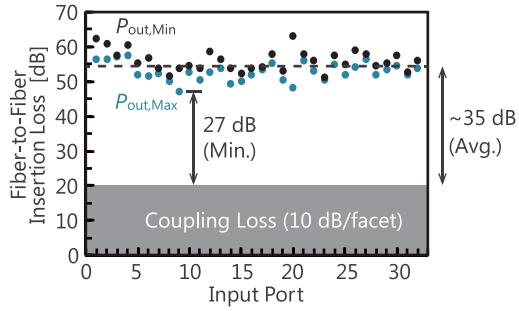

Fig. 7. Measured fiber-to-fiber insertion losses of sampled paths (1 (input)-1' (output), 2–2', …, 32–32'). $P_{\mathrm{out,\ Max}}$ and $P_{\mathrm{out,\ Min}}$ are the maximum and minimum output powers while adjusting the input polarization.

TABLE I
MINIMUM ON-CHIP LOSS BREAKDOWN

Devices	Insertion Loss (dB)
Routing WG (SSC to PSR)	0.6
Input PSR	3
Switch Matrix	6.1
SiN/Si Transfer	1.6
SiN WG	8.5
SiN Intersections	3.8 (i.e., 0.06 × 64)
Output PSR	3
Routing WG (PSR to SSC)	0.6

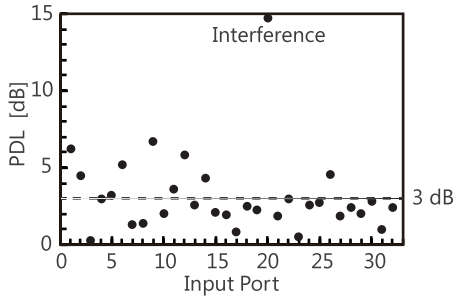

Fig. 8. Measured polarization-dependent losses of sampled paths (1 (input)-1'(output), 2–2', …, 32–32').

if we could calibrate all switches adequately, the insertion loss would be improved.

Fig. 8 shows the obtained PDLs of the sampled paths. The average and minimum PDLs are 3.5 and 0.32 dB, respectively. We note that the loss in 75% of the measured paths falls below 3 dB. We suspect that two factors caused the variation in the PDL, including the significantly high PDL of path 20-20'. The first factor is the interference between the light propagating through the established paths and the leakages from the path of the oppositely polarized component in the switch matrix. The other factor is the inadequate polarization splitting and rotating in the PSRs. We believe that the negative effects from these factors can be decreased by optimizing the design of the device,

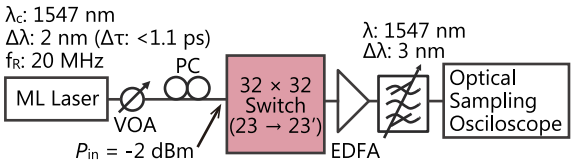

Fig. 9. Experimental setup for differential-group-delay evaluation with optical pulses. λ_c: center wavelength, $\Delta\lambda$: 3-dB spectrum width, $\Delta\tau$: pulse width (FWHM), f_R: repetition frequency, VOA: variable optical attenuator, PC: polarization controller, EDFA: erbium doped fiber amplifier.

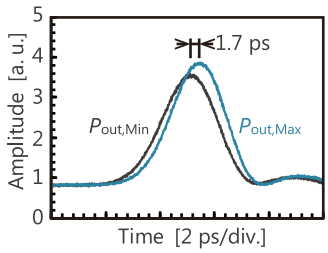

Fig. 10. Observed optical pulses at maximum ($P_{\mathrm{out,\ Max}}$) and minimum ($P_{\mathrm{out,\ Min}}$) output powers while adjusting the polarization of the input optical pulse.

fiber-to-chip coupling, and calibration algorithm of the element switches for leakage suppression.

C. Differential Group Delay (DGD)

We measured the differential group delay (DGD) by comparing the delay times of the optical pulses at the input polarization states with the maximum and minimum output powers. Fig. 9 shows the experimental setup. The optical pulses from a mode-locked laser are adjusted in terms of the power and polarization and then sent to the switch. In the switch, the lowest PDL path (23 → 23') was established. The output pulses were amplified using an erbium-doped fiber amplifier and then filtered at the center wavelength of the optical pulses. The filtered pulses were observed using an optical sampling oscilloscope (Agilent, 86100A, 86109B). Fig. 10 shows the observed pulses. The DGD was 1.7 ps. This value is low enough for signal transmission, such as 50 Gbaud. As the nominal optical path lengths of the two polarizations are equal in design, we infer that the residual DGD is caused by slight fluctuations of fabricated waveguide width. The path lengths of all the paths in the switch matrix are the same owing to the PILOSS topology. Therefore, we expect a similarly low DGD for all the paths.

D. Crosstalk

We characterized the crosstalk in one of the worst crosstalk switch states, as shown in Fig. 11. Path 30–31' is one of the worst paths having 29, 30, and 64 time crossings in the MZ switches, Si intersections, and SiN intersections, respectively. The crosstalk was defined as the transmitted power from path 30–31' divided by the sum of leakages from the other paths to the port 31'. Fig. 12 shows the measured output power from path 30–31' and the leakages from the other paths to port 31'. The crosstalk is

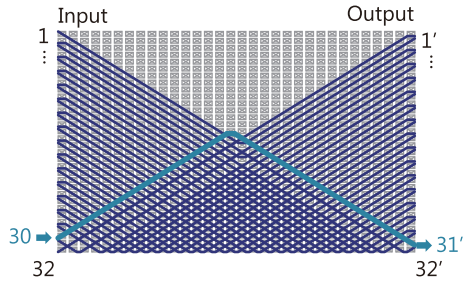

Fig. 11. One of the worst-case crosstalk switch states. The path from port 30 to port 31' is one of the worst paths with 29, 30, and 64 time crossings with other paths in the Mach–Zehnder switches, Si intersections, and SiN intersections, respectively.

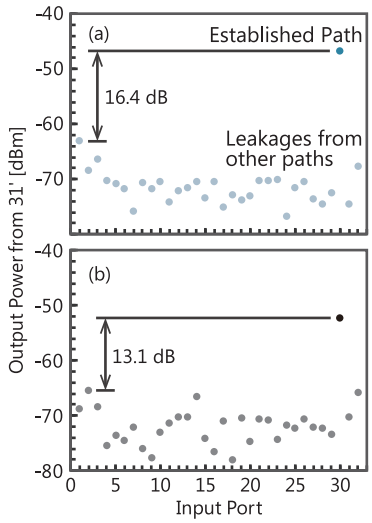

Fig. 12. Measured output powers from the established path and leakages from other paths to port 31': (a) Maximum and (b) minimum output cases while adjusting input polarization.

−8.8 dB in the maximum output case and −3.7 dB in the minimum output case. In this switch, we calibrated a limited number of element switches because of the interference effect and/or inadequate performance of the PSR. If all the element switches can be calibrated correctly, the crosstalk can be reduced.

IV. Conclusion

We fabricated a nonduplicate polarization-diversity 32 × 32 switch based on the SiN/Si double-layer platform. The fabricated switch exhibited a PDL of less than 3 dB for 75% of the measured paths and a DGD of 1.7 ps. These results confirm the feasibility of the polarization-insensitive operation of the nonduplicate polarization-diversity switch. The performance of the switch can be further improved by optimizing the structural parameters.

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