Delta-Sigma Modulation for Next Generation Fronthaul Interface

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Abstract—A new function split option for the next generation fronthaul interface (NGFI) is demonstrated based on all-digital RF transmitter using bandpass delta-sigma modulation. Different from other low layer split (LLS) options, such as option 6 (MAC-PHY), 7 (high-low PHY), and 8 (CPRI), the proposed option 9 implements RF functions in the digital domain, and splits within the RF layer, with high-RF layer centralized in the distributed unit (DU) and low-RF layer distributed in remote radio units (RRUs). A proof-of-concept all-digital RF transmitter based on real-time delta-sigma modulation is implemented using a Xilinx Virtex-7 FPGA. A 5-GSa/s delta-sigma modulator is demonstrated to encode LTE/5G signals with bandwidth up to 252 MHz and modulation format up to 1024-QAM to a 5-Gb/s OOK signal, which is transmitted over 30-km single-mode fiber from DU to RRU. To relax the FPGA speed requirement, a 32-pipeline architecture is designed. Two-carrier aggregation of 5G and 14-carrier aggregation of LTE signals are demonstrated with error vector magnitude (EVM) performance satisfying the 3GPP specifications. Compared with option 8 (CPRI), although the proposed option 9 split occurs at a lower level, it offers improved spectral efficiency and reduced NGFI data rate than CPRI. Moreover, other LLS options, such as 6, 7, and 8, all require a complete RF layer implemented in the analog domain at remote cell sites; whereas option 9 realizes high-RF layer in the digital domain at DU, and eliminates the need of analog RF devices, such as DAC, local oscillator and mixer at RRU, which not only makes low-cost, energy-efficient, and small-footprint cell sites possible for the wide deployment of small cells, but also paves the road toward software defined radio (SDR) and virtualization of DU and RRU for improved compatibility and reconfigurability among multiple radio access technologies (multi-RATs). Given its centralized architecture and deterministic latency, option 9 is suitable for radio coordination applications, and has potential in low-frequency narrowband scenarios with cost, power, and/or size sensitive cell sites, such as massive machine type communication (mMTC) and narrowband internet of things (NB-IoT).

Index Terms—All-digital RF transmitter, delta-sigma modulation, fronthaul, NGFI, software defined radio.

I. Introduction

THE emerging video-intensive and bandwidth-consuming services, e.g., virtual reality, augmented reality, immersive applications, are driving the explosive growth of mobile data traffic [1]–[3], making radio access networks (RAN) become the bottleneck of user experience. During 4G era, to enhance the capacity, coverage, and flexibility of mobile data networks, centralized/cloud-RAN (C-RAN) was proposed [4] to separate the baseband processing functions from base stations (BS) at cell sites, and consolidate them in a centralized baseband unit (BBU) pool, which not only simplifies each BS to a remote radio head (RRH), but also enables radio coordination among multiple cells [5]–[8]. In this way, C-RAN architecture is divided into two segments, i.e., backhaul from 4G evolved packet core (EPC) to BBUs and fronthaul from BBUs to RRHs. Common public radio interface (CPRI) proposed by CPRI cooperation (Ericsson, Huawei, NEC, Nokia) was adopted as the fronthaul interface [9]. However, it was quickly realized that as a digital interface developed for narrowband radio access technologies (RATs), e.g., UMTS (CPRI version 1 and 2), WiMAX (v3), LTE (v4), and GSM (v5) [9], CPRI suffers from limited scalability due to its low spectral efficiency and tremendous data rate. Moreover, it features traffic-independent constant data rate, which scales with antenna number and cannot support statistical multiplexing, making CPRI become the bottleneck in massive MIMO and large-scale carrier aggregation applications.

To circumvent the CPRI bottleneck, three strategies were developed, including analog fronthaul, CPRI compression, and next generation fronthaul interface (NGFI) based on new function splits. Analog fronthaul transmits mobile signals in their analog waveforms using radio-over-fiber (RoF) technology [10], [11], which features high spectral efficiency and simple low-cost system implementations but is susceptible to nonlinear and noise impairments [12]–[14]. CPRI compression solutions maintain the CPRI interface but manage to reduce the fronthaul data rate by exploiting compression algorithms [15]–[17] or nonlinear quantization techniques [18]–[20] with the penalty of additional hardware and latency.

By rethinking the RAN architecture and reorganizing its function distribution [21], the next generation RAN (NG-RAN) architecture is proposed with function split options other than option 8 (CPRI), including high layer split (HLS) and low layer split (LLS). NG-RAN has three segments, i.e., backhaul from core network to central unit (CU), midhaul (fronthaul II) from CU to distributed unit (DU), and fronthaul (fronthaul I or NGFI) from DU to remote radio unit (RRU) [22]–[24]. Option 2 was adopted by 3GPP as the HLS choice; whereas there is still debate among several candidates of LLS, including option 6 and 7 (7.1, 7.2, 7.3) proposed by 3GPP [25]–[27], and I_D, II_D, I_U interfaces proposed by CPRI cooperation in the Ethernet CPRI (eCPRI) specification [28], [29]. Both CPRI compression based

TABLE I
STATE-OF-THE-ART OF ALL-DIGITAL TRANSMITTER BASED ON DELTA-SIGMA MODULATION

Reference	Sampling rate (GSa/s)	Bandwidth (MHz)	Fc (GHz)	Signal band	Implementation	Pipeline #	Signal type
[30]	0.0352	1.1	Baseband	Lowpass	CMOS 0.5 μm	1	Continuous time Tx
[31]	0.7	< 1	0.175	Bandpass	CMOS 130 nm	1	GSM
[32]	2.625	200	5.25	Lowpass	CMOS 130 nm	1	Digital RF Tx
[33]	<3.6	10, 20	2.4-3.6	Lowpass	CMOS 90 nm	1	Digital RF Tx
[34]	5.4	5.6, 11.2, 20	2.4-2.7	Lowpass	CMOS 65 nm	1	Wi-Fi, WiMAX
[35]	2.6, 4	Up to 50	0.05-1	Bandpass	CMOS 90 nm	1	Digital RF Tx
[36]	0.05	0.25, 0.5	Baseband	Lowpass	Altera Stratix	1	OFDM, CDMA
[37]	0.045	1.25/1.23	2.45, 1	Lowpass	Altera Stratix	1	WiMAX, CDMA, EDGE
[38]	0.64, 0.8	3.84/7.68 (LTE) 4/8 (WiMAX)	2.1, 2.5	Lowpass	Altera Stratix II GX	8	WiMAX, LTE
[39]	0.025	1.6	1	Lowpass	Unknown FPGA	4	CDMA
[40]	3.9	5+5	0.8, 1.5	Dual-band	Unknown FPGA	1	Dual-band LTE
[41]	0.225	1.25+1.5	0.45, 0.9	Lowpass	Xilinx Virtex 6 HX380T on ML628	1	Dual-band WiMAX + SC-QAM[1]
[42]	0.15625	1.25+1.5	1.25, 0.78125	Lowpass	Xilinx Virtex 6 HX380T on ML628	1	Dual-band SC-64QAM + WiMAX
[43]	1/0.9 (1st/2nd order)	Up to 12.5	1, 0.9	Lowpass	Xilinx Virtex 6 HX380T on ML628	4	Single-carrier
[44]	3.2	6.1-122	1.6	Lowpass	Xilinx Virtex 6 VHX280T on ML628	16	Single-carrier
[45]	3.2	6-120	3.2	Lowpass	Xilinx Virtex UltraScale XCVU095 on VCU1287	16	Single-carrier
[46]	0.7	5	0.7	Envelope	CMOS 90 nm	1	LTE
[47]	10.4 = 0.325 * 32	20	5.2	Lowpass	Xilinx UltraScale XCVU095 on VCU108	32	Wi-Fi 802.11a
[48]	9.6 = 0.3 * 32	488	4.8	Lowpass	Xilinx UltraScale XCVU095 on VCU108	32	SC-64QAM
[49][3]	6.25	20+20	0.856, 1.45	Dual-band	Simulation + AWG[2]	1	Dual- band LTE
[50]	6.25	10+20	0.874, 1.501	Dual-band	Simulation + AWG	1	Dual-band LTE
[51]	2.15	5+10	0.244, 0.5	Dual-band	Simulation + AWG	1	Dual-band LTE
[52]	7	10+10+10	0.71, 1.75, 2.51	Triple-band	Simulation + AWG	1	Triple-band LTE
[60, 61]	10	625	Baseband	Lowpass	Simulation + AWG	1	32 LTE carrier aggregation
[62, 63]	16-32	1200	Baseband	Lowpass	Simulation + AWG	1	5 DOCSIS 3.1 channels
This work	5	99-252	0.96	Bandpass	Xilinx Virtex-7 VX485T on VC707	32	5G, LTE carrier aggregation

[1]SC-QAM: single-carrier quadrature amplitude modulation.

[2]AWG: arbitrary waveform generator.

[3]The performance of references [30]–[48] are illustrated in Fig. 1. References [49]–[52], [60]–[63] are not included since they are not implemented by CMOS or FPGA, but by offline processing.

on option 8 and other LLS candidates require a complete RF layer implemented in the analog domain at each remote cell site, which increases the complexity and cost of small cells.

Different from the popular trends of moving LLS from option 8 to a higher level, e.g., option 6, 7, we propose a disruptive option 9 to push the LLS further deeper into the RF layer, with functions of high-RF layer centralized in DU, and low-RF layer distributed in RRUs. Enabled by all-digital RF transceiver based on delta-sigma modulation, the proposed option 9 implements both baseband and RF functions in the digital domain, which not only improves the spectral efficiency compared with CPRI, but also eliminates the need of analog RF devices, such as DAC, local oscillator (LO) and mixer at RRUs, making simple, low-cost, and energy-efficient RRU possible for small cell deployment in the 5G era.

Meanwhile, the vision of software defined radio (SDR) is to push the AD/DA conversion as close as possible to the antenna, leaving both baseband and RF processing in the digital domain for enhanced flexibility and compatibility to multiple radio access technologies (multi-RATs) with different PHY layer specifications. SDR also enables dynamically reconfigurable function split, since different 5G scenarios with drastically

different requirements in terms of data rate and latency, e.g., enhanced mobile broadband (eMBB), ultra-reliable low latency communication (uRLLC), and massive machine type communication (mMTC), can benefit from reconfigurable function split. As a cornerstone of SDR, all-digital RF transceiver based on delta-sigma modulation has attracted intensive research interest due to its low cost and flexibility to accommodate multiband multi-RAT operations. Both transmitter [30]–[52] and receiver [53]–[59] designs have been reported, and various delta-sigma modulators, including lowpass [30], [32]–[34], [36]–[39], [41]–[45], [47], [48], bandpass [31], [35], and multiband [40], [49]–[52] have been demonstrated. To relax the FPGA speed requirement, several time-interleaving or parallel processing techniques are also presented [38], [39], [43]–[45], [47], [48]. Table I and Fig. 1 show a summary of all-digital transmitters based on delta-sigma modulation, implemented by either CMOS or FPGA. In [48], a 9.6 GSa/s, 488-MHz signal bandwidth lowpass delta-sigma modulator was demonstrated with 32 pipelines and 300-MHz clock rate in each line, but only second-order delta-sigma modulation was realized to accommodate the speed of FPGA. In this work, we present a fourth-order bandpass delta-sigma modulator, which has the highest sampling rate and
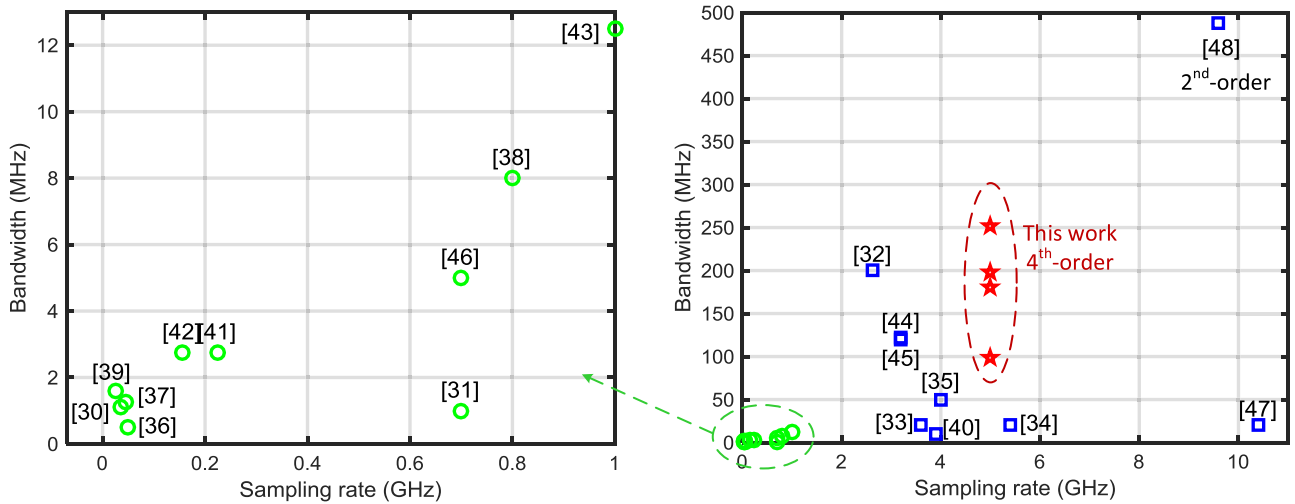
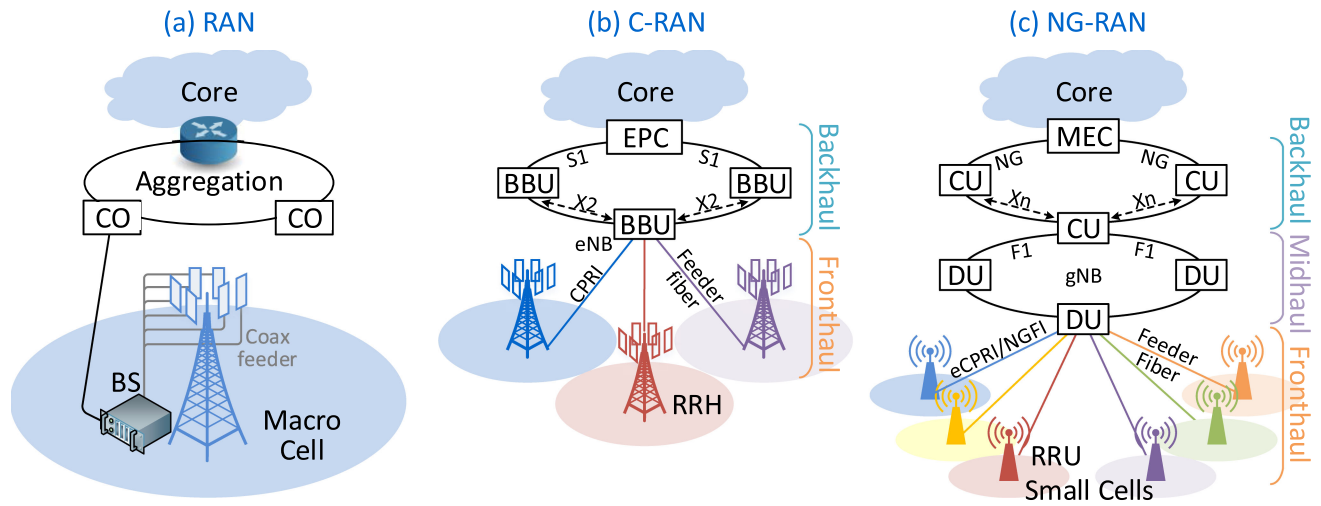Fig. 1. State-of-the-art of delta-sigma modulator for all-digital RF transmitter.

Fig. 2. Evolution of radio access network (RAN). (a) 3G RAN. (b) 4G cloud/centralized-RAN (C-RAN). (c) Next generation-RAN (NG-RAN) for 5G.

widest reported signal bandwidth for fourth-order modulation. It also uses a 32-pipeline architecture, but the FPGA clock rate in each pipeline is limited to 156.25 MHz due to the increased order.

In [60]–[63], we first proposed to replace CPRI by delta-sigma modulation to improve the fronthaul spectral efficiency, but those modulators were realized by offline processing. So far, there is no demonstration of real-time delta-sigma modulation for NGFI application. In this paper, we propose a new NGFI function split option 9 enabled by all-digital RF transmitter based on delta-sigma modulation, and present a real-time FPGA demonstration for the first time. The proposed option 9 not only improves the spectral efficiency, but also simplifies RRU design to facilitate the deployment of small cells. The all-digital RF transceiver design enables SDR and virtualization of DUs, making NG-RAN compatible with multiple RATs, including 4G-LTE, Wi-Fi, and 5G-NR, etc.

The paper is organized as follows. Section II discusses NG-RAN and its function split. Section III explains operation prin-

ciples of the proposed option 9 function split. Sections IV and V present the experimental setup and results. A comparison of option 9 with CPRI and other functions split options, e.g., 6, 7, are given in Section VI. Section VII concludes the paper.

II. NG-RAN AND FUNCTION SPLIT

Fig. 2 shows the RAN evolution from 3G, 4G toward 5G. In the 3G RAN (Fig. 2(a)), both baseband and RF processing functions locate in an all-in-one BS at each cell site, and mobile signals are fed from BS to antennas via coaxial cables due to the short distance. In Fig. 2(b), C-RAN architecture separates the baseband processing functions from each BS, and consolidates them into a centralized BBU pool, so each BS is simplified to a RRH. Since the distance between BBU and RRH is extended to tens of kilometers, mobile signals are transmitted via digital fiber links with CPRI interface. Due to the CPRI bottleneck, NG-RAN architecture is proposed with function split other than
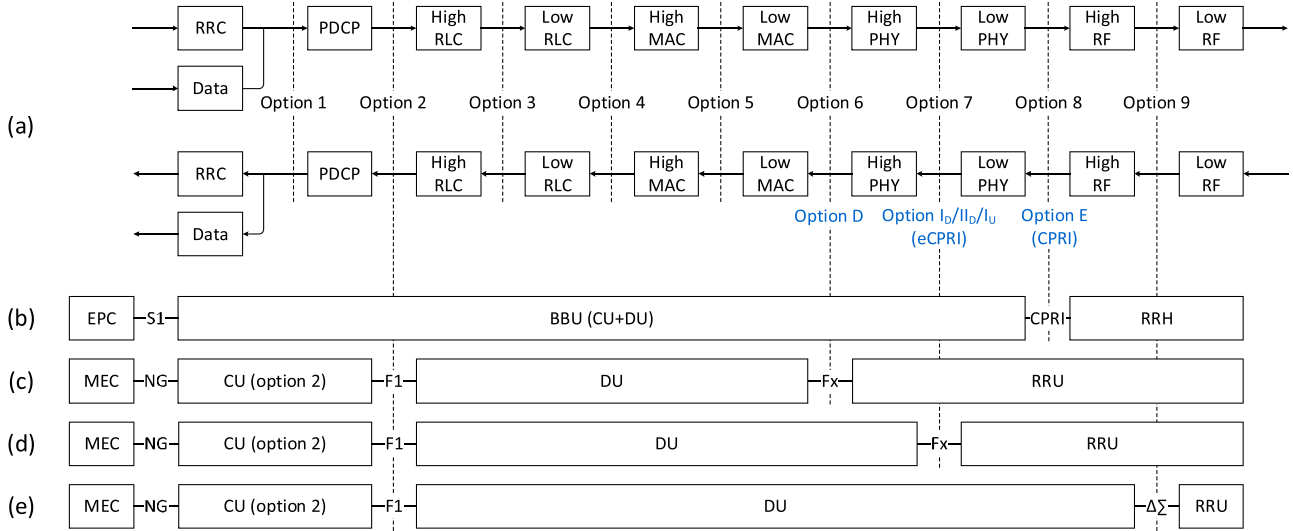
Fig. 3. Function split options of C-RAN and NG-RAN. (a) Block diagram of functions [23]–[26]. (b) C-RAN architecture with option 8 (CPRI) split between BBU and RRH. (c, d) NG-RAN architectures with HLS of option 2 between CU and DU, and LLS of option 6 (MAC-PHY) or 7 (high-low PHY) between DU and RRU [25], [26]. (e) NG-RAN with LLS of option 9 (high-low RF).
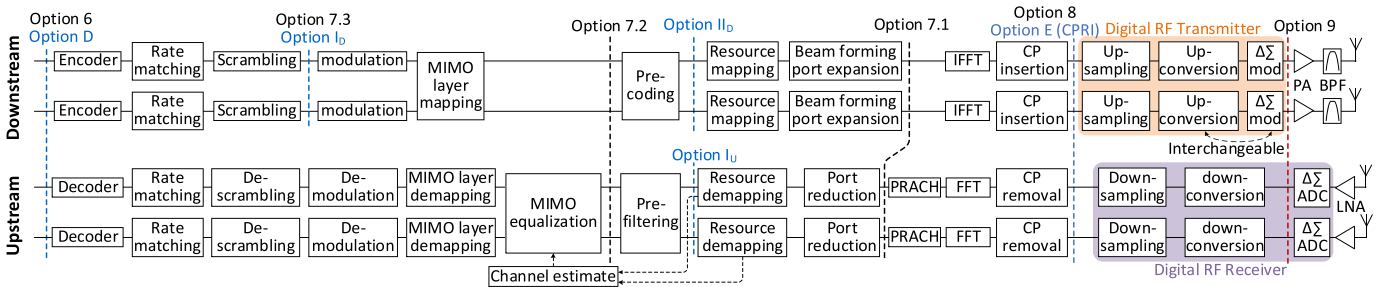

Fig. 4. Block diagram of functions in PHY and RF layers [28], [29], including downstream and upstream. 2×2 MIMO is used as an example to illustrate MIMO processing.
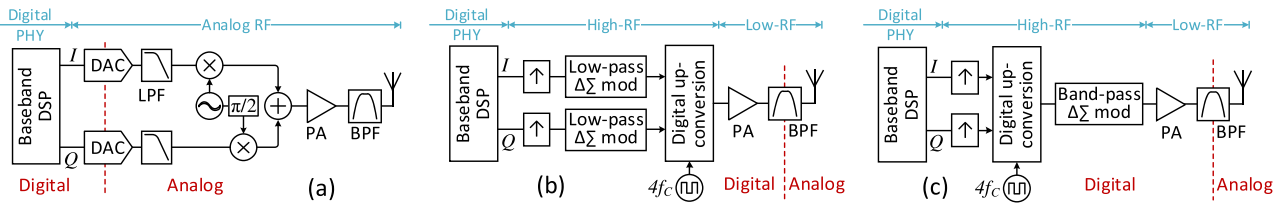

Fig. 5. Architectures of analog/digital RF transmitter. (a) Analog RF transmitter based on DAC and analog RF chain. (b) All-digital transmitter based on low-pass delta-sigma modulation and digital up-conversion. (c) All-digital transmitter based on digital up-conversion and bandpass delta-sigma modulation.

option 8, including HLS and LLS, shown in Fig. 2(c). Baseband functions in BBUs are distributed into CU and DU, dividing NG-RAN into three segments, i.e., backhaul from mobile edge computing (MEC) to CU, midhaul from CU to DU, and fronthaul from DU to RRU.

Fig. 3 shows a comprehensive summary of function split options for C-RAN and NG-RAN. Fig. 3(a) shows the block diagram of functions including radio resource control (RRC), packet data convergence protocol (PDCP), radio link control (RLC), media access control (MAC), physical (PHY), and RF layers [23]–[26]. Fig. 3(b) shows the C-RAN architecture with option 8 (CPRI) split between BBU and RRH [25], [26]. Fig. 3(c) and (d) show the NG-RAN architectures with HLS of option 2 between CU and DU, and LLS of option 6 (MAC-PHY) or 7 (high-low PHY) between DU and RRU [25], [26].

Fig. 3(e) shows LLS of option 9, where the high-RF layer is implemented in the digital domain and centralized in DU, leaving only low-RF layer in RRU. Fig. 4 shows a detailed block diagram of functions within the PHY and RF layers [28], [29]. Function split options proposed by 3GPP are labeled in black, and options from eCPRI specification are labeled in blue. The MAC-PHY split is defined as option 6 by 3GPP or option D in eCPRI specification; PHY-RF split is defined as option 8 by 3GPP and option E in eCPRI specification. Within the PHY layer, both 3GPP and CPRI cooperation offer three different options, 7.1, 7.2, 7.3, and I_D, II_D, I_U. Only 7.1 and 7.2 are bi-directional; the rest are for one direction only, i.e., 7.3, I_D, II_D for downstream, and I_U for upstream.

In Fig. 4, the RF layer consists of a downstream digital RF transmitter based on delta-sigma modulator and an upstream
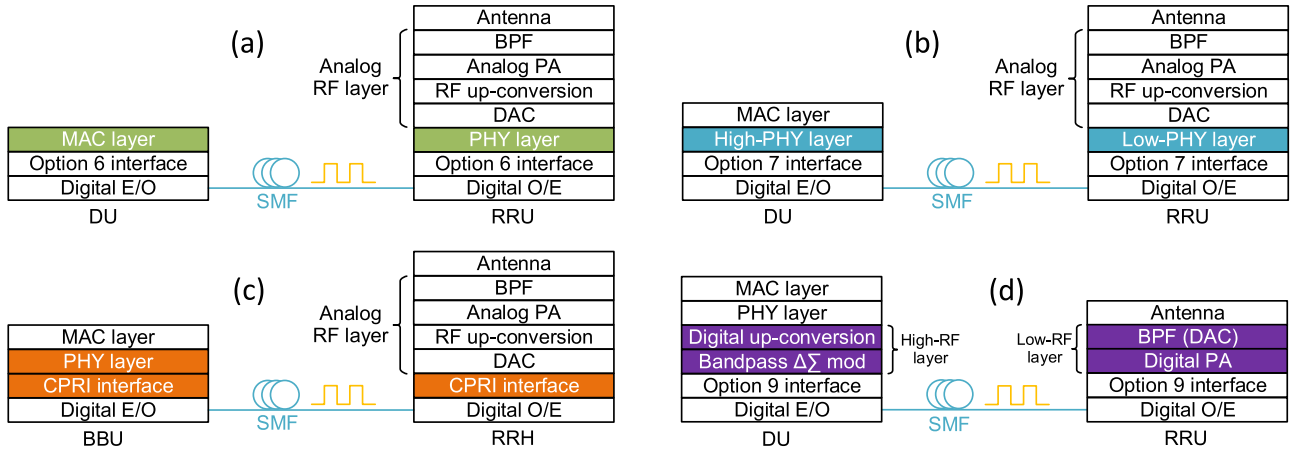
Fig. 6. Architecture comparison of different LLS options of 6, 7, 8 and 9. (a) Option 6 split between MAC and PHY layers. (b) Option 7 split within the PHY layer. (c) Option 8 (CPRI) split between PHY and RF layer. (d) Option 9 split within the RF layer. Except option 9, all other LLS options have a complete RF layer implemented in the analog domain at RRU, including DAC, local oscillator, mixer and linear power amplifier.

digital RF receiver based on continuous-time delta-sigma ADC. Two architectures of digital RF transmitter are shown in Fig. 5. Except for option 9, all other LLS options including 6, 7, and 8, implement RF layer in the analog domain, consisting of local oscillator (LO), mixer, filter, and linear power amplifier (PA), shown in Fig. 5(a), where a DAC separates the digital processing of baseband signals from the analog processing of RF signals. For option 9 split, on the other hand, the RF layer is implemented in the digital domain, and there is no analog LO, mixer, or linear PA. In Fig. 5(b), baseband I and Q signals are first up-sampled, then encoded by two low-pass delta-sigma modulators, respectively, where the discrete-time multibit baseband I/Q signals are converted to two one-bit data streams. Then a digital frequency up-converter converts the I/Q bit streams to radio frequency. In Fig. 5(c), after up-sampling, I and Q components are first up-converted to radio frequency, then encoded by a bandpass delta-sigma modulator. Since delta-sigma modulation utilizes noise shaping to push the quantization noise out of the signal band, a bandpass filter (BPF) not only filters out the desired signal, but also eliminates the out-of-band noise and retrieves the analog waveform. Therefore, the conventional DAC is replaced by a simple, low-cost BPF. This also aligns with the view of digital RF transceiver to push the DAC as close as possible to the antenna, so both baseband and RF processing are carried out in the digital domain.

One advantage of all-digital transmitter is its flexibility and reconfigurability to different carrier frequencies and multiple RATs. As a cornerstone to SDR, it enables the virtualization of DU and RRU, making NG-RAN compatible with 4G-LTE, Wi-Fi, and 5G-NR. Another advantage of all-digital transmitter is high linearity. In Fig. 5(a), both PA and BPF are dealing with an analog RF signal, and nonlinear impairments are inevitable. But in Fig. 5(b) and (c), the PA is placed before BPF, which acts as a DAC, so the PA is in the digital domain, so high-efficiency switch-mode PA can be used without nonlinearities. One limitation of all-digital transmitters is the high oversampling rate, and a clock rate four times of carrier frequency is needed for digital up-conversion.

III. OPTION 9 FUNCTION SPLIT

The RF layer in Fig. 4 uses a digital RF transmitter based on a bandpass delta-sigma modulator as shown in Fig. 5(c). For downstream, option 9 function split takes place after the bandpass modulator, which encodes the discrete-time multibit signal into a one-bit data stream and transmits it from DU to RRU via digital fiber links. For upstream, a digital RF receiver based on a continuous-time delta-sigma ADC is used to digitize the received analog signal to discrete levels, and option 9 split takes place after the delta-sigma ADC, transmitting digital bits representing these discrete levels from RRU back to DU.

Fig. 6 shows the architecture of different function split options, including 6, 7, 8, and 9. Fig. 6(a) shows the architecture of option 6 (MAC-PHY) split, where the MAC layer is centralized in DU, whereas both PHY and RF layers are distributed in the RRU. Note that baseband processing of the PHY layer is implemented in the digital domain; whereas the RF layer is implemented by analog RF chain, including DAC, LO, mixer, and PA.

Fig. 6(b) shows a digital fronthaul based on option 7 split. Baseband processing in the high-PHY layer is carried out in DU; the remaining baseband processing in the low-PHY layer is implemented in RRU. After DAC, all the RF functions are realized in the analog domain at RRU. Option 7 effectively reduces the fronthaul data rate compared with CPRI, but also increases the cost and complexity of RRU at cell site, which hinders the wide deployment of small cells.

Fig. 6(c) shows a digital fronthaul based on option 8 (CPRI) split. Digital fiber link transmits the digital signals after FFT and separates PHY and RF layers in DU and RRU, respectively. Like option 7, after a DAC, all RF layer functions are carried out in the analog domain at RRU. CPRI has low spectral efficiency, requires tremendous data rate, and has limited scalability for massive MIMO and carrier aggregation. Moreover, CPRI has a fixed chip rate (3.84 MHz), and can only accommodate UMTS (v1 and 2), WiMAX (v3), LTE (v4), and GSM (v5).

Fig. 6(d) shows a digital fronthaul based on option 9 split, with both PHY and RF layers implemented in the digital domain.
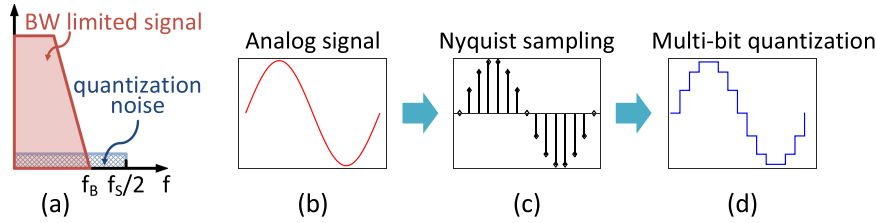
Fig. 7. Operation principles of Nyquist ADC. (a) Each signal is digitized at baseband. Quantization noise is evenly distributed in the Nyquist zone. (b) Input analog signal. (c) Nyquist sampling. (d) Multi-bit quantization.
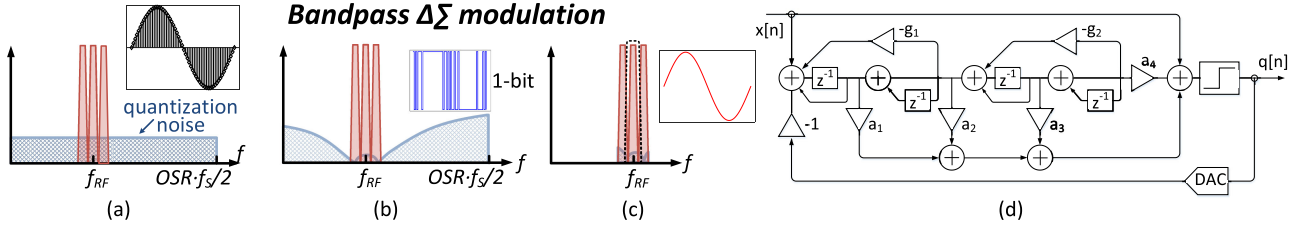

Fig. 8. Operation principles of bandpass delta-sigma modulation. (a) Oversampling expands the Nyquist zone. (b) Noise shaping pushes the quantization noise out of the signal band. (c) BPF not only filters out the desired signal, but also eliminates the out-of-band noise to retrieve the analog waveform. BPF acts as an essential DAC of an all-digital transmitter. (d) Cascaded-resonator feedforward structure of bandpass delta-sigma modulator.

PHY and high-RF layers, i.e., digital up-conversion, delta-sigma modulation, are centralized in DU; only low-RF layer functions, e.g., PA, BPF, are left in RRU. Since the BPF acts as the effective DAC of an all-digital transmitter, PA works in the digital domain, and high efficiency switching-mode PA can be used. Option 9 split enables a low-cost, DAC-free and RF-simple RRU design, which reduces the cost and complexity of cell site, and facilitates the dense deployment of small cells.

Since option 7 and 8 transmit digital baseband signals over fronthaul interface, time division multiplexing (TDM) is needed to interleave the baseband I/Q components, and components from multiple mobile signals, and time synchronization might be an issue considering the coexistence of legacy RAT and 5G-NR. On the other hand, option 9 transmits digital RF signal with I/Q components already converted to radio frequency, and frequency division multiplexing (FDM) can be used to accommodate multiband mobile signals.

Figs. 7 and 8 show the operation principles of Nyquist ADC and bandpass delta-sigma modulation, respectively. For a Nyquist ADC, each analog signal is digitized at baseband with a Nyquist sampling rate. The quantization noise is evenly distributed in the frequency domain. To reduce the quantization noise, multiple quantization bits are used for each sample, which leads to low spectral efficiency and large data rate after digitization and makes CPRI become the fronthaul bottleneck.

Different from Nyquist ADC, delta-sigma modulation trades quantization bit for sampling rate, using high sampling rate and only few quantization bits. After baseband processing, digital baseband signal is up-converted to radio frequency, then a bandpass delta-sigma modulation encodes the discrete-time multibit RF signal into a one-bit data stream. In Fig. 8(a), oversampling extends the Nyquist zone, so quantization noise can be spread over a wide frequency range. In Fig. 8(b), noise shaping

technique pushes the quantization noise out of the signal band and separates the signal and noise in the frequency domain. After delta-sigma modulation, the signal waveform is transformed from analog to digital by adding out-of-band quantization noise. In Fig. 8(c), at RRU, a BPF filters out the desired signal, which not only eliminates the out-of-band noise, but also retrieves the analog waveform as an effective DAC. Due to the noise shaping, the retrieved analog signal has an uneven noise floor.

In this paper, a one-bit bandpass delta-sigma modulator is implemented using a 4th-order cascaded resonator feedforward (CRFF) structure, shown in Fig. 8(d). There are four stages of feedback loops (z^{-1}), each two cascaded together to form a resonator. There is a feedback path in each resonator, g_1, and g_2. The outputs of four stages are feedforwarded with coefficients of a_1, a_2, a_3, and a_4 to the combiner, then a one-bit quantizer acts as a comparator and outputs a one-bit (0/1) OOK signal.

IV. EXPERIMENTAL SETUP

Using the CRFF structure in Fig. 8(d), a real-time one-bit bandpass delta-sigma modulation is demonstrated with Xilinx Virtex-7 VX485T FPGA on a VC707 development board, shown in Fig. 9(a). A FPGA mezzanine card (FMC170) from 4DSP is inserted in the high-pin count (HPC) connector on VC707 as the input ADC. The FMC170 ADC has a sampling rate of 5 GSa/s and 10 quantization bits per sample. The input analog signal is first digitized to 10 bits, then fed to the FPGA to perform delta-sigma modulation, which transforms the 10 input bits to one output bit. After delta-sigma digitization, the output 5-Gb/s OOK signal is outputted via a multi-gigabit transceiver (MGT) port on VC707. The 5-GSa/s sampling rate of FMC170 is contributed by 32 time-interleaved ADCs, each working at 156.25 MSa/s, so the FMC170 clock rate is 156.25 MHz. In
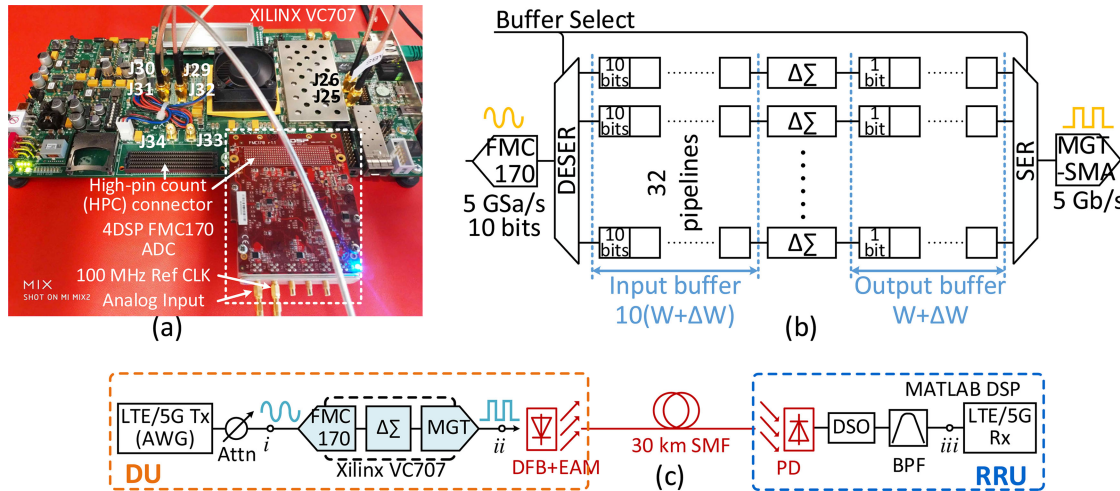
Fig. 9. Experimental setup. (a) Xilinx Virtex-7 VX485T FPGA on VC707 development board with 4DSP FMC170 ADC. (b) 32-Pipeline architecture to relax FPGA speed. (c) Optical testbed.

TABLE II
OFDM PARAMETERS OF 4G-LTE AND 5G-NR SIGNALS USED IN THE EXPERIMENTS

Case	Signals	Sampling rate (MSa/s)	FFT size	Subcarrier spacing (kHz)	Data subcarriers	Carrier number	Actual BW (MHz)	Modulation (QAM)
I	5G-NR	122.88	4096	30	3300	1	99	1024
II						2	198	256*2
III	4G-LTE	30.72	2048	15	1200	10	180	256*6, 1024*4
IV						14	252	1024*2, 256*4, 64*8

each clock cycle, it outputs $32 * 10 = 320$ bits for 32 consecutive samples.

In Fig. 9(b), due to the speed limit of FPGA, a 32-pipeline architecture is designed to match the speed difference between the FPGA and FMC170. The input samples are de-serialized and sequentially filled into the first-in-first-out (FIFO) buffers in 32 pipelines. In each pipeline, once the input FIFO is filled up, delta-sigma modulation is performed, and the output bits are stored in an output FIFO. The output bits from 32 output FIFOs are serialized to a single bit stream. Since delta-sigma modulation is performed parallelly in all 32 pipelines, the operation speed of each line is relaxed to 156.25 MSa/s. Assuming each FIFO can store W samples with ΔW margin, since the input ADC has 10 bits per sample, each input FIFO has a size of $10(W + \Delta W)$ bits. The margin ΔW is allocated to each buffer for easy implementation. After delta-sigma modulation, the 10 input bits are transformed to one output bit, so the output FIFO has a size of $W + \Delta W$ bits.

Note that memoryless signal processing can be easily implemented by pipeline architecture, since the processing to each sample only depends on the current sample and has no relation with previous ones. After segmenting the input sample stream into several blocks, all blocks can be processed in parallel without performance penalty. On the other hand, delta-sigma modulation is a sequential operation with memory effect. The output bit not only depends on the current sample, but also previous ones, which makes it difficult to implement in a parallel way. There will be performance penalty to segment a contin-

uous sample stream into several blocks, and the smaller block size is, the larger penalty will be. By making a tradeoff between performance penalty and the memory usage on FPGA, we choose a buffer size of $W = 20$ k with margin of $\Delta W = 2$ K. There have been several parallel processing techniques reported for high-speed, wide bandwidth delta-sigma modulators, including polyphase decomposition [44], [45], look-ahead time-interleaving [47], [48]. For a proof-of-concept experiment, here we only demonstrate the basic idea of pipeline processing with large buffer size. With the help of these parallel processing techniques, buffer size and processing latency can be significantly reduced.

Fig. 9(c) shows the experimental testbed. Carrier aggregated LTE/5G signals are generated by a Tektronix 7122C arbitrary Waveform Generator (AWG), then captured by the FMC170 ADC working at 5 GSa/s. The FPGA works as a one-bit bandpass delta-sigma modulator, transforming the 10 input bits to one output bit, and outputs a 5-Gb/s OOK signal. The OOK signal is delivered from DU to RRU via a digital fiber link, consisting of a 12.5 Gb/s Cyoptics DFB+EAM, 30-km single-mode fiber, and a 10 Gb/s Discovery optical receiver. 5-Gb/s error free transmission is achieved and the received OOK signal is captured by a 20 GSa/s Keysight data storage oscilloscope (DSO) MSOS804A and followed by real-time MATLAB DSP for bandpass filtering and LTE/5G receiving.

Four experimental cases are designed to verify the proposed all-digital transmitter based on delta-sigma modulation, and their OFDM parameters are listed in Table II. 30 kHz subcarrier
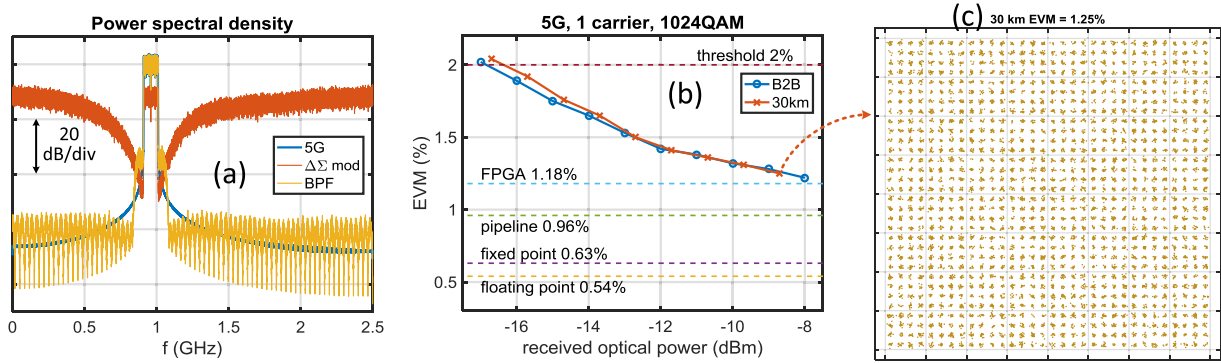
Fig. 10. Experimental results of Case I: one 5G carrier with 99-MHz bandwidth and 1024-QAM. (a) Electrical spectra of the input analog signal, the OOK signal after delta-sigma modulation, and the retrieved analog signal after BPF, respectively. (b) EVM vs received optical power. (c) Received constellation after 30-km fiber.

TABLE III
EVM REQUIREMENTS FROM 3GPP TS 36.104 V15.2.0 [64]

Modulation	QPSK	16-QAM	64-QAM	256-QAM	1024-QAM
EVM (%)	17.5	12.5	8	3.5	2.5 (2)*

*EVM requirement of 1024-QAM was first specified by TS 36.104 V15.2.0 in 03/2018. Since this work is done before that date, we used a stricter criterion of 2%.

spacing is used for 5G signals with FFT size of 4096 and 122.88 MSa/s sampling rate. The number of active subcarriers is 3300, and the signal bandwidth of each 5G carrier is 99 MHz. The system performance is evaluated by the error vector magnitude (EVM) of received signals, and 3GPP requirements of different modulations are listed in Table III [64]. Note that the EVM requirement of 1024-QAM is first specified by TS36.104 V15.2.0 in 03/2018. Since this work was done earlier than that date, we use a stricter criterion of EVM < 2%.

In Case I, one 5G carrier with 1024-QAM and 99-MHz bandwidth is used, and the EVM performance of received signal is less than 1.25%. In case II, two 5G carriers with 256-QAM are used. Since the signal bandwidth is doubled to 198 MHz, the oversampling rate (OSR) is halved with reduced signal-to-noise ratio (SNR). So lower modulation format is used to accommodate the increased EVM, and less than 2.83% EVM is achieved for both 5G carriers. Case III and IV deal with LTE signals. In Case III, 10 LTE carriers are used with different modulations loaded on different carriers, depending on their SNR. As shown in Table II, there are four carriers with sufficient SNR to support 1024-QAM, whereas the rest six carriers supporting 256-QAM. Similarly, in the 14 carriers in Case IV, there are two 1024-QAM, four 256-QAM, and eight 64-QAM. The reduction of modulation formats is due to the wider signal bandwidth and increased quantization noise.

V. EXPERIMENTAL RESULTS

The experimental results of Case I are shown in Fig. 10. One 5G carrier with 1024-QAM and 99 MHz bandwidth centered at 960 MHz is generated by the AWG and converted to a 5-Gb/s OOK signal by the bandpass delta-sigma modulator on FPGA. Fig. 10(a) shows the RF spectra of input and output signals of the delta-sigma modulator. The input 5G signal at point i in the experimental setup (Fig. 9(c)) is labeled in blue; OOK signal after FPGA at point ii in red; the retrieved analog signal after BPF at point iii in yellow. For the retrieved analog signal, the adjacent channel leakage ratio (ACLR) is determined by the residual out-of-band noise after BPF. For easy implementation, a finite impulse response (FIR) Kaiser window filter with 40 dB out-of-band antennation was used. By using a filter with higher out-of-band antennation, it is not difficult to achieve the 44.2 dB ACLR requirement specified in 3GPP TS 36.141 [65].

Fig. 10(b) shows the EVM of the retrieved 5G signal as a function of the received optical power. Verilog simulation results, including floating point, fixed point, and pipeline, are also presented to show the step-by-step FPGA implementation and the performance penalty in each step. Compared with back-to-back transmission, there is no EVM penalty observed after 30-km fiber, and the received constellation is shown in Fig. 10(c).

The experimental results of Case II are shown in Fig. 11. Two 5G carriers with 198-MHz total bandwidth and 256-QAM are converted to a OOK signal by the bandpass delta-sigma modulator on FPGA. Compared with Case I, lower modulation formats are employed due to the doubled signal bandwidth and increased quantization noise. The electrical spectra of the input analog signal (point i in Fig. 9(c)), OOK signal (point ii), and retrieved analog signal (point iii) are presented in Fig. 11(a). EVMs of both carriers as functions of received optical power are shown in Fig. 11(b). After 30-km fiber transmission, EVMs of both carriers are less than 2.80% and 2.83%, satisfying the 3.5% requirements of 3GPP. Constellations after 30-km fiber are shown in Fig. 11(c) and (d).

Fig. 12 shows the experimental results of Case III, where 10 LTE carriers are used with different modulations assigned on different carriers according to 3GPP requirements. Fig. 12(a) shows the electrical spectra of input analog, OOK, and retrieved analog signals. Fig. 12(b) shows the EVMs of each LTE carrier. Within the 10 carriers, there are four carriers (2, 3, 8, 9) with EVM less than 2%, which can support modulation up to 1024-QAM; the rest six carriers (1, 4–7, 10) have EVMs less than 3.5%, and are able to support 256-QAM. The results of Case IV are shown in Fig. 13. Due to the increased signal bandwidth, within the 14 carriers, there are only two carriers (3 and
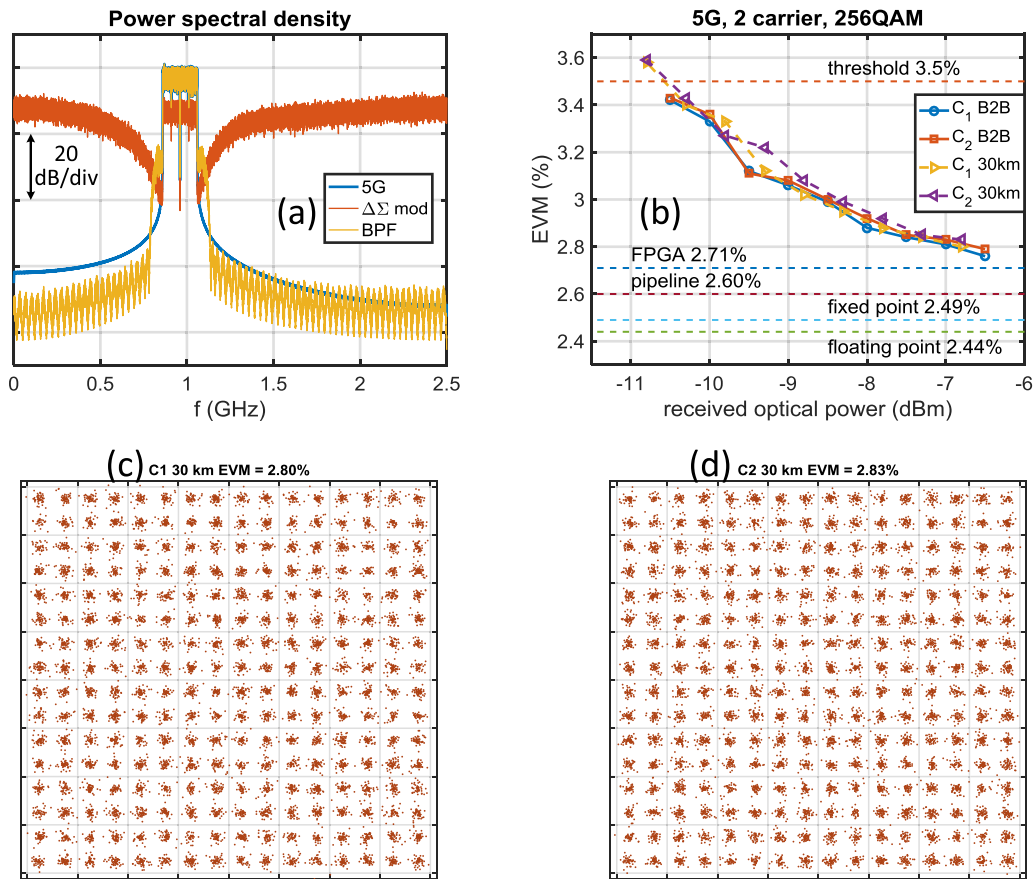
Fig. 11. Experimental results of Case II: two 5G carriers with 198-MHz total bandwidth and 256-QAM. (a) Electrical spectra of the input analog signal, the OOK signal after delta-sigma modulation, and the retrieved analog signal after BPF, respectively. (b) EVM of two 5G carriers vs received optical power. (c), (d) Received constellations after 30-km fiber.
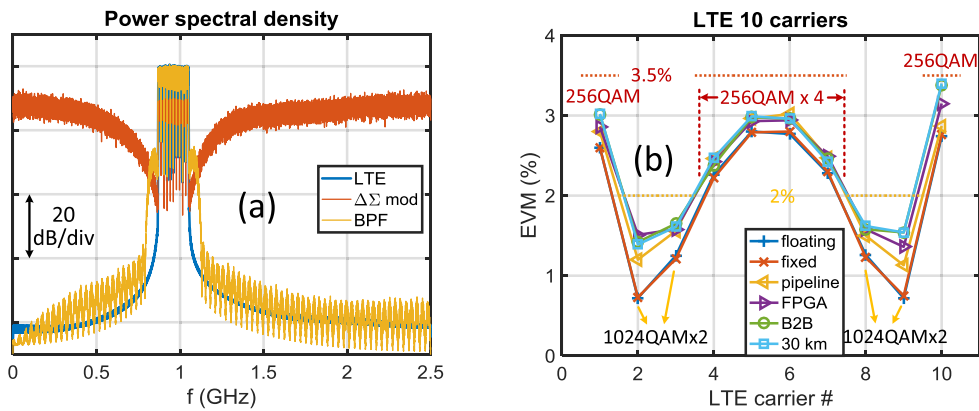

Fig. 12. Experimental results of Case III. (a) Electrical spectra of 10 LTE carriers. (b) EVMs of 10 LTE carriers.

12) with EVM smaller than 2%, and they can support modulation of 1024-QAM. There are four carriers (2, 4, 11, 13) with EVM less than 3.5% and used to carry 256-QAM; and the rest eight carriers (1, 5–10, 14) carry 64-QAM.

A summary of the resource utilization of Xilinx Virtect-7 FPGA is listed in Table IV. All four cases have similar resource usage, and the values listed are from Case II, 5G two-carrier aggregation. Note that 35.53% memory usage is due to the 22 k

TABLE IV
RESOURCE UTILIZATION OF XILINX VIRTEX-7 VX485T FPGA

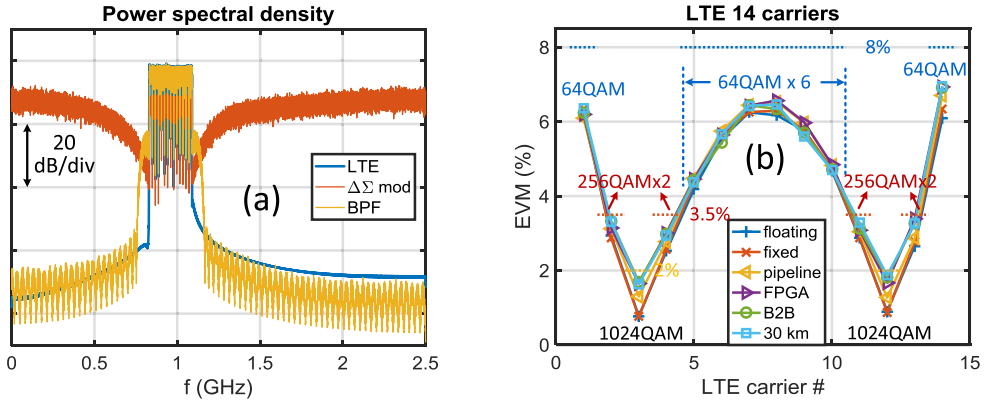| Resource	Utilization	Available	Utilization %
Logic cells	53362	485760	10.99%
DSP slices	64	2800	2.29%
Memory	13.18 Mb	37.08 Mb	35.53%
Transceivers	2	56	3.57%
I/O	181	700	25.86%
Max clock rate	156.25 MHz	650.20 MHz	N/A

Fig. 13. Experimental results of Case IV. (a) Electrical spectra of 14 LTE carriers. (b) EVMs of 14 LTE carriers.

TABLE V
DATA RATE AND EFFICIENCY COMPARISON OF CPRI, CPRI-COMPRESSION, AND DELTA-SIGMA MODULATION FOR NGFI

NGFI	CPRI-based solutions[1]			Delta-sigma modulation				
	CPRI	Statistical Compression	Lloyd Compression[3]				This work	
References	[9]	[18, 19]	[20]	[60]	[61]	[61]	This work	
Order		N/A		2	4	4	4	4
Sampling rate (MSa/s)	30.72	23.04	30.72	10,000	10,000	10,000	5,000	5,000
Bits	15[2]	8	8	1	1	2	1	1
Fronthaul data rate (Gbps)	0.9216	0.36864	0.49152	10	10	20	5	5
LTE carrier #		1		32	32	32	10	14
LTE bandwidth (MHz)		18		576	576	576	180	252
Modulation		1024		64*18 16*14	256*16 64*16	1024*10 256*22	1024*4 256*6	1024*2 256*4, 64*8
Net information data rate (Gbps)		0.18		2.952	4.032	4.968	1.584	1.8
Bandwidth efficiency (MHz/Gbps)[4]	19.5	48.8	36.6	57.6	57.6	28.8	36	50.4
Bandwidth efficiency gain w.r.t. CPRI	1	2.5	1.875	2.95	2.95	1.48	1.85	2.58
Bit efficiency[5]	0.195	0.488	0.366	0.295	0.403	0.248	0.317	0.36
Bit efficiency gain w.r.t. CPRI	1	2.5	1.875	1.51	2.07	1.27	1.63	1.85

[1]CPRI uses one control word per 15 data words of IQ samples [9]. For a fair comparison, there is no control word or line coding (8b/10b or 64b/66b) considered.

[2]CPRI supports sample width from 8 to 20 bits for downstream, and from 4 to 20 bits for upstream. We use the most general case of 15-bit sample width as baseline.

[3]To support 1024QAM, at least 8 bits are needed [20], and the band/bit efficiencies of 8-bit CPRI are identical to the results of [20], excepted that Lloyd algorithm can reduce EVM further by 2–3 dB.

[4]Bandwidth efficiency = LTE bandwidth / fronthaul data rate, which measures the amount of LTE bandwidth that can be delivered by unit fronthaul data traffic.

[5]Bit efficiency = net information data rate / fronthaul data rate, which measures the mapping efficiency between the fronthaul traffic and mobile traffic.

buffer size in each pipeline. If time-interleaving technique is used, the memory usage can be significantly reduced.

VI. DISCUSSIONS

According to CPRI specification [9], a single 20-MHz LTE carrier requires 30.72 MSa/s * 15 bits/Sa * 2 = 921.6 Mb/s fronthaul capacity without considering control word and line coding (8b/10b or 64b/66b). So CPIR can take up to 9.22 Gb/s or 12.9 Gb/s to support 10 or 14 LTE carriers, respectively. In this work, all LTE carriers are encoded by a delta-sigma modulator and transmitted through a 5-Gb/s OOK link, which saves 45.8% or 61.2% data rate compared with CPRI.

Table V lists a comparison in terms of spectral efficiencies of CPRI, CPRI compression, and delta-sigma modulation. Since CPRI has one control word for every 15 data words of IQ samples [9], and uses line coding of 8b/10b or 64b/66b, for a fair composition, no control word or line coding is considered in Table V.

Since CPRI-based solutions have smaller quantization noise and higher SNR than delta-sigma modulation, it will be fair to introduce two measuring metrics, bandwidth efficiency and bit efficiency. Bandwidth efficiency is defined as the ratio between the fronthaul data rate and LTE signal BW, measuring the required fronthaul capacity per unit of BW. Bit efficiency is the radio between fronthaul data rate and the net information rate carried by LTE signals, measuring the mapping efficiency from fronthaul traffic to real mobile traffic.

In this and our previous works [60], [61], delta-sigma modulation shows high BW efficiency, i.e., it only consumes small fronthaul capacity per unit of BW of LTE signals. On the other hand, CPRI-based solutions offer small EVM and high SNR, and therefore can support higher modulation and larger net information rate, so bit efficiency is introduced as a second metric. Although delta-sigma modulation has high bandwidth efficiency, its bit efficiency gain will not be as high as its bandwidth efficiency gain due to the high EVM and low modulations. In Table V, it is assumed that all CPRI-based solutions carry the

TABLE VI
COMPARISON OF VARIOUS LOW LAYER SPLIT (LLS) OPTIONS

3GPP / CPRI cooperation		6/D	7.3/I_D	7.2/II_D, I_U	7.1	8 (CPRI)/E	9
Architecture		Most distributed	More centralized on the right				Most centralized
RRU functions		PHY + RF layers	Low-PHY + RF layers			RF layer	Low-RF layer
RRU complexity		Highest	Medium (higher on the right)			Low	Lowest
		Complete RF layer implemented in analog domain at RRU, including DAC, LO, mixer					Only need PA and BPF
NGFI data		Baseband bits	Scrambled bits	Frequency domain I/Q samples		Time domain I/Q samples	Bits after $\Delta\Sigma$ modulation
Data rate		Lowest	1/10 of CPRI (higher on the right)			Highest	1/4~1/2 of CPRI [60, 61]
Data rate scalability		Traffic dependent Antenna independent, scale with MIMO			Traffic independent Antenna dependent, scale with antenna		
Ethernet compatibility	802.1CM	Future amendament	Class 2			Class 1	Future amendment
	P1914.1	Support	Support			N/A	N/A
	P1914.3	N/A	Structure-agnostic encapsulation Native RoE mapping			Structure-aware encapsulation Native RoE mapping	Structure-agnostic encapsulation
Latency requirement		Lowest	Higher latency requirement on the right				Highest

modulation of 1024-QAM. So far, the best bandwidth efficiency was achieved by delta-sigma modulation [60], [61], which was implemented by offline processing. The highest bit efficiency was achieved by our previous work [18], [19] using statistical compression of CPRI. Fig. 14 illustrates the bandwidth and bit efficiencies of different solutions.

Table VI gives a comparison of various LLS options. Although the proposed option 9 splits at a lower level than option 8, it has improved bandwidth/bit efficiency and reduced fronthaul data traffic than CPRI. Compared with higher level split options 6, 7, and 8, it exploits an all-digital RF transceiver, centralizing high-RF layer at DU, replacing conventional DAC by a low-cost BPF, and eliminating the need of local oscillator and mixer at RRU. It not only makes low-cost, low-power, and small-footprint cell sites possible for small cell deployment, but also paves the road toward SDR and virtualization of DU/RRU for improved compatibility and reconfigurability among multi-RATs. Since option 9 splits deep in the RF layer, it has very stringent latency requirement, which demands highly deterministic latency and makes it suitable for radio coordination applications.

There are several IEEE standards addressing the Ethernet compatibilities of LLS options [66]–[68], shown in Table VI. As a collaborative effort of CPRI cooperation and IEEE 802.1 working group, IEEE 802.1CM specifies time sensitive network (TSN) profiles for fronthaul traffic over Ethernet bridged networks [66], [67]. Currently it supports two function split options, Class 1 for CPRI and Class 2 for eCPRI, and can address other split options, such as option 9, by future amendment. IEEE P1914.1, standard for packet-based fronthaul transport networks, defines the architecture and requirements of Ethernet-based mobile fronthaul traffic [68], including the Ethernet packetization of option 6 and 7. IEEE P1914.3 (previously P1904.3), standard for radio over Ethernet (RoE) encapsulations and mappings, defines 3 encapsulation methods of radio data into Ethernet packets [68], including structure-aware encapsulation, structure-agnostic encapsulation, and native RoE mapping. Structure-aware encapsulation maps CPRI frames to/from Ethernet frames with the help of knowledge of CPRI frame structure. It is optimized for CPRI and allows CPRI to be structurally remapped to RoE. Structure-agnostic encapsulation offers a simple tunneling of radio data stream without knowledge
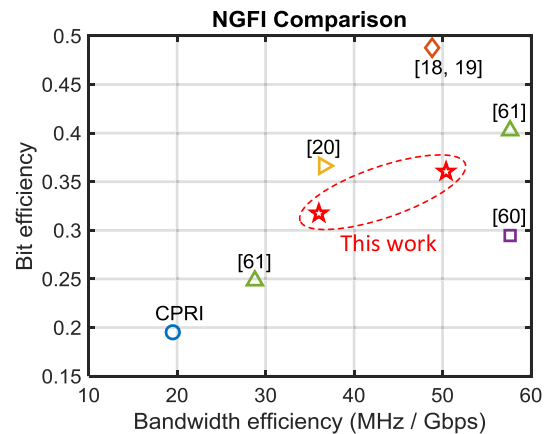

Fig. 14. Comparison of NGFI solutions based on CPRI, CPRI compression, and delta-sigma modulation.

of its frame structure, which is not restricted to CPRI and can support option 9. The third encapsulation method, native RoE mapping maps IQ payload data directly to Ethernet packets, and can support IQ samples from either time domain, such as option 8 (CPRI), or frequency domain, such as eCPRI or option 7.1, 7.2.

One major challenge to all-digital transceiver and SDR is the high processing speed. Delta-sigma modulation requires high oversampling ratio to achieve satisfying SNR/EVM performance. Moreover, digital frequency up-conversion needs a clock rate four times of the carrier frequency. To circumvent the speed limit of existing CMOS or FPGA, several parallel processing techniques have been reported, including polyphase decomposition [44], [45] and look-ahead time-interleaving [47], [48]. In this paper, for a concept-proof experiment, only basic pipeline technique is used. Given the wide frequency range of 5G from sub-1 GHz to millimeter wave, and various scenarios, e.g., eMBB, uRLLC, and mMTC, the proposed option 9 function split is expected to first find its applications in low frequency radio coordinate scenarios, such as low band 5G (T-Mobile 600 MHz). Given its highly deterministic latency, it also has high potential in uRLLC. By leveraging the low-cost, low-power, and small-footprint cell site enabled by all-digital RF transceiver, option 9 split can also be used to support low frequency narrowband IoT (NB-IoT) applications.

VII. Conclusion

In this paper, we propose and demonstrate a new NGFI function split option 9 based on all-digital RF transceiver using delta-sigma modulation. Different from other low layer split options, e.g., 6 (MAC-PHY), 7 (high-low PHY), and 8 (CPRI), the proposed option 9 exploits the design of all-digital RF transceiver and splits functions within the RF layer, with high-RF layer centralized in DU, and low-RF layer left in RRUs. A proof-of-concept all-digital RF transmitter of LTE/5G signals is experimentally demonstrated using real-time bandpass delta-sigma modulation implemented with a Xilinx Virtex-7 FPGA. The delta-sigma modulator works at 5 GSa/s and can encode LTE/5G signals with bandwidth up to 252 MHz and modulation format up to 1024-QAM to a 5Gb/s OOK signal, which is transmitted from DU to RRU over 30-km fiber. To relax the FPGA speed requirement, a 32-pipeline architecture is designed for parallel processing. Four experimental cases are presented to validate the feasibility of proposed option 9, and 5G two-carrier aggregation and LTE 14-carrier aggregation are successfully demonstrated with the EVM performance satisfying the 3GPP requirement. A detailed comparison between CPRI, CPRI compression, and deltas-sigma modulation, in terms of bandwidth and bit efficiencies is also presented.

Although it splits at a lower level than option 8, the proposed option 9 offers improved efficiency than CPRI and reduces the fronthaul data rate requirement. Compared with higher level split option 6, 7 and 8, it exploits a centralized architecture with most RF layer functions consolidated in DU, eliminating DAC, local oscillator and RF mixer at RRU, and enables a low-cost, low-power, small-footprint cell site for small cell deployment. Moreover, given its highly deterministic latency, option 9 is more suitable for radio coordination applications than other higher level split options. All-digital RF transceivers pave the road toward SDR and virtualized DU/RRU for multi-RAT compatibility. Given its deterministic latency, it is expected that the proposed option 9 function split will find applications in low frequency radio coordination scenarios. By exploiting the low cost, low power, and small footprint features of cell sites enabled by all-digital transceiver, option 9 also has high potential in mMTC and NB-IoT applications.

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