Low-Insertion-Loss and Power-Efficient 32 × 32 Silicon Photonics Switch With Extremely High-Δ Silica PLC Connector

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(Post-Deadline Paper)

***Abstract*—We fabricate a 32 × 32 silicon photonics switch on a 300-mm silicon-on-insulator wafer by using our complementary metal-oxide-semiconductor pilot line equipped with an immersion ArF scanner and demonstrate an average fiber-to-fiber insertion loss of 10.8 dB with a standard deviation of 0.54 dB, and on-chip electric power consumption of 1.9 W. The insertion loss and the power consumption are approximately 1/60, and less than 1/4 of our previous results, respectively. These significant improvements are achieved by design and fabrication optimization of waveguides and intersections on the chip, and by employing a novel optical fiber connector based on extremely-high-Δ silica planar-lightwave-circuit (PLC) technology. The minimum crosstalk was −26.6 dB at a wavelength of 1547 nm, and −20-dB crosstalk bandwidth was 3.5 nm. Furthermore, we demonstrate low-crosstalk bandwidth expansion by using output port exchanged element switches. We achieve a −20 dB crosstalk bandwidth of 14.2 nm, which is four-times wider than that of the conventional element switch based 32 × 32 switch.**

***Index Terms*—Optical fiber coupling, optical switches, photonic integrated circuits, silicon photonics, strictly-non-blocking switches.**

I. Introduction

THERE has been strong demand for multi-port optical switches for use in telecom and datacom network systems to deal efficiently with massive data flow [1]. Requirements for such optical switches include several hundred switching ports, strictly-non-blocking switching, fast switching speed, compact size, and low-cost. To meet these requirements, one promising platform is silicon photonics. The silicon photonics platform is based on the complementary metal-oxide-semiconductor (CMOS) process that enables densely integrated and very uniform optical devices, and mass-production resulting in low-cost. Silicon photonics switches based on various topologies have been demonstrated by several groups, including path-independent insertion loss (PILOSS) [2], [3], switch and select [4], [5], phased array [6], and MEMS-actuated cross point [7]. Among these topologies, the PILOSS topology remains a promising candidate for large port-count switches from the viewpoint of insertion loss, power consumption, and available electrical packaging technology.

Previously, we fabricated a 32 × 32 PILOSS switch using our CMOS pilot line, and developed its packaging and control technologies based on a land-grid-array (LGA) interposer and a pulse-width modulation scheme, respectively [8]. We demonstrated full operation of the 32 × 32 switch with the transmission of all ($32^2 = 1{,}024$) paths, and the feasibility of large port-count silicon photonics switches. However, the average fiber-to-fiber insertion loss was 28.4 dB, which consisted of 14.5-dB on-chip loss and 13.9-dB coupling loss. These losses remained important issues. Recently, we have found that the loss and electric power consumption on the chip can be significantly reduced by optimizing the device design and fabrication process, and demonstrated an ultralow-loss 8 × 8 switch [9]. As for the coupling loss, we have developed an optical fiber connector based on extremely-high-Δ (5.5%) silica planar-lightwave-circuit (PLC) technology [10], of which the mode field diameter is matched to those of the silicon edge couplers and high-Δ fibers fusion-spliced to standard single mode fibers. With the connector, we have demonstrated a 32-port connection with a uniform coupling loss of 1.4 to 1.6 dB/facet. The performance improvement of the 32 × 32 switch is expected by adopting the two technologies.

In this paper, we report on a high performance 32 × 32 PILOSS switch that exhibits a minimum insertion loss of 8.9 dB and on-chip electric power consumption of 1.9 W [11]. These values are approximately 1/60 and 1/4 of the previous results [8]. Moreover, we show a new result for another 32 × 32 switch that utilizes output-port-exchanged Mach-Zehnder (MZ) element switches. The 32 × 32 switch exhibits four-times broader operating bandwidth than that of the conventional MZ-switch-based 32 × 32 switch.

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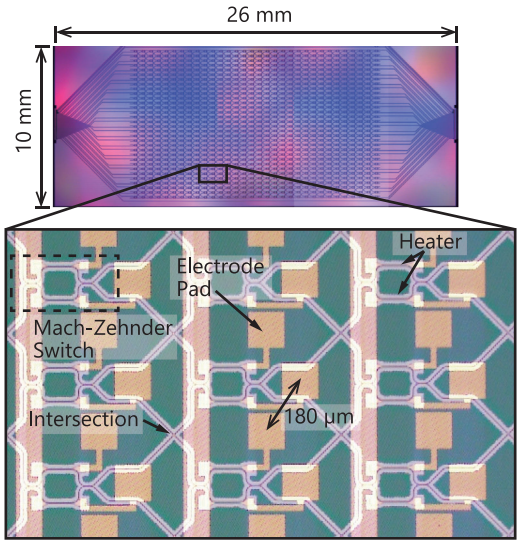

Fig. 1. Microscope image of fabricated 32 × 32 switch chip. We used gold as electrode material instead of a standard material (Al-Cu) due to a machine issue. Thus, the electrode was not formed in the CMOS pilot line. However, it makes no difference to the switch performance.

II. Fabricated 32 × 32 Switch

The silicon photonic circuits and thermo-optic phase-shifters were fabricated on a 300-mm silicon-on-insulator (SOI) wafer (top silicon thickness is 225 nm, buried oxide thickness is 3 μm) using our CMOS pilot line equipped with an immersion ArF scanner.

Fig. 1 shows the fabricated 10 mm × 26 mm switch chip. The silicon waveguides were buried with a 1.5-μm thick SiO_2 over-cladding layer on which TiN thin film heaters as thermo-optic phase shifters were fabricated. The inversely tapered edge couplers with edge width of 175 nm reduced from 430 nm were aligned with a 50-μm pitch on each side, and connected to the switch matrix with routing waveguides. The switch matrix was arranged in the PILOSS topology [12], which consists of an $N \times N$ array of 2 × 2 element switches with intersections in-between. For $N = 32$, there are 1024 element switches and 961 intersections. The element switch was the MZ switch with a thermo-optic phase shifter (5-μm wide, 70-μm long) on each arm and directional couplers as the 3-dB coupler. The intersection was an adiabatic intersection [13]. All the silicon photonic components were designed for the transverse-electric (TE)-like mode. After the wafer fabrication and dicing, the 300-nm-thick gold electrode was patterned by a lift-off method using photolithography and *e*-beam evaporation. The minimum pitch of the electrode pads was 180 μm.

The fabricated switch chip was packaged by using a ceramic interposer with a 2112-pin 0.5-mm-pitch LGA [8], and the extremely-high-Δ PLC fiber connector [10], as shown in Fig. 2. First, the ceramic interposer was flip-chip bonded to the Si switch chip using Au bumps and a non-conductive paste. Then, the PLC connector connected to 48 single mode fibers was butt-coupled to the Si waveguides and bonded to the Si chip with a refractive-index-matched UV-cured glue, as shown in Fig. 3. In the PLC connector, single mode fibers were connected to high-Δ fibers by the thermally-expanded core technique. Then, the high-Δ fibers were bonded to the extremely-high-Δ PLC chip. Thanks to the compact size of the PLC chip, the PLC connector is handled like a conventional fiber array. The mode field diameter of the PLC waveguide was about 3 μm, for which the Si edge coupler was designed. With this optical coupling method, it is possible to integrate high-performance components on the PLC chip as well as to reduce the coupling loss. As a simple example, waveguide pitch conversion from 127 μm to 50 μm was implemented on this PLC chip.

The optically and electrically packaged 32 × 32 switch was mounted on a printed circuit board (PCB) with control electronics. Fig. 4 shows the switch inserted into an LGA socket on the

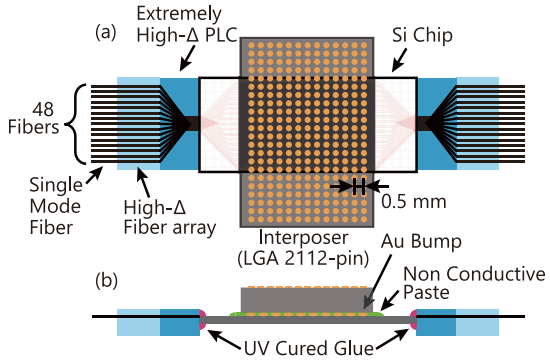

Fig. 2. Schematic of electrical and optical packaging. (a) Top view. (b) Cross sectional view.

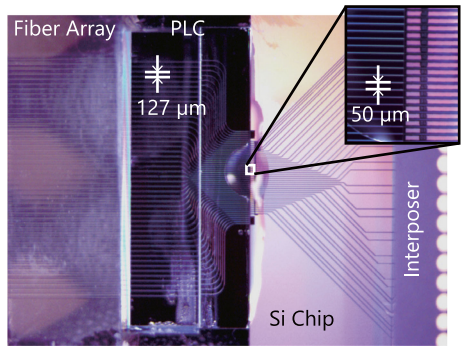

Fig. 3. Microscope image of optical coupling part.

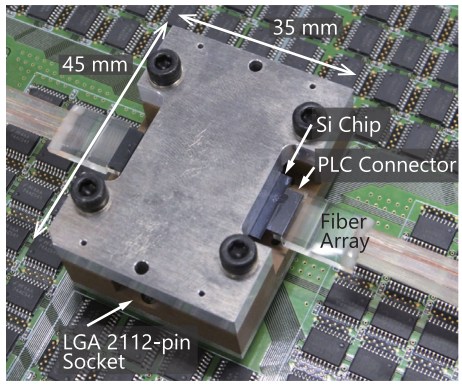

Fig. 4. Si switch chip mounted on printed circuit board with control electronic circuit.

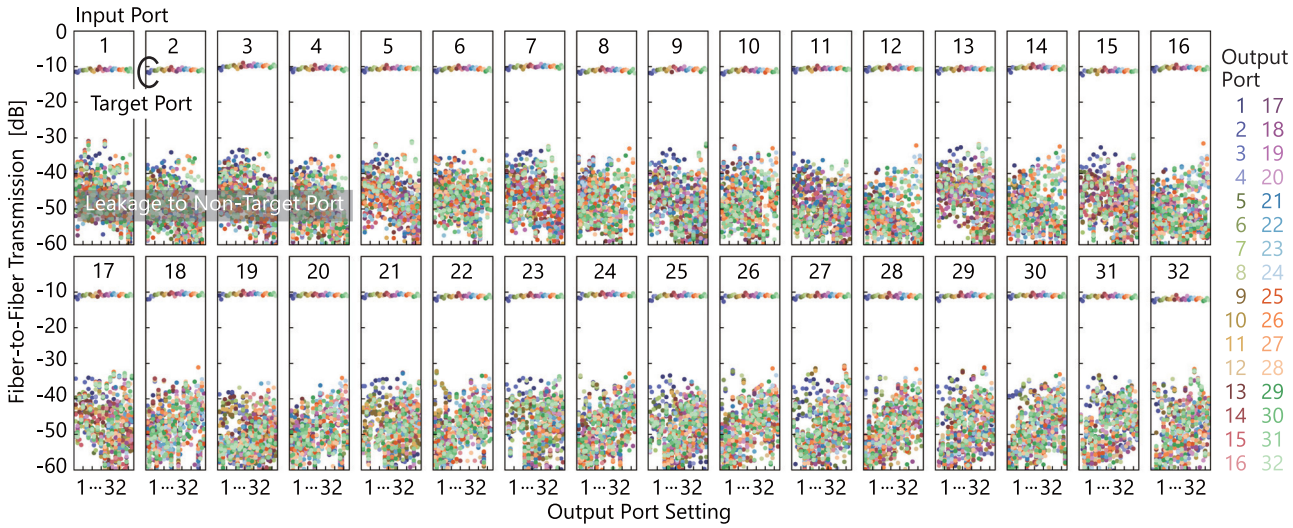

Fig. 5. Fiber-to-fiber insertion losses of all target ports ($32 \times 32 = 1{,}024$ paths) and leakages to non-target output ports at wavelength of 1547 nm. There are $32 \times 32 + 32 \times 32 \times 31 = 32{,}768$ data points.

PCB. We confirmed that all the element switches were operable. The average and the standard deviation of electric resistance of the heaters were 395 Ω and 11.2 Ω, respectively. As the control electronics, five field programmable gate arrays (FPGAs) and buffer ICs were assembled on the 220 mm × 235 mm PCB. The FPGA generates a rectangular pulse sequence (5 V amplitude, 1 MHz repetition), whose duty cycle is tunable to adjust applied power to the heater. The response speed of the heater is ∼30 kHz, which is sufficiently slower than the pulse repetition frequency. Phase errors between the two arms of all MZ switches caused by tiny fabrication errors were compensated by individual trimming currents. The optimum trimming current was automatically determined by a calibration algorithm [14].

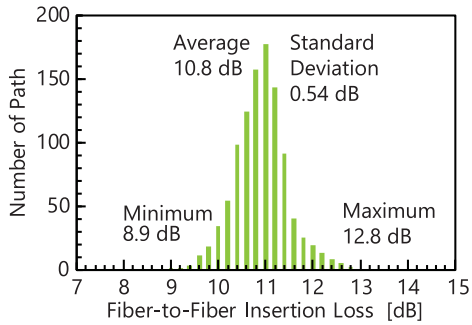

Fig. 6. Distribution of fiber-to-fiber insertion losses of all paths at wavelength of 1547 nm.

III. Experimental Results and Discussion

A. Fiber-to-Fiber Insertion Loss

Fiber-to-fiber insertion losses of all paths and leakages to non-target ports were evaluated by using a tunable laser diode (TLD) and four eight-channel optical power meters. CW light from the TLD was adjusted to TE-like polarization with a polarization controller, then launched to the switch chip through the PLC fiber connector. The input optical power to the PLC connector was 0 dBm, and its wavelength was tuned to 1547 nm, at which the crosstalk becomes the lowest as described in the next section. The output light from the switch propagated through another PLC fiber connector, then entered the optical power meters.

Fig. 5 presents the measured fiber-to-fiber insertion losses of all ($32^2 = 1{,}024$) paths and the leakages ($32^2 \times 31 = 31{,}744$). It is should be noted that the variation of the insertion losses is very small, thanks to the PILOSS topology. The residual insertion loss variation is attributed to the two reasons. One is propagation length differences among the routing waveguides between the edge couplers and the switch matrix. The propagation loss difference between the maximum route and the minimum route was estimated to be 0.4 dB. The other is the coupling loss variation at the input side because it is observed in Fig. 5 that the insertion loss depends on the input ports, rather than the output ports. We suspect that there are misalignments between the high-Δ fibers and the PLC waveguides, or unclean facets of the high-Δ fibers, the PLC, or the Si chip. The leakages were less than −30 dB, which can be improved by optimizing the calibration algorithm because manual calibration could reduce the leakages.

Fig. 6 presents the distribution of the fiber-to-fiber insertion losses. The minimum, the maximum, and the average losses were 8.9 dB, 12.8 dB, and 10.8 dB, respectively. The standard deviation was 0.54 dB. By comparing with a previous average loss of 28.4 dB [8], the insertion loss was improved by 17.6 dB (∼1/60). The breakdown of the minimum insertion loss is summarized in Table I. The on-chip loss, which is the insertion loss without the fiber-to-chip coupling loss, was 6.1 dB. The propagation loss per Si waveguide length and the propagation length on the switch chip were 1.2 dB/cm and longer than 2.6 cm, respectively. Therefore, the propagation loss on the chip was estimated to be at least 3.1 dB. By adopting the latest fabrication process, in which the propagation loss is less than 0.5 dB/cm [15], the on-chip loss could be reduced by ∼1.8 dB. As for the

TABLE I
BREAKDOWN OF MINIMUM FIBER-TO-FIBER INSERTION LOSS

Component	Loss [dB]	
SMF/Si	1.4	
Routing WG	0.70	
MZ Switches	4.0	On chip 6.1 dB
Intersections	0.74	
Routing WG	0.63	
Si/SMF	1.4	
Fiber-to-Fiber	8.9	

SMF: Single mode fiber, WG: Waveguide, MZ: Mach-Zehnder

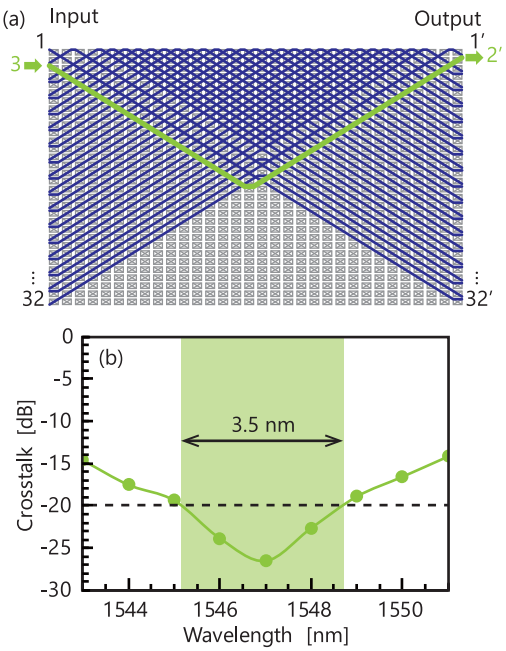

Fig. 7. (a) One of the worst crosstalk paths (input 3 → output 2'). Connection: input 1 → output 32', 2 → 30', 3 → 2', 4 → 28', 5 → 27', . . . , 29 → 3', 30 → 29', 31 → 1', 32 → 31'. (b) Measured wavelength dependence of crosstalk.

fiber-to-chip coupling loss, we assumed the minimum coupling loss of the current PLC connector to be 1.4 dB/facet. However, it is possible to further improve it to less than 1 dB/facet, or by ∼0.8 dB, as numerically indicated in [10]. With these improvement, we could achieve a fiber-to-fiber insertion loss of 6.3 dB.

B. Crosstalk in One of Worst Cases

Because the 32 × 32 switch has 32! ≈ 2.63 × 10^{35} switch states, the crosstalk evaluation of all the switch states would take too long. Therefore, we evaluated one of the worst crosstalk switch states shown in Fig. 7(a). In the switch state, the path from input port 3 to output port 2' is the worst crosstalk path in which there are 29-, and 30-time crossings with other paths in the MZ switches and the intersections, respectively. The crosstalk was defined as the output power of the path 3 → 2' divided by the sum of the leaked power from other paths to output port 2'.

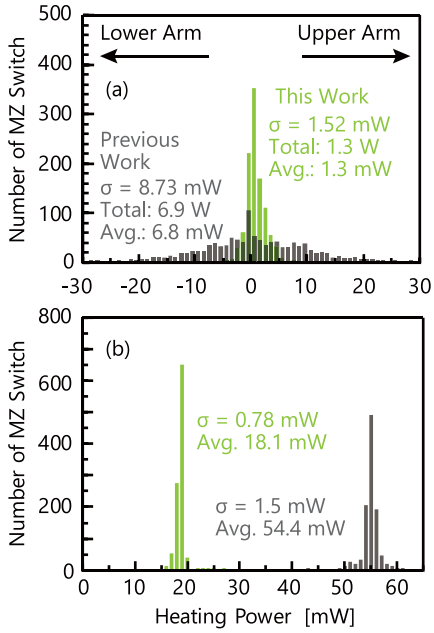

Fig. 8. Electric power distribution on switch chip. Previous work is ref. [8]. (a) Trimming power for initial phase errors between two arms of element Mach-Zehnder switches. The positive (negative) value in the horizontal axis means the heating power of the upper (lower) side heater of the Mach-Zehnder switch. (b) Switching power from cross state to bar state.

The experimental setup is the same as that of the insertion loss measurement, and the TLD wavelength was changed from 1543 to 1551 nm. Fig. 7(b) presents the measured wavelength dependence of the crosstalk. The minimum crosstalk was −26.6 dB at a wavelength of 1547 nm. For −20-dB crosstalk, its bandwidth was 3.5 nm. These values are almost the same as those of the previous work [8], and indicate that fabrication accuracy of our fabrication process is enough for the devices designed for the TE-like mode which require more precise waveguide width control than those designed for the transverse-magnetic (TM) -like mode. The expansion of the −20-dB crosstalk bandwidth will be discussed in section D.

C. Electric Power Consumption on Chip

The electric power consumed on the switch chip was for trimming the initial phase error between the two arms of the MZ switches and also for changing the switch state from the cross state to the bar state. Especially, the trimming power is important for the large port-count PILOSS switch because $N \times (N-1)$ switches are the cross-state consuming the trimming power and only N switches are the bar state consuming the switching power for an $N \times N$ switch in operation. For example, in the 32 × 32 switch, 32 × 31 = 992 switches are the cross-state and 32 switches are the bar state. Therefore, the trimming power occupies a large part of the total electric power consumption on the chip.

Fig. 8(a) shows the distribution of the trimming power. The total trimming power (i.e., the sum of all the trimming powers of each element switch) was 1.3 W, its standard deviation

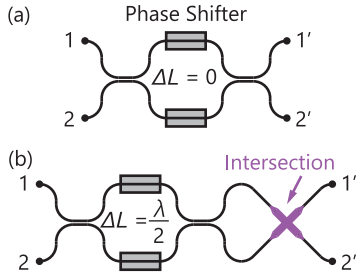

Fig. 9. (a) Conventional Mach-Zehnder element switch. (b) Output port exchanged Mach-Zehnder element switch. ΔL: arm length difference. λ: wavelength.

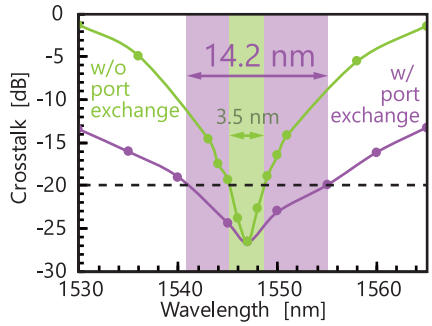

Fig. 10. Measured crosstalk spectra of 32 × 32 switch in one of worst cases. The switch state is the same as that shown in Fig. 7(a).

was 1.52 mW, and average trimming power (i.e., an average of the absolute trimming powers) was 1.3 mW. These values are less than one-quarter of those of the previous result [8], and were achieved by improved thermal efficiency owing to operating polarization change from the TM-mode to the TE-mode, and reduced phase error owing to arm length shortened from 100 μm to 70 μm. Fig. 8(b) presents the distribution of the switching power from the cross state to the bar state. The average switching power was 18.1 mW, and the standard deviation was 0.78 mW. These values are one-third of those of the previous work. Based on the above results, we estimated the total electric power consumption in full-operation where 992 switches are the cross-state, and 32 switches are the bar-state, as 1.9 W (1.3 W for trimming, 0.6 (= 0.018 × 32) W for switching). On the other hand, that of the previous work was 8.7 W (6.9 W for trimming, 1.8 W for switching). This reduction was mainly achieved by improvement of the efficiency of the thermo-optic effect in the waveguide mode. We changed the operating polarization from the TM-like mode to the TE-like mode, which resulted in the efficiency becoming approximately twice as good owing to the tighter optical confinement to the silicon waveguide core in the TE-like mode.

D. 32 × 32 Switch Based on Output Port Exchanged Element Switches

To expand the low crosstalk bandwidth, we fabricated another 32 × 32 switch with modified element MZ switches. Fig. 9 illustrates the structure of the modified MZ switch, in which another adiabatic intersection was added to exchange the two output ports of the MZ switch. This output port exchange improves the low crosstalk bandwidth [16]. Based on coupled-mode theory, the optical leak to the cross port (when the input port is 1 (2), the cross port is 2' (1') in Fig. 9(a)) at the bar-state becomes completely extinct if the splitting ratios of the two directional couplers are the same, despite they are not equal to 3-dB [17]. This means that the wavelength dependence of the directional couplers does not affect the optical leak to the cross port. Therefore, the wavelength dependence of the leakage to the cross-port at the bar-state depends only on the wavelength dependence of the phase-shifter, of which slope against the wavelength is more moderate than that of directional couplers, resulting in a wider low-crosstalk bandwidth. On the other hand, the leakage to the bar port (when the input port is 1 (2), the bar port is 1' (2') in Fig. 9(a)) at the cross-state becomes completely extinct if the splitting ratio is exactly 3-dB or complementary (e.g., 60:40 (front), 40:60 (rear)) [17]. This means that the leakage to the bar port becomes the minimum only around the designed wavelength, resulting in a narrower low-crosstalk bandwidth. This output port exchange is effective for the PILOSS and the crosspoint topologies [16].

The output port exchanged MZ switch has asymmetric arms with a half wavelength (i.e., the MZ switch itself is in the bar-state without thermo-optic phase shift). By adding the intersection to each element switch, the number of the intersections on a path increases by 32. Therefore, it is estimated that the on-chip loss increases by 0.77 dB (0.024 dB/intersection × 32). The switch chip fabrication and electrical packaging are the same as those presented in Section II. For the optical packaging, we used a 127-μm-pitch high-Δ fiber array, rather than the extremely high-Δ PLC connector. The electric power consumption in full operation was almost the same as that of the conventional switch.

Fig. 10 compares measured crosstalk spectrum of the 32 × 32 switch based on the output port exchanged MZ switches with that based on the conventional MZ switches. The bandwidth for −20-dB crosstalk was expanded by four times (from 3.5 nm to 14.2 nm). The minimum crosstalk at a wavelength of 1547 nm was −26.6 dB for both switches. We suppose that two factors govern the bottom of the crosstalk spectra. One is the leakage accumulation due to the imperfect cross-state switches, which can be reduced by improving the calibration algorithm. The other is the residual TM-like mode component of the input light, which can reach the output ports through the switch matrix designed for the TE-like mode. Inserting a polarization cleaner into each port is effective for suppressing the residual TM-like mode.

IV. Conclusion

We fabricated the 32 × 32 PILOSS Si switch in combination with the extremely-high-Δ PLC fiber connector and demonstrated a significant reduction of loss and electric power consumption on the chip. The average fiber-to-fiber insertion loss was 10.8 dB and the standard deviation was 0.54 dB. The total

electric power consumption on-chip in full operation was 1.9 W. These results indicate that this multi-port optical switch based on silicon photonics is a promising candidate for use in high capacity and energy efficient future telecom and datacom network systems. Polarization independence and broad operating bandwidth remain important issues. For the polarization independence, a polarization diversity scheme is a realistic option as demonstrated in [18], because polarization independent structures require severe fabrication tolerance [19]. For expansion of the operating bandwidth, a double-MZ switch is one of the good options [9]. In the double-MZ switch configuration, the number of the intersection on a path becomes twice, and one MZ switch is added on a path. The additional loss comes from these devices is estimated to be less than 1 dB.

We believe that an insertion loss of about 6 dB, which is comparable to 32 × 32 switch made of the silica PLC platform [20], is possible because there are some rooms for loss reduction in the propagation loss of the Si waveguides and the coupling loss of the extremely high-Δ PLC connector.

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