Low-Crosstalk Simultaneous 16-Channel × 25 Gb/s Operation of High-Density Silicon Photonics Optical Transceiver

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(Highly-Scored Paper)

***Abstract*—We successfully developed a high-density broadband 16-channel × 25 Gb/s on-package silicon photonics optical transceiver. The flip chip bonded bridge structure realized high density of about 363 Gb/s/cm^2. We demonstrated simultaneously on all 16 channels error-free operations with low crosstalk penalties of Tx-to-Tx 1.4 dB, Rx-to-Rx 1.4 dB, and Tx-to-Rx <0.1 dB.**

***Index Terms*—Crosstalk, electric integrated circuit, flip chip bonding, package substrate, penalty, photonic integrated circuit, power integrity, receiver, signal integrity, silicon photonics, transceiver, transmitter.**

I. Introduction

INTERCONNECT bandwidths are increasing exponentially in high-performance computing systems and servers [1]–[3]. Furthermore, bandwidths are expected to reach over a few Tb/s per node in the near future. Until now, optical interconnect has been adopted for interconnections between system boards in light of the merits of broad bandwidth and low power transmission compared with electrical interconnects. In order to realize bandwidths of over a few Tb/s per node, development of further broadband, and lower power and higher density optical interconnect technologies will be required. In particular, the realization of an optical transceiver (TRx) to satisfy the demands above described is one of the critical issues.

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As a structure of the next generation optical TRx, on-package (PKG)-type is thought to be promising. The TRx is placed near a large scale integration (LSI) and is co-mounted on a PKG substrate. This is because it is advantageous to overcome the limit of the number of pins on the backside of a PKG substrate [4] and to reduce the consumption of power in order to compensate for the distorted electrical signals such as equalizers by shortening the electrical wiring lengths between the LSI and the TRx. To place several TRxs adjacent to the LSI chip on a limited area of a PKG substrate, a small footprint is an important issue. For realizing such a broadband capability and high-density TRx, silicon photonics technology is suitable. This is because the TRx optical elements are able to be integrated in a photonic integrated circuit (PIC). Furthermore, a PIC, which is made of a silicon substrate, can be assembled on a PKG substrate using conventional electric packaging technologies.

Taking all this into consideration, we have developed an on-PKG-type silicon photonics optical TRx with a "high-density bridge structure." We demonstrated the bridge-assembled 25 Gb/s silicon photonics transmitter (Tx) and receiver (Rx) with single-ch operation [5]. Recently, we demonstrated simultaneous 12-ch × 25 Gb/s operation with low crosstalk penalty using a prototype of multi-ch silicon photonics Rx [6]. As a next step, we worked on the development of an aggregate 400 Gb/s broadband and high-density optical TRx for realizing the broadband interconnect. To add 16-ch Tx lanes to develop the receiver, the TRx also requires the performance of low crosstalk penalties of Tx-to-Tx, Tx-to-Rx. In this paper, we report on the designs and the performances of a prototype of high-density bridge-assembled broadband 16-ch × 25 Gb/s on-PKG silicon photonics TRx [7].

II. Designs and Fabrication of Prototype TRX

Fig. 1 shows a schematic of the structure of the TRx. To realize the multichannel operation, the signal lines and the power lines have to be carefully designed. We employed a high-density bridge structure [7]. In the structure, an electric integrated circuit (EIC) die and a PIC die were flip chip bonded directly by solder bumps. This enabled us to minimize the wiring length and

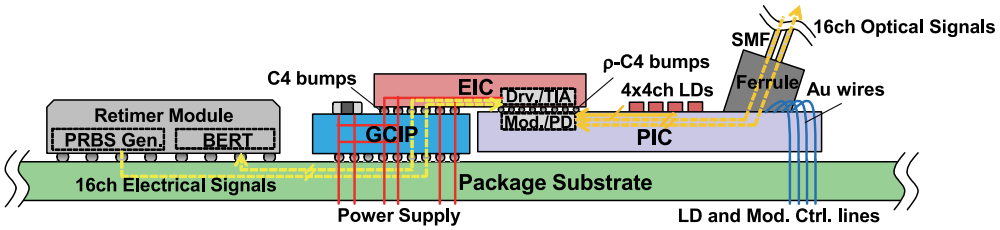

Fig. 1. A schematic structure of 16-ch × 25 Gb/s silicon photonics optical TRx on package substrate. We employed a high-density bridge assembly. Here, the EIC and PIC are bonded by solder bumps and they are mounted on a glass ceramic interposer (GCIP).

the parasitic capacitance between the electronic and photonic circuits, and to mitigate the degradation of the electrical signals between the transimpedance amplifiers (TIAs) and photo detectors (PDs), the drivers and modulators, respectively. We also employed a high-density glass ceramic interposer (GCIP) to support the bonded chips on a flat surface of a PKG substrate. The GCIP can accommodate many signal and power lines without many bonding wires connecting the PIC with the PKG substrate. Laser-diode arrays (LDs) were mounted as light sources for Tx and processed multifiber ferrules as optical I/O were fixed on the PIC. Retimer modules were co-mounted on a PKG substrate. The retimer modules functioned as pseudo random bit sequence (PRBS) generators and bit error rate testers (BERTs) to demonstrate simultaneous 16-ch Tx and Rx operation.

As measures for suppressing crosstalk penalties, we designed the signal lines and the power lines as described below. At first, to reduce the reflections and crosstalk interference in the signal lines, we designed 100 Ω differential signal lines even on the EIC and 100 Ω signal vias inside the GCIP. The patterns of signal vias, ground vias, and planes in the GCIP were laid out properly to satisfy the characteristic impedance of 100 Ω. Hence, the transmission signal lines of 100 Ω differential signal lines between the retimer modules and TRx elements on the EIC were designed. Next, in order to reduce the simultaneous switching noise (SSN) in the power lines, we ensured the impedance of the power lines for Tx and Rx were lower than target impedances. We set the target impedance for Tx and Rx to 50 mΩ and 80 mΩ, respectively. Here, we considered the fluctuation ratio of the power at the EIC. In the design, we put capacitors on the GCIP in order to reduce the L-C resonant peaks at 100–200 MHz in the frequency characteristic for the power lines. Furthermore, we laid out 60 nF and 35 nF on-chip-capacitors adjacent to the Tx and the Rx power lines on the EIC, respectively. Finally, we obtained low impedance power lines for Tx and Rx. Then, in order to ensure the Tx power noise did not affect the Rx sensitivity, the power lines for the Tx and the Rx were perfectly separated from the PKG substrate.

Photographs of the prepared EIC and PIC are shown in Fig. 2(a) and (b). The EIC was fabricated using 28 nm CMOS technology. The configuration of all the 16-ch elements for the TRx and the number of the channels are described on the photo.

As for the Tx elements, we assembled four 4-ch LDs emitting at a wavelength of 1540 nm on the PIC. We formed pedestals and an Au-Sn electrode on the PIC by foundry processes. Using the pedestals and the electrode, LDs could be assembled passively on the edges of spot size converter structured waveguides in the PIC with high coupling efficiency. After assembling, the LDs

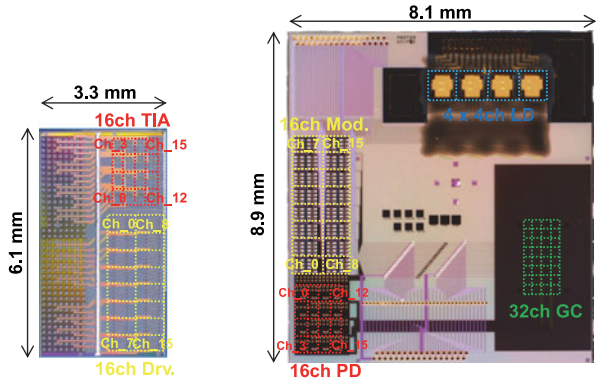

Fig. 2. Photographs of (a) EIC and (b) PIC of the high-density 16-ch optical TRx. Tx and Rx elements were highly integrated in the chips. Four 4-ch LDs were assembled and 32-ch GCs were formed in the PIC.

were covered with transparent gel and encapsulation resin. Here, the black encapsulation resin functions not only as protection of the inside gel but also to prevent stray light entering other areas in the PIC [8], [9].

The drivers amplified high-speed 25 Gb/s differential signals and divided the signals into four segments with delay control. Delays between segments could be controlled by the current settings. Here, the driving voltages for the driver circuits and the bias for the modulators were both 1.0 V. We also employed push-pull type Mach–Zehnder interferometer (MZI) modulators with p-n junctions. The modulator arms have four divided electrodes. Then, we generated large-amplitude driving signals like differential signals with a voltage of 2.0 Vp-p by pairing one outputted differential driving signal, which is biased, with one of the other signals. The large-amplitude signals generated were applied to the p-n junctions in the modulators. This meant the large-amplitude Vp-p enabled the folded arm's lengths to be shortened, thus enabling us to realize high-density modulators. The control lines of the LDs' current and the phase shifter of the modulator were directly connected between the PIC and the PKG by bonding wires, as shown in Fig. 3(b). As for the receiver (Rx) elements, the designs of the TIA with inductor circuit were based on previous reports [9]. The driving voltages for Rx and the bias voltage for the PDs were 0.9 V and −2.0 V, respectively. Here, p-i-n-type germanium waveguide PDs were employed. The PDs show a responsibility of 0.75 A/W at a wavelength of 1550 nm [6].

The modulators and PDs were optically connected to an array of grating couplers (GCs) by waveguides. This resulted in an ar-

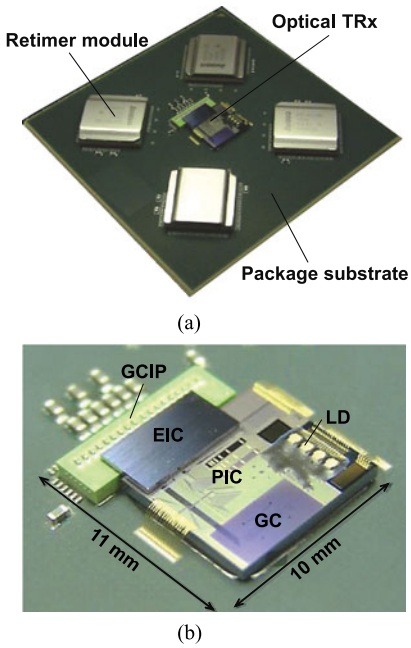

Fig. 3. Photographs of (a) perspective view, and (b) magnified view of a developed optical TRx. High-density bridge structures assembled on-PKG optical TRx were realized.

ray of 32-ch GCs for 16-ch Tx and 16-ch Rx being formed on the PIC. As the GC type for Tx and Rx, we employed one-dimensional and two-dimensional polarization diversity, respectively. Loopback GCs for assembling the multifiber ferrule by an active alignment were also formed at both sides of the GC array.

Fig. 3(a) and (b) show photographs of the assembled TRx on a PKG substrate. At first, we bonded the EIC and the PIC by a flip chip bonding. After the bonded area was covered with underfill resin, the bonded chips were mounted on a GCIP on a PKG substrate. We confirmed the bump connectivity by directly observing a cross-section of the bridge structure. The control lines were connected by bonding wires. The footprint of the TRx is only 10 mm $\times$ 11 mm. Therefore, we realized broadband and a high-density structure with 363 Gb/s/cm^2. Then, we attached the optical single mode multifiber ferrule to the GC array by using an active alignment method and fixed it using an ultraviolet cure epoxy adhesive. Some thermal interface materials (TIM), a lid and cooling units were also attached on the TRx. Finally, we set the TRx on PKG substrate to an evaluation board by a land grid array. Using the evaluation board, we fed power and controlled the various settings for the TRx and the retimer modules.

III. Performance of Multichannel Operation

The typical optical eye diagrams for 25 Gb/s non-return zero (NRZ) signal with PRBS 2^7-1 at single-ch operation and at 16-ch operation for a Tx channel are shown in Fig. 4(a) and (b), respectively. The eye diagram at 16-ch operations is slightly deteriorated compared with the eye diagram at single-ch operation. Even so, the eye diagram shows clear eye opening. The extinction ratios for single-ch and 16-ch operation are 6.9 dB and 5.5 dB, respectively. Furthermore, the jitter$_{\mathrm{p-p}}$ for

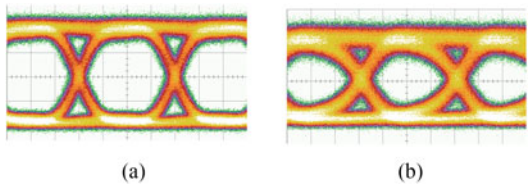

Fig. 4. Optical eye diagrams of Tx channels (a) at single-ch operation and (b) simultaneously at all 16-ch operations. While the eye diagram shows slight deterioration, it shows clear eye opening.

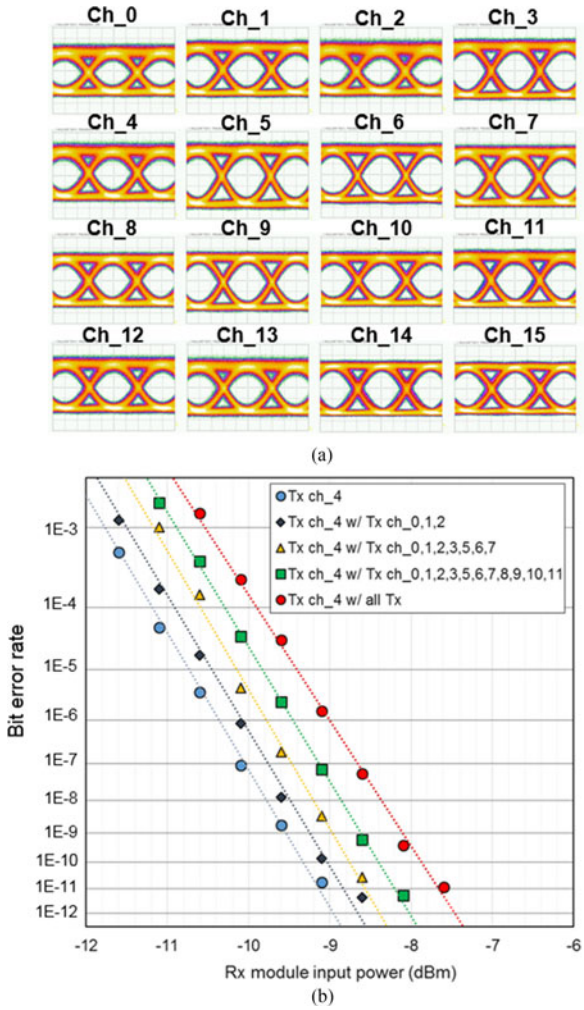

Fig. 5. (a) Optical eye diagrams of Tx channels and (b) the sensitivity changes of ch_4 at multichannel Tx operations. The total Tx-to-Tx crosstalk penalty was found to be 1.4 dB.

single-ch and 16-ch operations shows 10.7 ps and 15.6 ps, respectively. We felt the effect of IR drops and residual SSN in power lines at all 16-ch Tx operations simultaneously may have been the cause. Eye diagrams of all Tx channels are shown in Fig. 5. All channels show clear eye openings without any failed channels.

Then, we investigated the Tx inter-channel crosstalk penalty by measuring the sensitivity using a commercially available Rx module and a BERT. We selected ch_4 as a victim channel and investigated the effect of a crosstalk penalty from the other aggressor Tx channels. Fig. 5(b) indicates the sensitivities of ch_4 when the number of other Tx channels is increased. Error-free

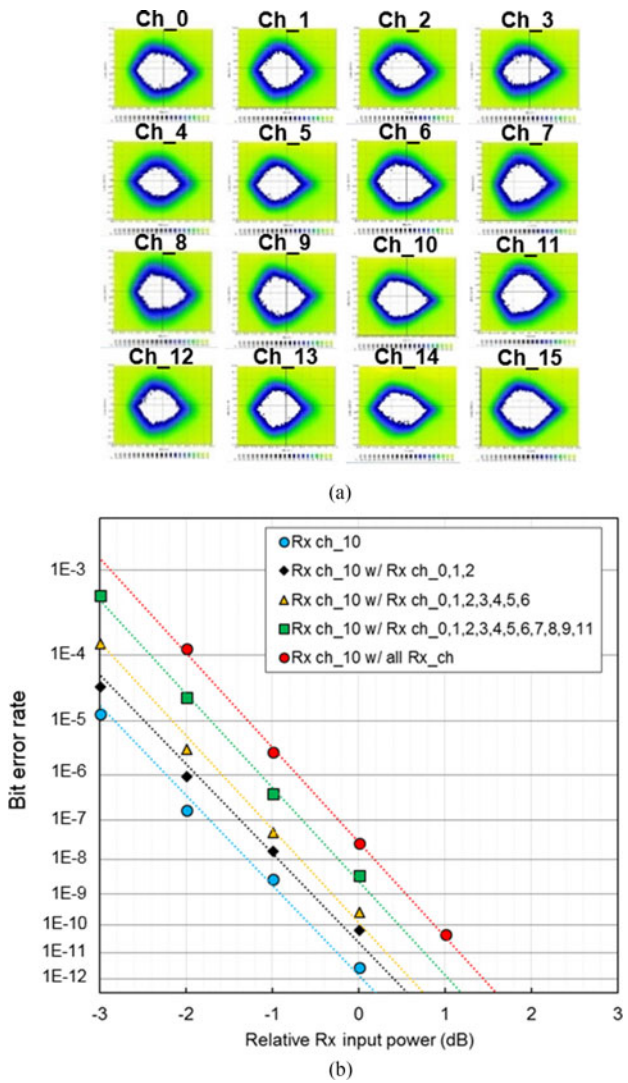

Fig. 6. (a) BER eyes of each channel at simultaneous 16-ch operations, (b) BER characteristics of Rx multichannel operations. The total Rx-to-Rx crosstalk penalty was found to be 1.4 dB.

(bit error rate, BER $< 10^{-12}$) operation was successfully confirmed even when all the channels were driven. The total penalty at 16-ch × 25 Gb/s driving was measured to be 1.4 dB. This value is thought to be small when the high-density assembled configuration is considered.

Next, we examined the Rx performance. A $LiNbO_3$ modulator driven by a pulse pattern generator and a laser light source with a wavelength of 1540 nm generated a 25 Gb/s NRZ signal with PRBS $2^{31}-1$ patterns. Using the signal, we confirmed a minimum receiving sensitivity of −9.8 dBm at the PD input power in single-ch operation. Then, we launched the signal to all channels at a power level of −6.0 dBm using a splitter, an erbium-doped fiber amplifier (EDFA) and an attenuator. The BER eyes of Rx under simultaneous 16-ch operation, which were measured with the retimer's function, are shown in Fig. 6(a). Here, the horizontal and vertical axis indicates the unit interval and amplitude, respectively. The white area indicates the BER $<10^{-6}$ regions. All channels show clear eye

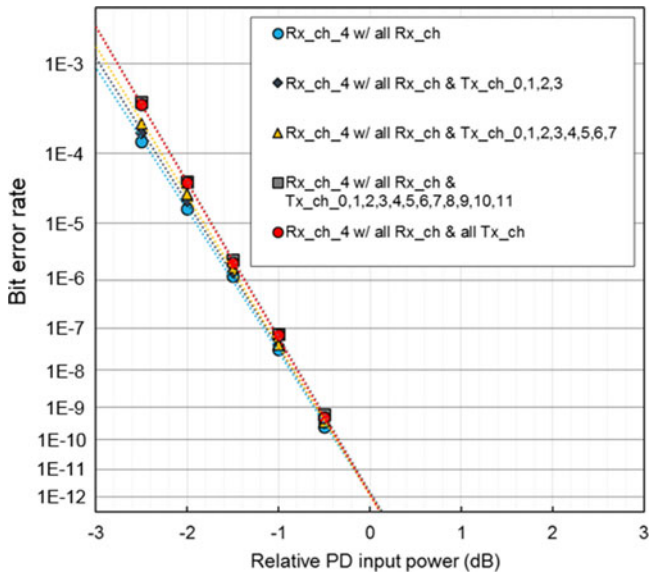

Fig. 7. Behavior of Rx ch_4 sensitivity when increasing the number of Tx driving channels. The crosstalk penalty from Tx aggressors has little influence on Rx operation even in the nearest channel to the Tx elements array.

openings, and error-free (BER $<10^{-12}$) operations were also confirmed using error counters.

To estimate the inter-channel crosstalk penalty for Rx, we investigated the BER characteristics of ch_10 while changing the number of other Rx channels. The result is shown in Fig. 6(b). The horizontal axis indicates the relative Rx input power, which is normalized by the minimum receiving sensitivity in single-ch operation. The sensitivity was seen to be marginally degraded and the crosstalk penalty was estimated to be 1.4 dB when all channels were operated. The estimated value per channel is almost the same as the smallest in the recent reports on 25 Gb/s receivers [11], [12].

Then, we investigated the crosstalk property of Tx-to-Rx. We set Rx_ch_4 as the victim channel because this channel is located nearest to the Tx channels in the Rx array. We measured the sensitivity of ch_4 with all Rx channels operating and as a function of the number of Tx driving channels. Here, the horizontal axis indicates the relative Rx input power, which is normalized by the minimum receiving sensitivity under Rx all-16-ch operation. The result is shown in Fig. 7. Almost no change was observed even with all Tx channels operating. We attribute this negligible crosstalk penalty between Tx and Rx to the careful design of the isolated Tx and Rx power lines from the PKG substrate to the EIC.

Furthermore, we note the power consumption of the developed TRx circuit. The measured total power for the Tx circuit including the driver and the modulator is 1995 mW. This value does not include the power required for the LD. The total power for the Rx circuit including the TIA and PD is 367 mW. Here, the power for the driver and TIA was dominant. As a consequence, the operation power efficiencies are 4.99 mW/Gb/s and 0.92 mW/Gb/s for Tx and Rx, respectively. This means the total power efficiency is estimated to be 5.91 mW/Gb/s. The power levels in this research are still high, because we employed a

TABLE I
PERFORMANCE COMPARISON OF THE STATE-OF-THE-ART SILICON PHOTONICS OPTICAL TRX ENGINES

	This work	[15]	[16]	[17]
Data rate x Channels (Aggregate bandwidth)	25 Gb/s x 16-ch (400 Gb/s)	28 Gb/s x 8-ch (224 Gb/s)	56 Gb/s x 2-ch (112 Gb/s)	20 Gb/s x 4-ch (80 Gb/s)
Engine Size (mm x mm)	11 x 10	13 x 9.6 (Estimated)	8 x 4	6 x 4.5
Bandwidth Density at Edge (Gb/s/mm)	40	23.3	28	4.4
Year	2017	2016	2015	2015

conventional MZI modulator. As for the Tx power, there is the potential to reduce it in future work. For example, we recently developed novel low-power modulators [13], [14]. We believe lower TRx can be realized by applying the modulators to the developed high-density TRx module.

Finally, the performances for the state-of-the-art high-density silicon photonics optical TRx engines are listed in Table I [15]–[17]. We confirmed that the developed TRx shows a broader aggregate bandwidth of 400 Gb/s and higher bandwidth density at the I/O side of 40 Gb/s/mm than those of the previously developed TRxs. To the best of our knowledge, we have achieved the broadest aggregate bandwidth and the highest density silicon photonics optical TRx in the world today.

IV. CONCLUSION

We realized an on-PKG-type broadband 16-ch $\times$ 25 Gb/s silicon photonics TRx. The aggregate bandwidth corresponds to 400 Gb/s, and demonstrated high-density transmission of 363 Gb/s/cm^2 thanks to carefully designed SI and PI and a flip-chip bonded high-density bridge structure. To the best of our knowledge, the developed silicon photonics optical TRx shows the broadest bandwidth and highest density in the world today. Furthermore, we successfully confirmed the 16-ch operation with low crosstalk penalties between Tx-to-Tx (1.4 dB), Rx-to-Rx (1.4 dB), and Tx-to-Rx ($\sim$0 dB). The developed TRx is promising for realizing broadband on-PKG-type optical TRx modules in the near-future optical interconnect.

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