Toward Programmable Microwave Photonics Processors

Daniel Pérez, *Student Member, IEEE*, Ivana Gasulla, *Senior Member, IEEE*, and José Capmany, *Fellow, IEEE*

(Invited Paper)

***Abstract*—We describe the advances that we, and others, have reported during the last years in the area of programmable microwave photonic processors. Following a brief historical sketch, we provide a detailed account of the salient theoretical and experimental results recently reported on waveguide mesh optical core processors. The incorporation of a waveguide mesh optical core into the general microwave photonics programmable processor architecture is then addressed. We illustrate through different examples how this processor can be programmed to enable the most important functionalities required in microwave photonics.**

***Index Terms*—Integrated optics, microwave photonics.**

I. Introduction

INFORMATION and communication technology (ICT) systems are expanding at an awesome pace in terms of capacity demand, number of connected end users and required infrastructure. According to recent forecasts [1]–[3], global mobile data traffic grew a 74 percent in 2015 alone to reach a figure of 3.7 exabytes per month worldwide, with this figure expected to experience an 8-fold increase to reach 30.6 exabytes per month by 2020. Furthermore, more than half of all traffic from mobile-connected devices will be offloaded to the fixed network by means of Wi-Fi devices and femto-cells each month. Similar growing rates are predicted for global internet [2] and data center traffic [3].

For ICT systems to cope with these rapidly increasing growth rates, there is a need for a flexible, scalable and future-proof solution for seamlessly interfacing the wireless and photonic segments of communication networks [4]–[7]. In addition, emerging paradigms such as 5G communications [7], [8], the Internet of Things (IoT) [9], car-to-car communications [4], wireless body and personal area networks (WB/PANs) [10], and high resolution sensing [11] are expected to push this pressure even further (see Fig. 1). The requirements demanded by most of these scenarios call for novel technology developments in both the physical layer and the network architectures. For instance, 5G wireless communications targets a 1000-fold increase in capacity, connectivity for over 1 billion users, strict latency control, and network software programming.

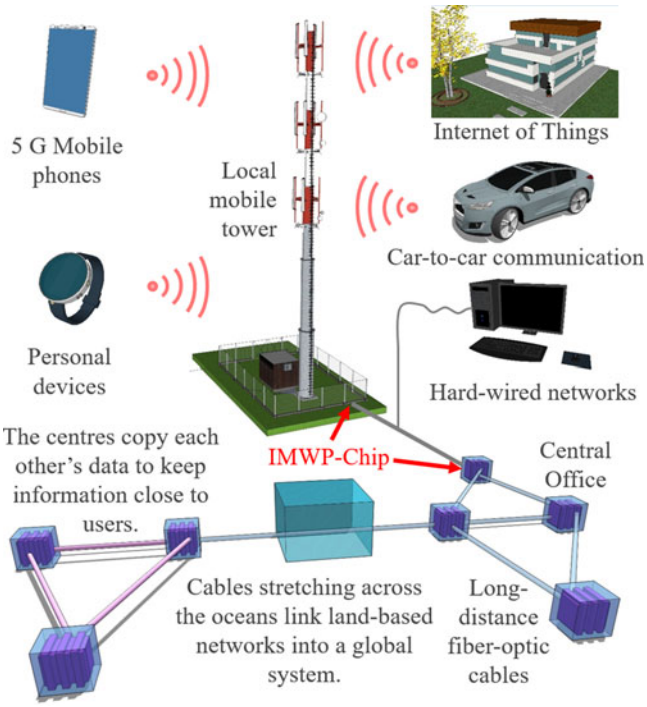

Fig. 1. Emerging ICT applications requiring smooth transition between the fiber and wireless segments of communication infrastructures (after [4]).

Radiofrequency (RF) or Microwave photonics (MWP) [12], [13], brings together the worlds of RF engineering and optoelectronics interfacing these highly dissimilar media. It is the best positioned technology to provide a flexible, adaptive and future-proof physical layer with unrivalled characteristics by enabling the realization of key functionalities in microwave systems, which are either complex or even not directly possible within the RF domain. Despite its tremendous potential, the widespread use and application of MWP is currently limited by the high-cost, bulky, complex and power consuming nature of its systems. The major challenge in

MWP research is therefore to reduce their cost, size, weight and power consumption (SWaP). Typical SWaP figures for commercial MWP systems are around 0.04–0.2 m^2 in size, 1.5–10 kg

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The authors are with the Photonics Research Labs, iTEAM Research Institute, Universitat Politècnica de València, Valencia 46022, Spain. (e-mail: jcapmany@iteam.upv.es; ivgames@iteam.upv.es; jcapmany@iteam.upv.es).

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in weight and 15–20 W in power consumption [14], making them unsuitable for the mass production and widespread use required by the next-generation and emerging applications outlined previously.

Integrated photonics has the potential to change the scaling laws of high-bandwidth systems through proper architectural choices that combine photonics with electronics to optimize performance, power, footprint and cost [15], [16]. In particular, analog photonics has a qualitatively different behavior compared to digital electronics since the energy per analog task is dominated by the steady-state bias power and does not increase significantly as the bandwidth increases. Furthermore, most photonic devices are currently highly temperature dependent and therefore, temperature regulation is required, which consumes the majority of bias power. As integrated photonics favors alternative means of temperature control, the power consumed by the photonic devices can be drastically reduced.

Drastic space, power consumption and weight reductions are immediate gains from Integrated Microwave Photonics (IMWP) [17], [18], which targets the incorporation of MWP components/subsystems in monolithic or hybrid photonic circuits. The activity in IMWP to date has almost exclusively focused on the so-called Application Specific Photonic Integrated Circuits (ASPICs) [17], [18], where a particular circuit and chip configuration is designed to optimally perform a particular MWP functionality. As a result, there are almost as many technologies as applications and, due to this considerable fragmentation, the market for many of these application-specific technologies is too small to justify their further development into cost-effective industrial mass-volume manufacturing processes.

A completely different approach is to consider the design of a universal MWP signal processor architecture, which based on a reconfigurable photonic waveguide core can be integrated on a chip, featuring parallel input/output operation and being capable of performing all the main functionalities by suitable software programming of its control signals [19]–[22]. Inspired by the similar flexibility principles of Digital Signal Processors (DSPs) and Field Programmable Gate Arrays (FPGAs), where a common hardware is shared by multiple functionalities through a software-defined approach (or programmability), this would allow for significant cost reduction in the hardware fabrication. Such a universal processor can overcome the former limitations and enable further flexibility and SWaP reductions as compared to the current ASPIC-based paradigm.

In this paper, we describe the advances that we, and others, have reported during the last years in this particular area of research. Section II provides a brief historical overview of the subject that covers from the initial proposal of the so-called MWP transistor (a subsystem resulting from the opening of the feedback loop of an optoelectronic oscillator), to its evolution towards a general MWP reconfigurable processor architecture, where the optical core is based on switching specific integrated signal processing subsystems such as delay lines, ring cavities and Mach-Zehnder Interferometers (MZIs). This approach leads to rather inflexible configurations.

An interesting approach to overcome the above limitation is to break down complex photonic circuits into a large network

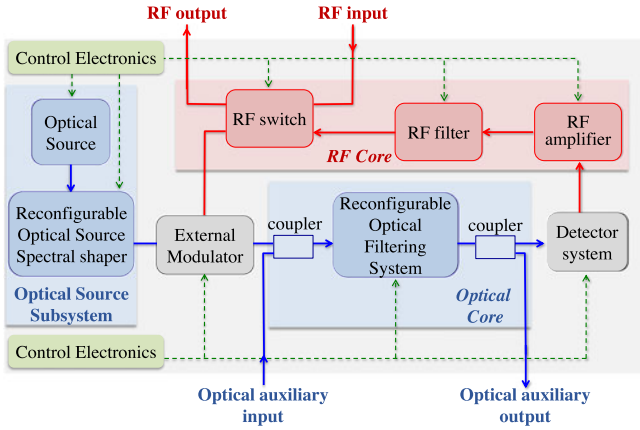

Fig. 2. Layout of a MWP transistor (After [27]).

of identical two-dimensional (2D) unit cells implemented by means of a MZI waveguide mesh or lattice. In Section III we consider this approach. We first review the seminal work by Zhuang and co-workers [22] who proposed a square waveguide mesh configuration to support this concept. Then, we revise the results that our group has reported on other waveguide mesh configurations [23]–[26], especially those pertaining to the hexagonal waveguide mesh configuration, for which optimum results as compared to other designs have been demonstrated for a comprehensive set of performance metrics. We then present the salient experimental results reported in the literature to implement the MWP signal processor core. In particular, the work in Silicon Photonics and Silicon Nitride structures is reviewed. In Section IV we discuss the implementation of the different MWP functionalities using the waveguide mesh core inside the overall MWP processor architecture. Finally, Section V addresses the future challenges and provides some conclusions.

II. Historical Development

The starting point for the MWP programmable processor can be traced back to the proposal of the MWP transistor [27] shown in Fig. 2, which is composed of subsystems, each of which is a collection of connected fixed-and-variable components.

The transistor configuration is obtained by opening the feedback loop of a generalized optoelectronic oscillator [28]. As it was shown in [27], this architecture is in principle capable of performing few, but important, required functionalities in MWP provided that its optical subsystems can be reconfigured by means of suitable control signals. The main limitation of the MWP transistor is however that it does not support the reconfiguration of interconnections between its internal optical subsystems. This results in an intermediate performance between ASPIC and a universal MWP processor.

As a first alternative to go one step further in terms of flexibility, the former approach can be extended to implement a *programmable MWP processor architecture* [20], which incorporates optical routing and switching elements (ORSEs) into the MWP transistor layout and replaces the reconfigurable optical filtering system by a more powerful and versatile optical core. The upper part of Fig. 3 schematizes the concept.

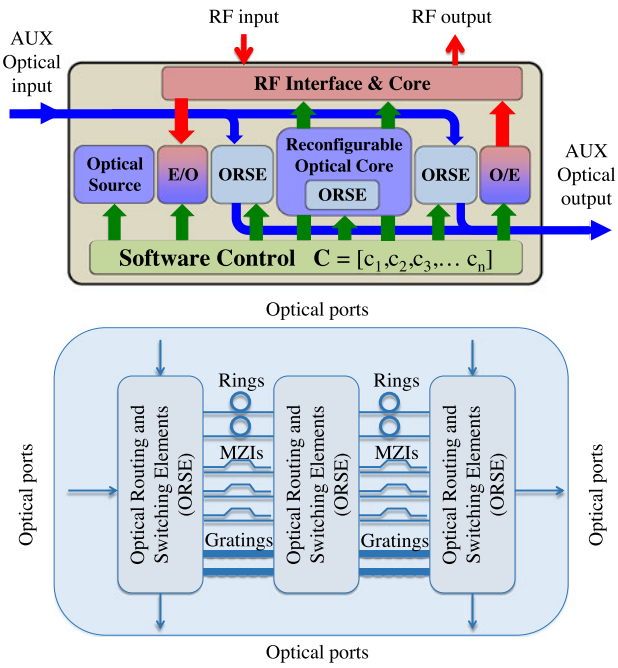

Fig. 3. (Upper) Layout of the universal processor (after [20]). (Lower) Particular implementation of the optical core using ad-hoc photonic components such as Mach Zehnder interferometers (MZIs), optical ring resonators (ORRs) and gratings connected by several optical routing and switching elements (ORSEs).

The central element of the programmable optical processor is the optical core, where the main signal processing tasks are carried in the photonic domain. Ideally, the optical core should be built upon a versatile architecture capable of implementing different functionalities in response to different electronic control signals. In practice, among the reconfigurable photonic circuits proposed in the literature, the ones that could especially emerge as candidates for this core are either based on the cascade of finite (i.e., Mach-Zehnder interferometers) or infinite (i.e., Ring Cavity) impulse response cells or a combination of both. These structures feature periodic filters and allow for bandwidth reconfiguration and notch tunability by moving the zeros and poles along the z-plane. Thus to further increase the degree of flexibility of the processor, the former configuration can be extended with a subsystem of switched optical signal processing elements including different types of fixed and reconfigurable filtering structures and interconnections, as illustrated in the lower part of Fig. 3. This example includes finite impulse response filters (FIR), infinite impulse response (IIR) and dispersive delay lines (DDL) that can be accessible by the correct programming of the ORSEs that interconnect them. The optical routing and switching elements would need to have medium-count ports depending on the number of component banks. This architecture, as discussed in [29], is still limited in a) flexibility, as ad-hoc designed photonic subsystems must be included and interconnected within the optical core, b) scalability, as fixed size photonic components are the building blocks for more complex circuits and c) loss, as considerable number of ORSEs need to be traversed to implement complex configurations.

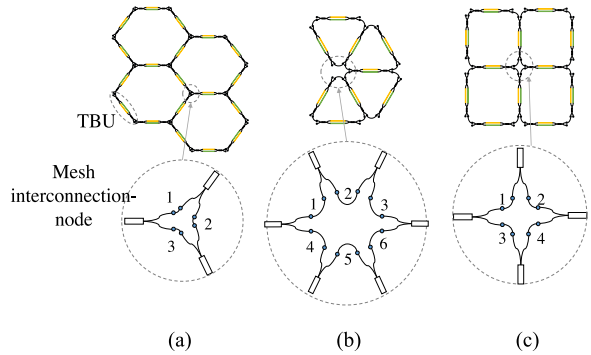

Fig. 4. Reconfigurable Mesh designs (upper): (a) Hexagonal type [23], (b) triangular type [23], (c) square type [26], and their associated interconnections points (bottom).

III. Waveguide Mesh Core Processors

A. Concept

A more versatile optical core architecture can be obtained by following similar principles as those of the FPGAs in electronics [21]. The central concept is based in breaking down complex circuits into a large network of identical two-dimensional (2D) unit cells implemented by means of a MZI waveguide mesh or lattice. Zhuang and co-workers [22] have been the first to propose a programmable optical chip architecture connecting MZI devices in a square-shaped mesh network grid. The distinctive feature of this approach is that it enables both feedforward and feedbackward filtering configurations, selecting the adequate path through the mesh and providing independent tuning of circuit parameters to complex valued coefficients by introducing phase tuning elements in both arms of the MZIs to enable independent control of amplitude and phase of light at coupler outputs. Further to the square shaped mesh, other configurations, such as the triangular and hexagonal geometries have been reported [23]. The operation principles of these and their comparative performance are discussed in the next subsection.

B. Waveguide Mesh Operation

Fig. 4 shows three different types of waveguide mesh designs. Fig. 4(a), (b) and (c) illustrate a 4-cell arrangement for the hexagonal, triangular and square-type meshes, respectively.

The basic building block of these meshes is a tunable coupler that must provide, independently, a complete splitting ratio tuning and phase response. This switching/tapping/de-phasing mechanism can be obtained either by exploiting the electro-refraction and/or the electro-absorption effect, or by means of the thermo-optic effect in a broadband 3-dB balanced MZI. By configuring each tunable coupler placed at each side of the cell perimeter as a switch (in either its cross or bar state) or as a tunable coupler, one can synthesize a given photonic integrated circuit topology, as shown in [22].

The upper part of Fig. 5 shows the tunable basic unit (TBU) composed by the tunable coupler and its access (input/output) waveguides. The geometry of the latter is a function of the bending radius and varies for each mesh topology due to different

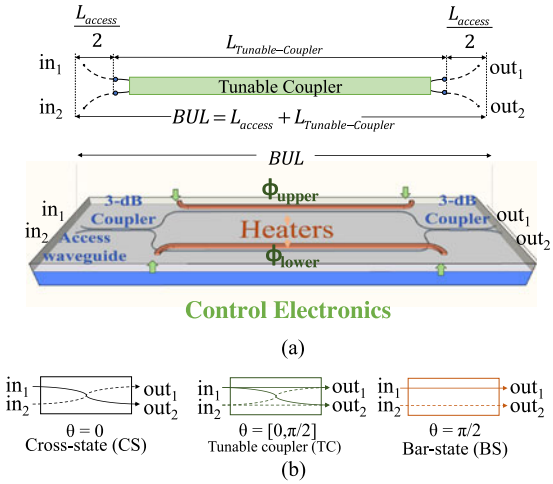

Fig. 5. (a) (Upper), Labeled schematic of a general tunable coupler acting as the basic building block of the mesh. The Basic Unit Length (BUL) is illustrated as the sum of the tunable coupler length and the arc length of the access waveguides. (Lower), Particular case of an integrated balanced MZI-based tunable coupler. (b) Signal flow for the different tunable basic unit (TBU) configuration states.

angle between elements. The basic unit length (BUL) is:

$$BUL = L_{access} + L_{Tunable-Coupler}, \tag{1}$$

where L_{access} is the overall length of the access waveguide segment and $L_{Tunable-Coupler}$ is the length of the tunable coupler.

Referring to Fig. 5(b), the tunable basic unit can implement 3 different states: cross state switch (light path connects in_1 to out_2 and in_2 to out_1), bar state switch (light path connects in_1 to out_1 and in_2 to out_2) and tunable splitter. For a balanced MZI loaded with heaters on both arms, the splitting ratio is obtained by increasing the effective index due to the Joule effect in the upper or lower arm, producing a ϕ_{upper} and ϕ_{lower} phase shift, respectively. Once set, a common drive in both heaters will provide a common phase shift, leading to independent control of the amplitude ratio and the phase. The device matrix is defined by:

$$h_{TBU} = je^{j\Delta}\begin{pmatrix}\sin\theta & \cos\theta\\ \cos\theta & -\sin\theta\end{pmatrix}\gamma, \tag{2}$$

where θ is $(\phi_{upper} - \phi_{lower})/2$ and Δ is $(\phi_{upper} + \phi_{lower})/2$. The coupling factor K is then defined as the $\cos^2(\theta)$ and the general loss term γ includes the effect of propagation losses in the access waveguides, the tunable coupler waveguide and the insertion losses for both 3-dB couplers.

The different waveguide mesh geometries have been analyzed and compared against a set of different figures of merit in [23], concluding that the hexagonal lattice yields the best performance for almost all the performance metrics. Table I summarizes the results of that analysis.

For reference, *the spatial tuning resolution step* quantifies which is the minimum step in BUL units by which the arm length mismatch or the cavity length can be increased/decreased, the *reconfiguration performance* of the mesh is given by the number of filters with different spectral period values that can be implemented given a maximum value X (in BUL units) for the path imbalance in unbalanced Mach Zehnder Interferometers (UMZIs) or the cavity length in Optical Ring Resonators (ORRs). The *replication flexibility* gives the number of possible alternative geometries for a specific filter implementation, while the *switching elements per unit area* denotes the amount of required BULs per surface unit to achieve an equivalent functionality. Finally, the two last rows in Table I quantify the overall losses in the TBUs of triangular and hexagonal waveguide meshes as compared to those in the square mesh configuration. A complete definition of the figures of merit can be found in [23].

TABLE I
SUMMARY OF VALUES FOR THE FIGURES OF MERIT OF THE DIFFERENT MESH DESIGNS (SEE DEFINITIONS IN [23])

Figure of Merit	Triangular	Square	Hexagonal
ORR cavity spatial tuning resolution step in BUL units (the lower the better)	3	4	**2* The first and second step has a resolution of 6 and 4.**
MZI arm imbalance spatial tuning resolution step in BUL units (the lower the better)	3	4	**2**
ORR reconfiguration performance (the higher the better) (for X=25 *BUL*)	8	6	**9**
MZI reconfiguration performance (for X=25 *BUL*)	8	6	**12**
Switching elements per unit area compared to *square* % (the lower the better for a fixed value of reconfiguration performance)	+65.00%	0.00%	**-36.66%**
Replication Ratio for ORR structures up to 16 BUL cavity length (the higher the better).	1	**2.68**	1.31
Replication Ratio for MZI structures up to 12 BUL interferometric length for a shorter path lower than 3 BUL. (the higher the better).	1	3	**3.36**
$L_{access}/L_{access\ square}$ % for a fixed radius of curvature *Ra* (the lower the better)	+33.33%	+0.00%	**-33.33%**
Ra/Ra_{square} % for a fixed BUL value (the higher the better)	-25.00%	+0.00%	**+50.00%**

With a suitable programming of a selected set of TBUs in the 2D waveguide mesh, different circuit layouts of variable complexity can be programmed over the same hardware. For example, the upper and lower parts of Fig. 6 show two implementation examples of simple UMZI FIR filters and ORR IIR filters with different path unbalance and cavity lengths, respectively. Filters with increased degree of complexity can be built upon cascading of these simple units, as shown experimentally in Section IV.

C. Experimental Results

Since waveguide mesh processor are a quite recent area of research, there are only few experimental results reported in

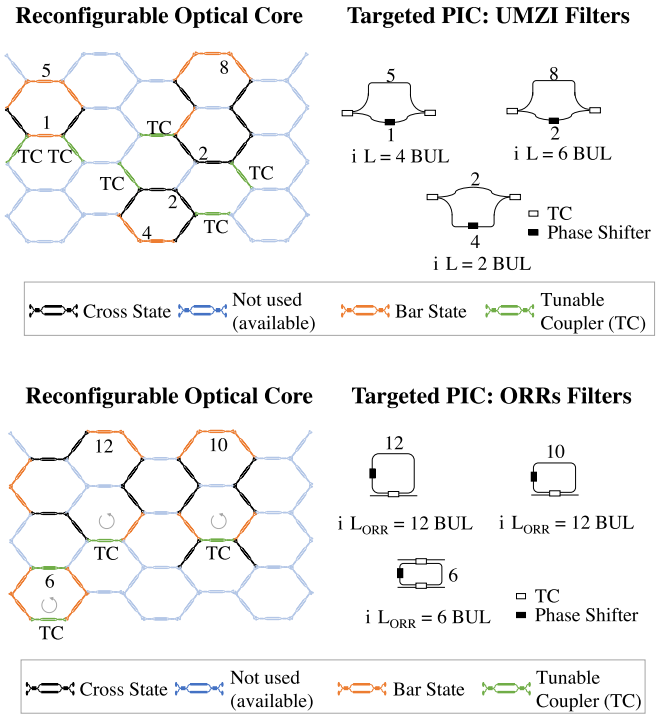

Fig. 6. (Upper) FIR filter implementations using a hexagonal waveguide mesh. (left) mesh setting for (top/right) three different targeted UMZI Filters,(Bottom/right) three different targeted ORRs.

the literature. Furthermore, despite the fact that recently a fully integrated multipurpose reconfigurable photonic processor has been reported using InP [30], the only configurations so far demonstrated in practice have been based on Silicon Nitride [22] and Silicon on Insulator (SOI) [31] technologies.

1) Si_3N_4 Chips: Fig. 7(a) shows the basic layout and photograph of the programmable optical chip architecture connecting MZI devices in a square-shaped mesh network grid proposed by Zhuang and co-workers [22]. The structure, fabricated in Si_3N_4, comprised two square cells and was employed to demonstrate simple FIR and IIR impulse response filters with single and/or double input/output ports of synthetized ORRs. The processor featured a free spectral range (FSR) of 14 GHz and is fully programmable. By appropriate programming of this processor, Zhuang *et al.* have demonstrated bandpass filters with a tunable center frequency that spans two octaves (1.6–6 GHz) and a reconfigurable band shape (including flat-top resonance with up to passband–stopband 25 dB extinction). They also demonstrated notch filters with up to 55 dB rejection ratio, Hilbert transformers and tunable delay lines as shown in Fig. 7(b).

2) SOI Chips: We recently reported the results of a waveguide mesh composed of 7 hexagonal cells fabricated in Silicon on Insulator [31]. The chip photograph is shown in Fig. 8. The device was fabricated at the Southampton Nanofabrication Centre at the University of Southampton. SOI wafers with a 220-nm thick silicon overlayer and a 3-μm thick buried oxide layer were used (for more details on fabrication and testing see [31]).

The overall structure comprised 30 independent MZI devices and 60 thermooptic heaters. The waveguide mesh MZI devices

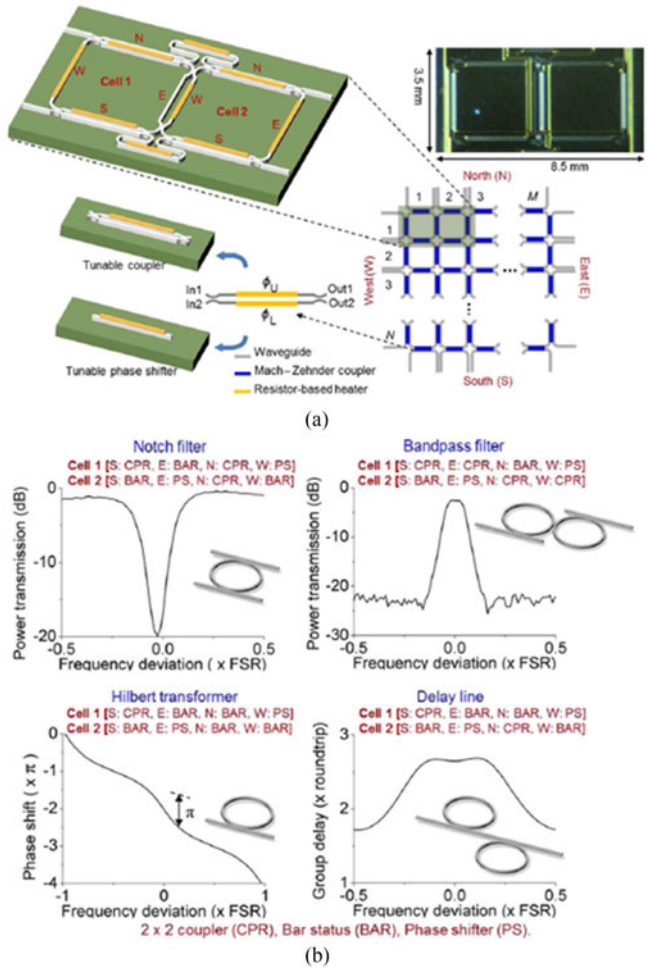

Fig. 7. (a) Schematic and a photo of the Si_3N_4 waveguide technology (TriPleX) chip implementing a 2 square cell waveguide mesh reported in [22]. (b) Different programmed circuit configurations obtained by varying phase-tuning elements in the chip and the measurements of their corresponding frequency responses.

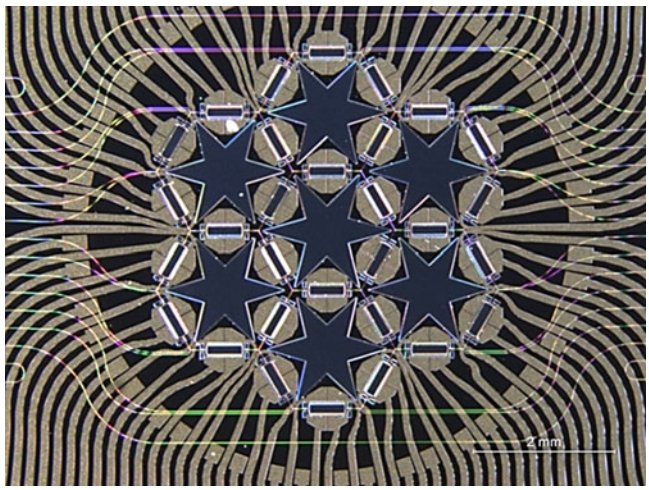

Fig. 8. Photograph of the 7-hexagonal cell waveguide mesh core fabricated in SOI and reported in [31].

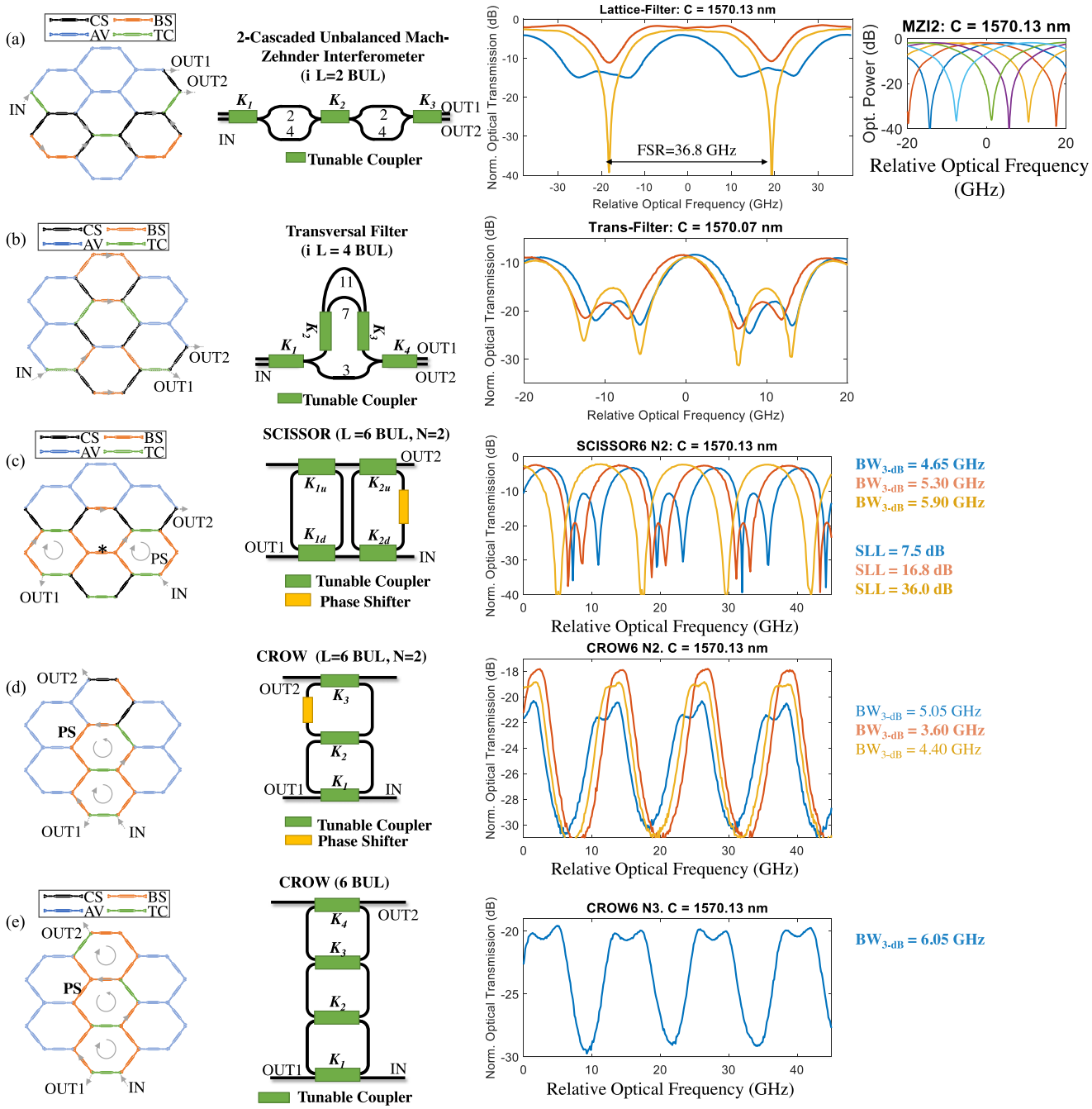

Fig. 9. Five examples of synthesised RF-photonic filters using the same 7-cell hexagonal mesh. In each case the left part shows the TBU settings in the mesh. The intermediate part shows the circuit layout and the right part shows the measured results for the RF transfer function modulus. (a) Two-cascaded Unbalanced 2-MZI FIR filter, (b) Three-tap transversal FIR filter, (c) Two-cavity SCISSOR FIR filter, (d) Two-Cavity CROW filter and (e) Three-cavity CROW Filter. MZI programming code: CS = Cross State switch, BS = Bar State Switch, TC: Tunable Coupler and AV: Available (unused).

where independently tuned in power splitting ratio and overall phase shift by means of current injection to the heaters deposited on top of the waveguides implementing the interferometer arms. Despite the simplicity of the layout depicted in Fig. 8, the 7-cell structure is capable of implementing over 100 different circuits. For MWP filtering applications basic MZI, FIR transversal filters, basic tunable ring cavities and IIR filters, as well as compound structures such as coupled resonator optical waveguides (CROWS) and side-coupled integrated spaced sequence of resonators (SCISSORS) are of particular interest. In [31] we reported different configuration featuring a wide variety of FSR values. Fig. 9 shows, for instance 5 examples of RF-Photonic FIR and IIR filters synthesised with the same hardware just by changing the operation state point of the different MZI elements in the mesh.

Another application of interest in RF-Photonics is true time delay lines as these are the basic building blocks of key functionalities, including arbitrary waveform generation and optical

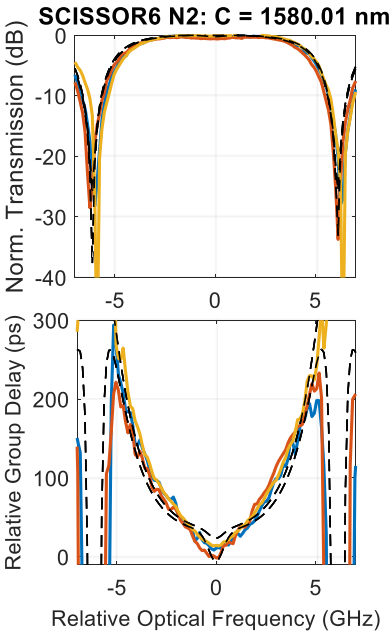

Fig. 10. Experimental (solid-line) and theoretical (dashed-line) results for 6-BUL ring resonator IIR dispersive delay line filter. 2-cascaded 6-ORR normalized transmission response (upper) and associated group delay (lower).

beamforming. The hexagonal waveguide mesh core can implement both dispersive as well as discrete time programmable true time delay lines.

For example, the proposed core can be designed to perform arbitrary group delays for ideally flat-passband filters employing MZIs or ORRs. Fig. 10 displays the modulus and group delay of a two cavity SCISSOR filter (see layout of Fig. 9(c)), where the coupling constants have been programmed to feature a flat-top bandpass and a parabolic dispersive group delay line featuring up to 215 ps inside the 3-dB bandwidth of the filter, what translates to a dispersive delay coefficient of 4.3 ns/nm, equivalent to more than 200 km of optical fiber.

Large discrete delay lines can be programmed by suitably tuning the TBUs involved in the light path. As an example, Fig. 11 illustrates two different settings for the 7-cell layout. In the first case, the light is travelling through 5 BULs, which results in a delay of 67.5 ps.

When the light path is modified as in the companion figure, the light path length was increased to 9 BULs, which corresponds to 121.5 ps. In the lower part of the figure, we have included some of the experimental delays obtained by changing the light path length from 3 to 12 TBUs (40.5–162 ps). Our device losses per delay figure was 44.44 dB/ns.

Simple optical beamforming configurations based on optical delay lines can be as well programmed in our 7-cell core. By configuring some of the TBUs as tunable couplers, it is possible to create adjacent light-paths with an incremental length ΔL. This incremental length will define the tilt angle of the antennas placed at the outputs [32]. Fig. 12 illustrates two measured cases that implement in the waveguide mesh a different optical delay $\Delta\tau$ corresponding to 2 and 3 BULs, respectively.

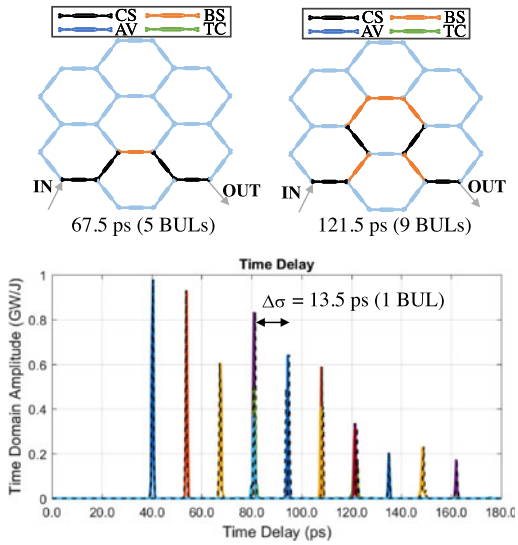

Fig. 11. Discrete optical delay line programming in the 7-cell hexagonal waveguide mesh. 7-cell layout and settings for two different time delays. (upper). Measured delays from 3 to 12 BULs (lower).

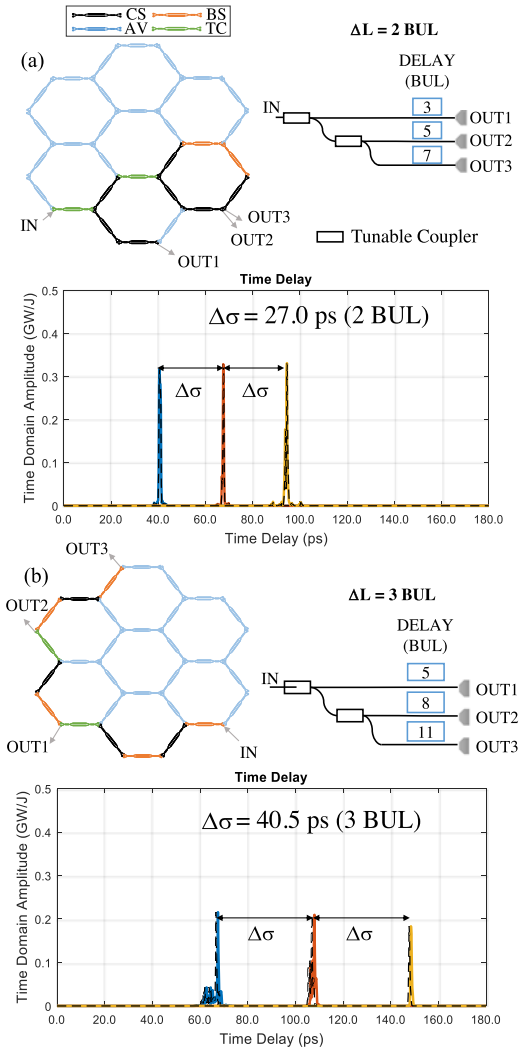

Fig. 12. Layouts and measured performance for two optical beamformer networks with different incremental delay implemented with the 7 hexagonal waveguide mesh: (a) 2-BUL delay, (b) 3-BUL delay.

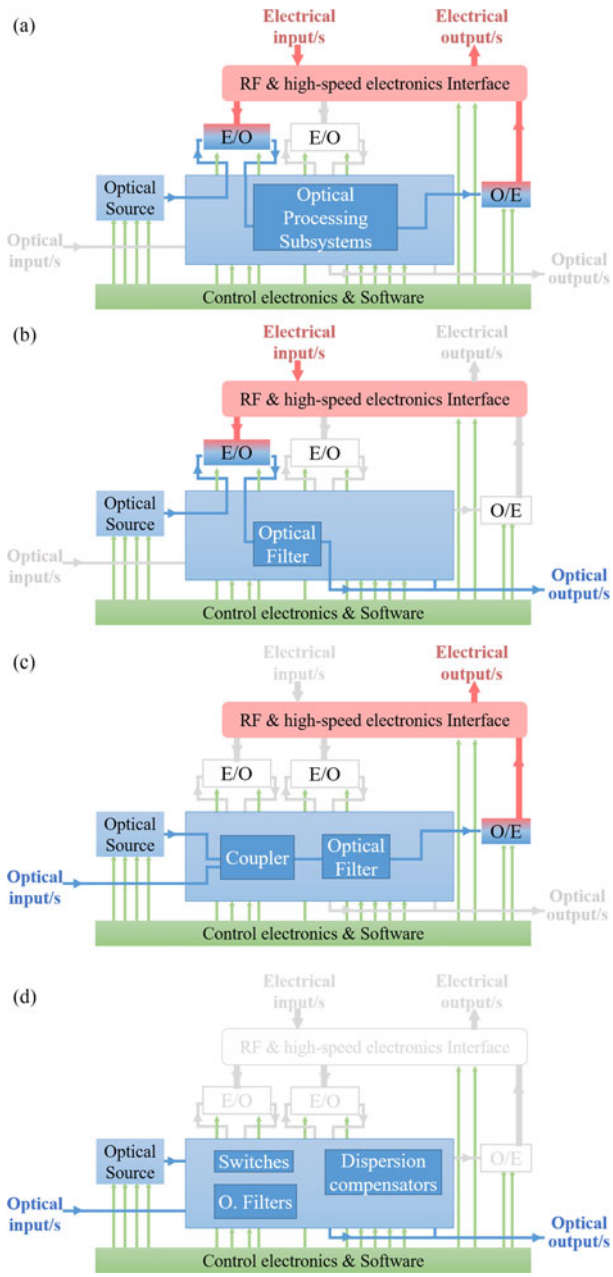

Fig. 13. Generic purpose MWP processor architecture programmed different modes of operation: (a) Electrical/Electrical, (b) Electrical/Optical, (c) Optical/Electrical and (d) Optical/optical.

IV. Overall MWP Processor Operation

The incorporation of the waveguide mesh structure in the MWP processor core enables a more versatile processor architecture, which is the one we propose for future development. In this architecture, which we show in Fig. 13, all the subsystems are directly connected to the reconfigurable optical core. This architecture represents, to the best of our knowledge, the first proposal for a generic-purpose software-defined MWP processor that incorporates the possibility of modifying the control signal flow to reconfigure the processing and interconnecting subsystems as required. It supports four different modes of operation as far as the input/output signals are concerned: electrical/electrical, electrical/optical, optical/electrical and optical/optical operations.

Electrical/electrical operations are typically employed in MWP functionalities such as RF-filtering, instantaneous frequency measurement, frequency mixing, RF and millimeter-wave arbitrary signal generation to cite a few. It requires the processor to enable an optical source, electro-optic (EO) and optoelectronic (OE) converters as well as the reconfigurable optical core. Fig. 13(a) illustrates the signal flow for these operations. Note that if a second modulator is integrated, it can be enabled to perform frequency mixing operations based on the cascade of two EO modulators.

Sometimes, the processed signal has to be distributed over a particular fiber link length after generation and/or processing. The processor can leverage the inherent properties of optical fibers for distribution purposes. The electrical/optical mode is widely employed in radio-over-fiber MWP links. At the receiver point of the link, another multipurpose MWP processor can be employed. In this case, the receiver would be working in optical/electrical mode, processing the signal before the photo-detection. Optionally, the receiver can enable its own optical source to act as a local oscillator as well. Both modes of operation are displayed in Fig. 13(b) and (c), respectively.

The last mode of operation, illustrated in Fig. 13(d), is the optical/optical. In this case, the input signal can be processed directly in the optical domain. Optical channel management can then perform common optical processing operations such as add/drop, switching and broadcasting. Note that all the previous modes of operation may coexist for a certain multi-task functionality. For example, a modulated signal could be divided after being processed and both distributed through the optical ports and down-converted by the photodetectors.

In the previous section, we have shown that the hexagonal waveguide core is the best candidate to perform the reconfigurable optical core task: featuring subsystems interconnection as well as enabling versatile optical processing operations. By suitable programming each element on the processor, including the reconfigurable optical core, the same hardware can be configured to perform all the main functionalities required in MWP, as we illustrate in Figs. 14 and 15.

True time delay lines (DL): Together with tunable RF phase shifters are a key functionality required in complex signal processing applications. In particular, they constitute an essential building block in a considerable number of filtering and optical beamforming schemes. Discretely and continuously tunable DLs [33], [34] have been demonstrated, both of which can be supported by the MWP processor. Fig. 14(a) illustrates, for example, the processor settings for the implementation of a discrete true time delay based on the Single Carrier Tuning (SCT) approach, [34]. Note that four ORRs need to be enabled for the carrier tuning and optical delay line sections, as well as a double-loaded MZI for the implementation of the optical single side-band filter.

Filtering applications: The same hardware can be programmed as well to perform versatile RF-photonic tunable filtering. Here, the spectral characteristics of the optical filter implemented by the optical waveguide mesh core are directly

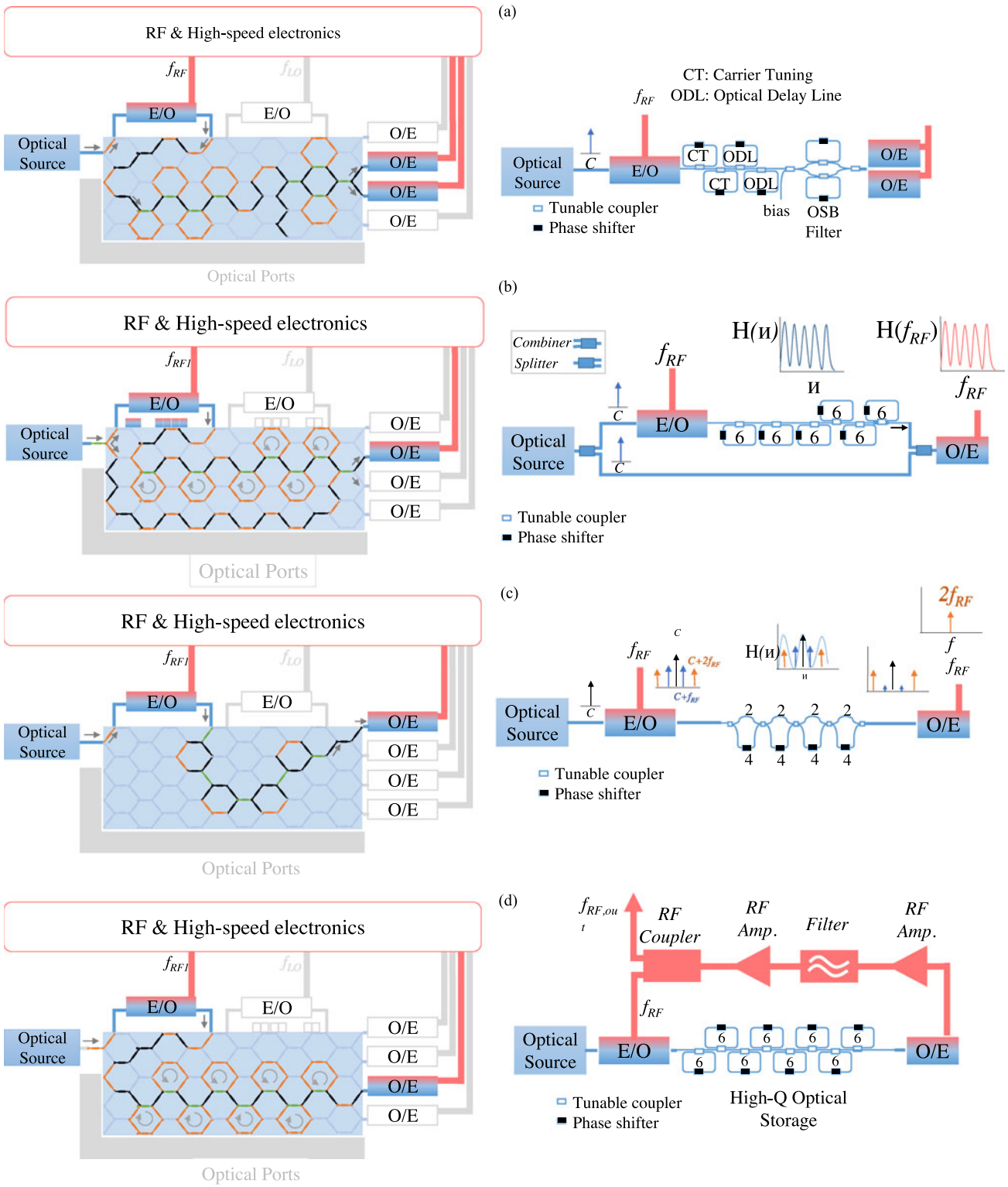

Fig. 14. (Left) Examples of MWP processor settings for the implementation of different MWP functionalities. For each functionality the circuit schemes are shown in the right handside: (a) true time delay line employing the Single Carrier Tuning (SCT) technique, (b) self-homodyne filter IIR, microwave and mm-wave tones generation based on (c) external modulation, and (d) optoelectronic oscillation.

translated into the RF spectrum by means of a self-beating homodyne technique, where part of the un-modulated optical carrier is sent separately and combined with the RF-modulated and optically filtered prior to photodetection, as illustrated in Fig. 14(b), [35]. In this example, the synthetized RF filter is implemented by means of 6 cascaded ORRs.

Microwave and mm-wave tone generation: This functionality enables the photonic generation and distribution of

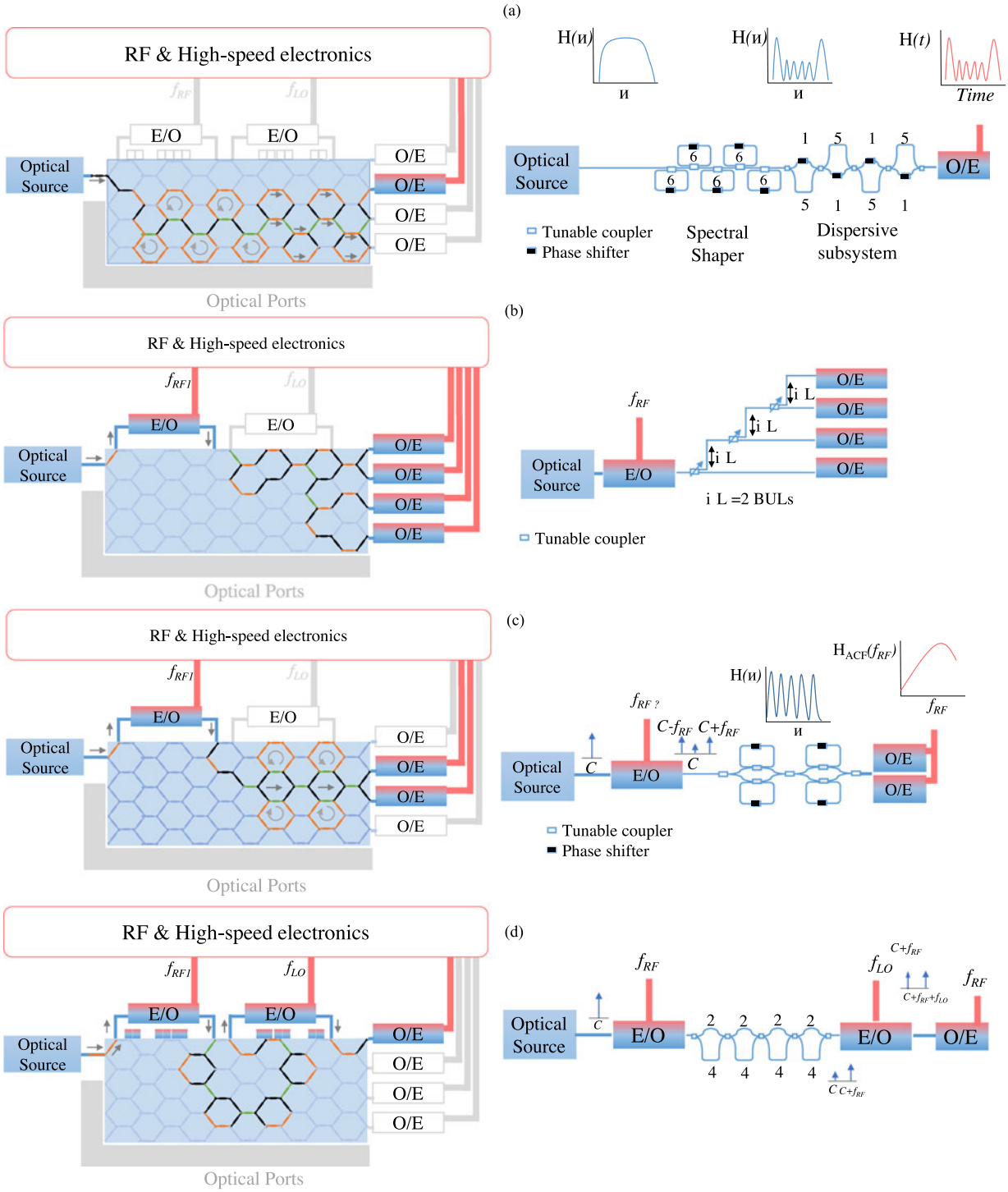

Fig. 15. (Left) General-purpose photonic processor settings for the implementation of a particular MWP scheme (right): (a) arbitrary waveform generation based on wavelength-to-time mapping, (b) beamforming networks based on true time delay, (c) instantaneous frequency measurement, and (d) RF-mixing based on 2 cascaded modulators.

high-frequency RF signals, [36], [37]. Among the different approaches reported, we illustrate here the implementation of two. Fig. 14(c) depicts the programmable processor employing the external modulator with different modulation biasing points together with an optical filter to suppress the optical carrier and the undesired (odd or even) modes. The filter is implemented here with a fourth-order lattice of MZIs. The second approach consists in programming an optoelectronic oscillator by closing the feedback loop of the RF section, as shown in Fig. 14(d), [37]. In this example, the reconfigurable optical core implements a High-Q optical storage section with seven ORRs.

Arbitrary waveform generation: This application consists in the generation of ultra-broad bandwidth RF waveforms with arbitrary and reconfigurable phase or amplitude characteristics.

Wavelength-to-time mapping is a promising solution and can be integrated on a chip, [38]. A broadband optical source is filtered by a spectral shaper. The spectral shape can be translated to the time domain by a dispersive element. Fig. 15(a) illustrates the processor settings to configure the spectral shaper by means of five cascaded ORRs [38], and a dispersive element implemented by a fourth-order lattice filter, [39]. Note that versatility is the most valuable property of the spectral shaper, and the hexagonal waveguide processor core suits perfect for this task, as demonstrated in the previous section. Higher dispersive delays might be required and could be obtained by employing the optical ports for the connection of dispersive fiber reels.

Beamforming networks: These systems are widely used to feed the radiating elements of phased array antennas. The radiation characteristics of an array can be modified by changing their electrical excitations, [32]. The use of tunable delay lines allows a stable pointing angle independent of the transmitted frequency, enabling broadband operation, [32]. Fig. 15(b) illustrates the implementation of a beamformer based on the natural discrete delay lines of the hexagonal core, as experimentally shown in Section IV. By modifying the length of the paths, the differential delay can be changed. The tilt angle tuning will be limited to discrete values in the range of $[-\pi, \pi]$.

Instantaneous frequency measurement: These systems are employed to measure the frequency of microwave signals in real-time applications. Fig. 15(c) depicts one of the approaches that consist in mapping the unknown microwave frequency to an optical power ratio by establishing a unique relationship, commonly referred as the amplitude comparison function (ACF), that is independent of both the laser and input RF powers. The ACF can be performed by a 2×2 complementary filter, [40], [41]. In this case, the filter is implemented by means of 2 cascaded balanced MZIs loaded with a total of 4 ORRs. Sharper filter functions lead to an increase in the resolution at the expense of reducing the frequency range. A key advantage of the reconfigurable processor is that the ACF can be made reconfigurable, so multiple measurements can be done while reconfiguring an ACP for each frequency range of measurement.

Frequency mixing: Frequency up-and/or down-conversion of RF signals is typically required in many radio-over-fiber and intermediate-frequency-over-fiber systems, [42]. Fig. 15(d) illustrates the processor configuration to achieve this functionality, where an optional optical filter, this time implemented by a fourth-order lattice filter, is employed to suppress the possible intermodulation contributions prior to the second modulator input.

For some of the previous functionalities, the integration of an optical amplifier subsystem or an optical amplifier array prior photodetection would be required to overcome the electrooptic and optoelectronic conversion losses.

V. Non-Ideal Effects and Main Limitations

The ideal behavior of the TBU leads to the perfect performance of the reconfigurable optical core. However, in practice, several sources of degradation must be taken into account: imperfect splitting ratios, phase control, parasitic back-reflections, loss imbalances, fabrication errors (gradients through the circuit in thickness or temperature), and drift in time, [43]. We briefly discuss the most important ones below.

Internal reflections and non-ideal states: Before programming the reconfigurable optical core, all the TBUs must be pre-characterized and their associated coupling factor vs electrical current saved on look-up tables. The use of imperfect 3-dB couplers and/or possible fabrication errors that change the losses in the upper/lower arm of each TBU introduce optical crosstalk, which is typically between 20 and 35 dB. Due to the cascade arrangement of TBUs, and the potential light recirculation of the mesh topologies reviewed here, large optical crosstalk or a drift in each TBU state leads to signal leaking through the mesh. From a photonic integrated circuit point of view, this effect would be similar to the addition of interferometric structures through different points in the ideal circuit with reduced coupling coefficients that will deteriorate the desired performance, [43]. In [31], a TBU optical crosstalk below 30 dB was measured and was maintained during the experimental demonstrations of programmed complex PICs, showing the robustness of the configured states.

In practice, one can tune the non-used TBUs to guide the reflected and leakage signals as far as possible from the defined circuit or to defined drain optical ports.

Accumulated losses: Due to the cascaded-arrangement, the TBU insertion losses are one of the most limiting issues in optical mesh networks. Losses limit the maximum number of TBUs to define the programmed circuit and thus, the versatility of the overall mesh. In [31], these losses were measured to be 0.6 ± 0.1 dB, mainly limited by MMI insertion losses of 0.15 ± 0.10 dB. To overcome this limitation, the use of directional couplers might be considered, since they introduce losses mainly associated to the propagation of the light and reduce back-reflected power. Due to the cascaded arrangement, a minimum TBU performance improvement leads to a high improvement in the overall mesh behavior. State-of-the-art MMI insertion losses are below 0.1 dB in silicon photonics [44] while the propagation losses are 1 dB/cm, [45].

Miniaturization tradeoff: minimum delay and losses. As stated in Section III, the BUL and the group index will determine the minimum delay. The BUL is mainly limited by the tuning mechanism length and the 3-dB coupler lengths. 3-dB couplers in silicon can be reduced to less than 50 μm, including the bend sections [44], [46] and heaters of 62 μm [47]. With the inclusion of bends and straight waveguides sections to increase the distance between both arms of the TBU to decrease thermal crosstalk, a total BUL of 240 μm seems achievable. Assuming a typical SOI group index of 4.18, this is translated to maximum FSRs of around 150 and 50 GHz for the synthesis of MZIs and ORRs, respectively, in the hexagonal waveguide mesh topology. However, a reduction of the BUL implies that the signal must go through a greater number of TBUs to obtain a desired delay. If the 3-dB couplers limit the overall IL of the TBU, this miniaturization trade-off must be considered.

Thermal stability and crosstalk: Due to the temperature dependence of PICs, they require, in general, thermal management. A typical strategy is to maintain the bottom of the PIC at a

constant temperature for which the PIC has been designed. In [31], we checked the thermal stability of our setup by synthetizing a simple optical ring resonator in the mesh and by measuring the wavelength drift of a particular spectral notch for 2 different temperatures, resulting in a notch wavelength drift of 7 pm during more than 45 min. This drift is associated to the temperature controller stability employed.

Neighboring TBUs may introduce undesired phase shift due to thermal crosstalk. The heat will flow, not only to the targeted waveguide underneath, but also to the adjacent ones producing a phase shift. In order to minimize this effect, thermal isolation trenches were introduced in the design and fabrication to increase the thermal resistance in the waveguide plane, increasing the heat flow to the thermal sink. The results obtained for the coupling constant versus injection current seem to be reasonably immune to thermal crosstalk. We attribute this to the fact that the arms of the MZI implementing the TBU are so close that both will experience almost the same crosstalk-induced temperature variation. However, due to the non-optimized metal layer, a non-negligible undesired common phase is induced to adjacent TBUs. This problem can be solved either by dynamic monitoring [51], a different tuning mechanism or deeper isolation trenches like in [48]. The fully-integrated design must prevent a temperature gradient over the PIC, produced typically by the optical source, the optical amplifiers and the IC for the correct chip behavior.

Power Consumption and integration density: To induce a π-phase shift, the thermo-optic phase shifters in silicon nitride typically consume more power ($\sim$300 mW) due to the low thermo-optic coefficient of the silicon nitride when compared to silicon ($\sim$30 mW). In [31], the thermal tuners were not optimized to prevent from misalignment errors between the fabrication mask and thus obtained a relatively higher power consumption of 110 mW. Different techniques like employing isolation trenches to focus the heat on the waveguide core have been demonstrated to reduce the power consumption of this effect $<$1 mW, [48]. When compared to an ASPIC, the programmable photonic processor will consume more power, mainly the one consumed by the reconfigurable optical core settings and it associated drivers. Employing state-of-the art heaters leads to a core power consumption of 100 mW if we assume that less than 100 TBUs are employed, which can be correct if we consider that a greater number will lead to higher insertion losses. Alternative tuning mechanisms, such as PZT [49] or Electro-mechanics [50], are promising solutions to reduce the power consumption while enabling a reduction of the distance between TBU arms due to their reduced tuning-associated crosstalk. The integration in silicon of more than 450 thermo-optic-effect-based TBUs in optical switch networks has been recently demonstrated [51].

Overall processor performance: Most of the ASPIC-based signal processors, and in particular, the ones performing microwave photonic applications are not fully integrated. If a high-performance fully integrated system is targeted, which is essential for a reduction in the SWaP figures, all the integrated subsystems should improve their quality. To date, high-power low-noise lasers have not been integrated with low-loss low-half-wave voltage modulators and efficient photodetectors either in monolithic or heterogeneous integrated circuits. However, promising demonstrations of heterogeneous integration technology of standalone components set the path for the integration of more efficient photonic integrated circuits, [52], [53].

VI. Summary, Conclusions and Future Challenges

Generic purpose integrated RF-photonic programmable processors are called to play a key role in future MWP systems designed to support emerging fiber-wireless communication paradigms with expected massive takeover, such as 5G, IoT, smart cities and autonomous driving, to cite a few.

A particularly interesting architectural option for these processors, includes a programmable optical core based on a 2D waveguide mesh, which effectively works in a similar way to FPGAs in electronics. In this paper, we have described the advances that we, and others, have reported during the last years in this area of research. We have provided a brief historical sketch followed by a detailed report of the salient theoretical and experimental results reported on waveguide mesh optical core processors. The incorporation of the waveguide mesh optical core into the general MWP programmable processor architecture has been addressed as well and we have illustrated through different examples how this processor can be programmed to enable the most important functionalities required in MWP.

The challenges to be addressed by future research are the following: In a first step, the complete integration of all the required photonic components in the chip should be targeted. This includes the optical waveguide mesh core, the optical source/s, modulators and detectors. To achieve this target, it is most probable that a hybrid integration approach should be required in order to incorporate active elements (optical sources and amplifiers). InP is a good candidate for hybrid integration with both SOI and Si_3N_4 optical cores [52], [53]. The second challenge is the incorporation of the electronics and RF parts of the processor. In the case of the low frequency electronics, the CMOS compatibility of SOI and Si_3N_4 favors at least the integration of the required control electronics for the waveguide mesh optical core. RF integration is not so straightforward, and a first step will call for co-integration in different chips and subsequent packaging. A final challenge that can be envisaged at this stage is the control software development to achieve a truly software-defined programmable MWP processor that will enable a faster progress and the appearance of versatile and upgradable photonic integrated systems.

References

[1] Cisco Visual Networking Index: Global Mobile Data Traffic Forecast Update, 2015–2020, 2016, White Paper. [Online]. Available http://www.cisco.com/c/en/us/solutions/collateral/service-provider/visual-networking-index-vni/mobile-white-paper-c11-520862.html

[2] Cisco Visual networking Index: The Zettabyte Era: Trends and Analysis, 2016, White Paper. [Online]. Available: http://www.cisco.com/c/en/us/solutions/collateral/service-provider/visual-networking-index-vni/vni-hyperconnectivity-wp.html

[3] Cisco Global Cloud Index: Forecast and Methodology, 2014—2019, 2016, White Paper. [Online]. Available: http://www.cisco.com/c/en/us/solutions/collateral/service-provider/global-cloud-index-gci/Cloud_Index_White_Paper.html

[4] J. Hetch, "The bandwidth bottleneck," *Nature*, vol. 536, pp. 139–142, 2016.
[5] D. Novak *et al.*, "Radio-over-fiber technologies for emerging wireless systems," *IEEE J. Quantum Electron.*, vol. 52, no. 1, 2016, Art. no. 0600311.
[6] R. Waterhouse and D. Novak, "Realizing 5G: Microwave photonics for 5G mobile wireless systems," *IEEE Microw. Mag.*, vol. 16, no. 8, pp. 84–92, Sep. 2015.
[7] J. G. Andrews *et al.*, "What will 5G be?" *IEEE J. Sel. Areas Commun.*, vol. 32, no. 6, pp. 1065–1082, Jun. 2014.
[8] Al. Gosh *et al.*, "Millimeter-wave enhanced local area systems: A high-data-rate approach for future wireless networks," *IEEE J. Sel. Areas Commun.*, vol. 32, no. 6, pp. 1152–1163, Jun. 2014.
[9] A. Al-Fuqaha, M. Guizani, M. Mohammadi, M. Aledhari, and M. Ayyash, "Internet of things: A survey on enabling technologies, protocols, and applications," *IEEE Commun. Surveys Tut.*, vol. 17, no. 4, pp. 2347–2376, Oct–Dec. 2015.
[10] S. Movassaghi, M. Abolhasan, J. Lipman, D. Smith, and A. Jamalipour, "Wireless body area networks: A survey," *IEEE Commun. Surveys Tut.*, vol. 16, no. 3, pp. 1658–1686, Jul.–Sep. 2014.
[11] J. Hervás *et al.*, "Microwave photonics for optical sensors," *J. Sel. Topics Quantum Electron.*, vol. 23, no. 2, Mar./Apr. 2016, Art. no. 5602013.
[12] J. Capmany and D. Novak, "Microwave photonics combines two worlds," *Nature Photon.,* vol. 1, pp. 319–330, 2007.
[13] J. Yao, "Microwave photonics," *J. Lightw. Technol*., vol. 27, no. 3, pp. 314–335, Feb. 2009.
[14] [Online]. Available: http://www.pharad.com/s-q-band-rf-photonic-link.html#
[15] D. J. Blumenthal *et al.*, "Integrated photonics for low-power packet networking," *IEEE J. Sel. Topics Quantum Electron.*, vol. 17, no. 2, pp. 458–471, Mar./Apr. 2011.
[16] M. K. Smit *et al.*, "An introduction to InP-based generic integration technology," *Semicond. Sci. Technol.*, vol. 29, no. 8, 2014, Art. no. 083001.
[17] D. A. I. Marpaung *et al.*, "Integrated microwave photonics," *Laser Photon. Rev.*, vol. 7, pp. 1–33, 2013.
[18] S. Iezekiel, M. Burla, J. Klamkin, D. Marpaung, and J. Capmany, "RF engineering meets optoelectronics," *IEEE Microw. Mag.*, vol. 16, no. 8, pp. 18–45, Sep. 2015.
[19] D. Pérez, I. Gasulla, and J. Capmany, "Microwave photonics transistor design equations," in *Proc. Int. Topical Meeting Microw. Photon./9th Asia-Pac. Microw. Photon. Conf.*, Sendai, Japan, 2014, pp. 82–85.
[20] D. Pérez, I. Gasulla, and J. Capmany, "Software-defined reconfigurable microwave photonics processor," *Opt. Express*, vol. 23, pp. 14640–14654, 2015.
[21] J. Capmany, I. Gasulla, and D. Pérez, "Microwave photonics: The programmable processor," *Nature Photon.*, vol. 10, pp. 6–8, 2016.
[22] L. Zhuang *et al.*, "Programmable photonic signal processor chip for radiofrequency applications," *Optica*, vol. 2, pp. 854–859, 2015.
[23] D. Pérez, I. Gasulla, J. Capmany, and R. A. Soref, "Reconfigurable lattice mesh designs for programmable photonic processors," *Opt. Express*, vol. 24, pp. 12093–12106, 2016.
[24] D. Pérez, I. Gasulla, J. Capmany, and R. A. Soref, "Integrated microwave photonics: The quest for the universal programmable processor," in *Proc. IEEE Photon. Soc. Summer Topical Meeting Series*, Newport Beach, CA, USA, 2016, pp. 144–145.
[25] D. Pérez, I. Gasulla, J. Capmany, and R. Soref, "Hexagonal waveguide mesh design for universal multiport interferometers," in *Proc. IEEE Photon. Conf.*, Waikoloa, HI, USA, 2016, pp. 285–286.
[26] D. Perez, I. Gasulla, J. Capmany, and R. A. Soref, "Hexagonal reconfigurable lattice mesh for programmable photonic processors," in *Proc. 42nd Eur. Conf. Opt. Commun.*, Düsseldorf, Germany, 2016, pp. 1–3.
[27] J. Capmany, J. Mora, P. Muñoz, and S. Sales, "A microwave photonics transistor," in *Proc. IEEE Topical Meeting Microw. Photon.,* Alexandria, VA, USA, 2013, pp. 190–193.
[28] L. Maleki, "Sources: The optoelectronic oscillator," *Nature Photon.*, vol. 5, pp. 728–730, 2011.
[29] D. Perez, I. Gasulla, and J. Capmany, "Honeycomb lattice meshes for reconfigurable universal microwave photonics processors," in *Proc. SPIE/COS Photon. Asia*, 2016, Paper 1002602.
[30] W. Liu *et al.*, "A fully reconfigurable photonic integrated signal processor," *Nature Photon.*, vol. 10, pp. 190–195, 2016.
[31] D. Pérez *et al.*, "General-purpose silicon photonics signal processor core," *Nature Commun.*, vol. 8, 2017, Art. no. 636.
[32] M. Burla *et al.*, "On-chip, CMOS-compatible, hardware-compressive integrated photonic beamformer based on WDM," in *Proc. Int. Topical Meeting de Microw. Photon.*, Alexandria, VA, USA, 2013, pp. 41–44.
[33] X. Wang *et al.*, "Continuously tunable ultra-thin silicon waveguide optical delay line," *Optica*, vol. 4, no. 5, pp. 507–515, 2017.
[34] M. Burla *et al*., "Separate carrier tuning scheme for integrated optical delay lines in photonic beamformers," in *Proc. Int. Topical Meeting Microw. Photon. Conf. Microw. Photon.*, Singapore, 2011, pp. 65–68.
[35] D. Pérez, I. Gasulla, J. Capmany, J. S. Fandiño, P. Muñoz, and H. Alavi, "Figures of merit for self-beating filtered microwave photonic systems," *Opt. Express*, vol. 24, no. 9, pp. 10087–10102, 2016.
[36] G. Qi, J.Yao, J. Seregelyi, S. Paquet, and C. Belisle, "Generation and distribution of a wide-band continuously tunable millimeter-wave signal with an optical external modulation technique," *IEEE Trans. Microw. Theory Techn.*, vol. 53, no. 10, pp. 3090–3097, Oct. 2005.
[37] L. Maleki, "Sources: The optoelectronic oscillator," *Nature Photon.*, vol. 5, pp. 728–730, 2011.
[38] M. H. Khan *et al.*, "Ultrabroad-bandwidth arbitrary radiofrequency waveform generation with a silicon photonic chip-based spectral shaper," *Nature Photon.*, vol. 4, pp. 117–122, 2010.
[39] K. Jinguji and Y. M. Kawachi, "Synthesis of coherent two-port lattice-form optical delay-line circuit," *J. Lightw. Technol.*, vol. 13, no. 1, pp. 73–82, Jan. 1995.
[40] H. Shao, H. Yu, X. Jiang, J. Yang, and G. Roelkens, "Large bandwidth and high accuracy photonic-assisted instantaneous microwave frequency estimation system based on an integrated silicon micro-resonator," in *Proc. IEEE 11th Int. Conf. de Group IV Photon.*, Paris, France, 2014, pp. 47–48.
[41] J. S. Fandiño and P. Muñoz, "Photonics-based microwave frequency measurement using a double-sideband suppressed-carrier modulation and an InP integrated ring-assisted Mach–Zehnder interferometer filter," *Opt. Lett.*, vol. 38, no. 21, pp. 4316–4319, 2013.
[42] K.-P. Ho, S. Liaw, and C. Lin, "Efficient photonic mixer with frequency doubling," *IEEE Photon. Technol. Lett.*, vol. 9, no. 4, pp. 511–513, Apr. 1997.
[43] D. Pérez, "Integrated microwave photonic processors using waveguide mesh cores," Ph.D. dissertation, Universitat Politècnica de València, València, Spain, 2017.
[44] Z. Sheng *et al.*, "A compact and low-loss MMI coupler fabricated with CMOS technology," *IEEE Photon. J.*, vol. 4, no. 6, pp. 22272–2277, Dec. 2012.
[45] T. Horikawa *et al.*, "Low-loss silicon wire waveguides for optical integrated circuits," *Mater. Res. Soc.*, vol. 6, no. 1, pp. 9–15, 2016.
[46] G. W. Cong *et al.,* "Demonstration of a 3-dB directional coupler with enhanced robustness to gap variations for silicon wire waveguide," *Opt. Express*, vol. 22, no. 2, pp. 2051–2059, 2014.
[47] N. C. Harris *et al.*, "Efficient, compact and low loss thermos-optic phase shifter in silicon," *Opt. Express*, vol. 22, no. 9, pp. 10487–10493, 2014.
[48] Fang *et al.*, "Ultralow power silicon photonics thermo-optic switch with suspended phase arms," *IEEE Photon. Technol. Lett.*, vol. 23, no. 8, pp. 525–527, Apr. 2011.
[49] C. W. Wong *et al.*, "Strain-tunable silicon photonic band gap microcavities n optical waveguides," *Appl. Phys. Lett.*, vol. 84, no. 8, pp. 1242–1244, 2004.
[50] M. W. Pruessner *et al.*, "Effective index tuning in micro-opto-mechanical structures using gradient electric forces," in *Proc. IEEE Photon. Soc. Summer Topical Meeting Series*, Newport Beach, CA, USA, 2016, pp. 164–165.
[51] D. Celo *et al.*, "32x32 silicon photonic switch," in *Proc. OptoElectron. Commun. Conf./IEEE Photon. Switching*, 2016, pp. 1–3.
[52] M. J. R. Heck *et al.*, "Hybrid silicon photonic integrated circuit technology," *IEEE J. Sel. Topics Quantum Electron.*, vol. 19, no. 4, Jul/Aug. 2013, Art. no. 6100117.
[53] C. G. H. Roeloffzen *et al.*, "Silicon nitride microwave photonic circuits," *Opt. Express*, vol. 21, pp. 22937–22961, 2013.

Daniel Pérez was born in Yecla, Spain. He received the B.Sc. degree in telecommunications in 2014 and the M.Sc. degree in telecommunication technologies, systems, and networks in 2015 from the Universitat Politècnica de València (UPV), Valencia, Spain, where he is currently working toward the Ph.D. degree in photonics. He has been involved in several research projects. He has authored or coauthored more than 30 international publications as a researcher with Photonics Research Labs, iTEAM Research Institute, UPV. His research interests include microwave photonics, focusing on integrated reconfigurable processors. He was the recipient of the COIT-AEIT award as the Best Final Degree Project in Fundamentals and Information Technologies, Communications and its Applications in 2015 and the 2017 IEEE Photonics Society Graduate Student Fellowship Award.

Ivana Gasulla (M'08–SM'16) received the M.Sc. and Ph.D. degrees from the Universitat Politècnica de Valencia (UPV), Valencia, Spain, in 2005 and 2008, respectively. She is currently a Senior Researcher with Photonics Research Labs, iTEAM Research Institute, UPV, as well as the Vice-Director for Promotion at the iTEAM Research Institute, since 2016. Between Stanford and Valencia, she has authored or coauthored more than 100 international publications. Her current research interests include space-division multiplexing technologies and microwave photonics systems. In 2016, she was the recipient of an ERC Consolidator Grant to develop new space-division multiplexing technologies for emergent fiber-wireless communications through the project InnoSpace. She was also the recipient of the 2008 IEEE Photonics Society Graduate Student Fellowship Award for her Ph.D. thesis, which is focused on broadband radio over multimode fiber transmission. Since 2014, she has been a member of the Technical Program Committee of the European Conference on Optical Communications.

José Capmany (M'92–SM'96–F'08) was born in Madrid, Spain, on December 15, 1962. He received the Ingeniero de *Telecomunicacion* degree from the Universidad Politécnica de Madrid (UPM), Madrid, in 1987, the Licenciado en Ciencias Físicas degree in 2009, the Ph.D. degree in electrical engineering from UPM, and the Ph.D. degree in quantum physics from the Universidad de Vigo, Vigo, Spain. Since 1991, he has been with the Departamento de Comunicaciones, Universitat Politècnica de València (UPV), Valencia, Spain, where he was involved with optical communications and photonics, founding the Photonics Research Labs. He has been an Associate Professor from 1992 to 1996, and Full Professor of optical communications, systems, and networks since 1996. In parallel, he has been the Telecommunications Engineering Faculty Vice-Dean from 1991 to 1996, and the Deputy Head of the Communications Department since 1996. From 2002 to 2016, he was the Director with the Institute of Telecommunications and Multimedia, UPVa. His research activities and interests include a wide range of subjects related to optical communications including microwave photonics (MWP), integrated optics, optical signal processing, fiber Bragg gratings, and more recently quantum cryptography and quantum information processing using photonics. He has authored or coauthored more than 520 papers in international refereed journals and conferences and has been a member of the Technical Program Committees of the European Conference on Optical Communications (ECOC), the Optical Fiber Conference (OFC), the Integrated Optics and Optical Communications Conference, CLEO Europe, and the Optoelectronics and Communications Conference. He has also carried out activities related to professional bodies and is the Founder and current Chairman of the IPS Spanish Chapter, and a Fellow of the Optical Society of America and the Institution of Electrical Engineers. He has acted as a Reviewer for more than 35 SCI journals in the field of photonics and telecommunications. He is also the Founder and the Chief Innovation Officer of the spin-off company VLC Photonics dedicated to the design of photonic integrated circuits and EPHHOX dedicated to MWP instrumentation. He was the recipient of the 2012 King James I Prize Laureate on novel technologies, the highest scientific distinction in Spain, for his outstanding contributions to the field of MWP. He was also the recipient of the Extraordinary Doctorate Prize of the Universidad Politécnica de Madrid in 1992. He is a distinguished Lecturer of the IEEE Photonics Society for the 2013–2014 term, an Associate Editor of IEEE PHOTONICS TECHNOLOGY LETTERS and the IEEE JOURNAL OF LIGHTWAVE TECHNOLOGY. He has also been a Guest Editor for the IEEE JOURNAL OF SELECTED TOPICS IN QUANTUM ELECTRONICS, IEEE TRANSACTIONS OF MICROWAVE THEORY AND TECHNIQUES, and *Optics Express* feature issue on MWP.