Low-Loss Passive Si_3N_4 Serial-to-WDM Interface for Energy-Efficient Optical Interconnects

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***Abstract*—The increasing number of computational servers in data centers is imposing tighter constraints on the networking infrastructure. Scalable power efficient optical interconnect network becomes necessary to leverage the bandwidth capacity of current electronic switches or opto-electronic components. Hence, novel optical interconnect technology can enhance the network capacity by harnessing the feasibility of simultaneous processing of optical signal in the wavelength and time domains. In this paper, we present a four channel optical passive wavelength-striped mapping (PWSM) device, which passively time compresses/expands serial packets through optical wavelength multiplexing/demultiplexing. The PWSM device, which has a 1 × 4 channel optical wavelength demultiplexer with integrated optical delay lines, is designed in a low-loss Si_3N_4 (propagation loss ∼3.1 dB/m) waveguide platform. The PWSM device multiplexes/demultiplexes four WDM channels and offsets in time the adjacent channels to optically serialize/de-serialize data packets. In this demonstration, a 64 ns long data packet is formed at the output of the device by combining four 16 ns data segments of the packet in time domain. Incremental optical insertion loss between adjacent channels is ∼9.7 dB due to the integrated passive optical delay waveguides. The data rate of the four segmented packets and the combined packet is 25 Gb/sec. We have measured a bit error rate performance below 1×10^{-9} for the 64 ns serial data packet regenerated by the PWSM device for a received optical power of –6.7 dBm.**

***Index Terms*—Photonic integrated circuits, silica and silicon nitride photonics, wavelength filtering devices..**

I. Introduction

THE Internet traffic growth in the last decade demands important data processing capabilities in modern data centers which host a large number of computational servers. Hence, the type of interconnection network between the servers is a major concern to meet the increasing network traffic. Optical interconnection between servers can enhance network scalability and data processing by exploiting space, time, and wavelength domains [1]. To further address the scalability challenge, server throughput incremental techniques have been implemented based on dynamically changing data traffic patterns between the interconnected servers [2], [3]. To fully exploit the optical domain parallelism and tremendous bandwidth, electrical data must be aggregated. However, high-speed electronic serial-to-parallel and parallel-to-serial data conversion in the time domain become more complex to design and more power demanding as capacity increases. For example, recently demonstrated 56 Gb/s PAM-4 transceiver based serializer-deserializer (SerDes) designed in the 40 nm CMOS technology node dissipates 710 mW electrical power (transmitter: 290 mW and receiver: 420 mW, [4]). On the other hand, a comparatively low bandwidth 25 Gb/s PAM-4 transmitter dissipates 101.8 mW [5] and 22 Gb/s PAM-4 receiver dissipates 228 mW power [6]. Indeed, scalable processing capacity and interconnectivity between servers have an important impact on the overall power consumption of modern computational platforms where serializing and de-serializing data constitute an increased portion of the overall operating cost [7].

Wavelength-striping has been shown to be a technique to overcome some of the scalability and power consumption limitations [8], [9]. In [10], it was shown that it is possible to convert a serial packet stream to parallel streams using a passive wavelength-striped mapping (PWSM) technique. The proposed technique requires simultaneous optical filtering and delaying each time segment of the serial data packet with respect to its adjacent channel by a pre-determined amount of time using optical buffer delay lines. In data center applications, the discrete fiber-based PWSM device needs to be integrated on a photonic integrated circuit (PIC) to be used in the intra-card and inter-card schedulers proposed in [1], [11]. The card schedulers on the network interface cards (NIC) facilitate designing modular multiple rack-based optical interconnects, where they receive electrical data from the serial packet generators or microprocessors [12]. The E/O modules are also placed on the NIC along with the PWSM device [1]. The PWSM PIC can be an important building block of the wavelength-striped based intra-card and inter-card schedulers, which are typically located in the top-of-rack (TOR) switches. Therefore, for practical purpose, an integrated approach becomes essential for highly paralleled optical interconnects with increased off-chip bandwidth density requirement in data communication. In this work, an integrated PWSM device is designed using low-loss Si_3N_4 waveguides [13]. The integrated optical PWSM circuit performs wavelength filtering of four channels and optically delays each channel from its adjacent channel by 16 ns. The insertion loss of the adjacent channels varies due to the integrated optical delay lines, with measured relative insertion loss of 0 dB, 9.7 dB, 19.1 dB and 28.7 dB in $ch-1$, $ch-2$, $ch-4$ and $ch-3$, respectively, with respect to $ch-1$. The optical demultiplexer section of the PWSM device is designed with a frequency spectral range (FSR) of 12.8 nm and 3.2 ± 0.1 nm wavelength

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separation between adjacent channels. The maximum crosstalk measured is 15.2 dB. A complete demonstration of the PWSM serial-to-WDM and WDM-to-serial process requires two PWSM devices with complementary optical delay lines. In such a system, the serial-to-WDM process of the PWSM device is used for time-compression of the data packet at the transmitter side while the WDM-to-serial process of another PWSM device is used for time-expansion of the data packet at the receiver end. In this work, we design the later stage where the concept is experimentally demonstrated. The WDM-to-serial PWSM device reconstructs a 64 ns long data packet from four 16 ns data packets. The bit error rate (BER) performance of the aggregated 64 ns packet is below 1×10^{-9} for a received optical power of -6.7 dBm. The PWSM device exhibits a 2.3 dB power penalty.

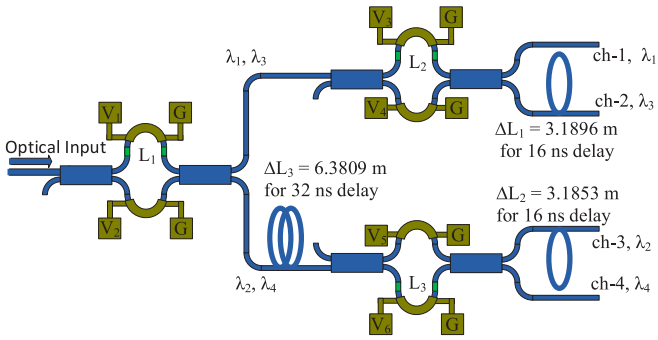


Fig. 1. Schematic of the four channel passive wavelength-striped mapping (PWSM) architecture with the integrated Cr heater on the delay arms of the Mach-Zehnder interferometer (MZI) (not to scale). V_1 to V_6: electrical pads to apply the DC voltages for thermal tuning, G: ground pads, ΔL_1 to ΔL_3: integrated delay waveguide lengths, L_1 to L_3: delay arm lengths in the MZIs (in green color).

II. Passive Wavelength-Striped Multiplexer Design

The PWSM PIC requires an optical demultiplexer with integrated low-loss optical delay lines. Si_3N_4 waveguide based low-loss optical delay lines delay the optical channels with respect to the adjacent channel for a specific amount of time. In this design, multiples of 16 ns are used for a WDM-to-serial process on a 64 ns long payload serial packet. Si_3N_4 waveguide with a cross-sectional area of 2.8 μm $\times$ 72 nm is used for lower loss properties necessary for the four optical delay lines of 0 m, 3.1896 m, 6.3809 m and 9.5662 m. The detailed characterization of this waveguide structure is presented in [14], with measured 3.1 dB/m propagation loss and group index (n_g) of 1.505 at the 1550 nm wavelength region.

In a conventional wavelength division multiplexing (WDM) based optical interconnect link, each wavelength is modulated using an optical modulator driven by the electrical serial data stream of the transmitter. The modulated optical wavelength channels are then multiplexed using an optical multiplexer (MUX) before transmission. This process requires one modulator per wavelength challenging the scalability of the optical interconnect link due to strongly coupled power consumption to the increasing number of modulators and electronic circuitry. In our proposed wavelength-striped data transmission process, the same data packet is simultaneously encoded on all WDM channels using one modulator. By time scaling the data packets from all the transmitters, the overall interconnect capacity can be scaled up [1]. A novel PWSM process enabling such process was initially demonstrated experimentally in [10], where one modulator was used to modulate eight wavelength channels with the same electrical data stream. The wavelength-striped process was implemented using discrete fiber-based off-chip delay lines and optical wavelength demultiplexer/multiplexer. However, time delaying the data packets with fiber delay lines requires long fiber lengths, which becomes impractical to implement as packet length increases in time. We first proposed the theoretical model of an integrated PWSM device with low-loss delay waveguides in [1]. Fig. 1 shows the schematic diagram of the PWSM PIC with four channels. In Fig. 1, the outputs (*ch-1*, *ch-2*, *ch-3* and *ch-4*) are the results of the PWSM circuit filtering each of the wavelengths and simultaneously time delaying the wavelength channels *ch-1* (λ_1), *ch-2* (λ_3), *ch-3* (λ_2) and *ch-4* (λ_4) by 0 ns, 16 ns, 48 ns and 32 ns, respectively.

In this section, we present the working principle of the integrated PWSM device. Next, we describe the design method of the long delay waveguides and their integration with the four channel optical demultiplexer.

A. Working Principle of the PWSM Device

Full functionality of the PWSM process is described in [1], [10], which requires two PWSM devices. In [10], eight WDM channels were modulated simultaneously with the same 2.5 Gb/s payload of 128 ns. The first PWSM device was used to apply 16 ns delay between each of the eight channels. The output of the first PWSM device was then gated to form the eight channel packet of 16 ns, such that the entire 128 ns long serial data packet was converted to a compressed 16 ns long WDM parallel packet. To recover the 128 ns long serial data packet from the 16 ns long parallel data packet, another PWSM device was used in [10] where the optical delay lines were oriented in a complementary manner. The complementary-oriented waveguide delay lines in the two PWSM devices also remove the optical power non-uniformity among the channels. This is achieved by applying increasing and decreasing order of time delays to the channels in the two PWSM devices. For example, the first channel (*ch-1*) in the PWSM device shown in Fig. 1 has no time delay waveguides in its optical path, whereas in the second PWSM device of the receiver node (not shown in Fig. 1), a 64 ns time delay will be applied to *ch-1*.

In this work, to explain the working principle of the PWSM device, we focus on one PWSM device and demonstrate how a 64 ns long data packet can be regenerated from four 16 ns data packets encoded on four distinct WDM channels. The same PWSM device can be used to demonstrate the full passive wavelength-striped process described in [10]. The working principle of the proposed device is shown in Fig. 2, where four WDM channels are simultaneously modulated with the same 64 ns long data packet using one modulator (not shown in Fig. 2). However only the first 16 ns of the packet segment

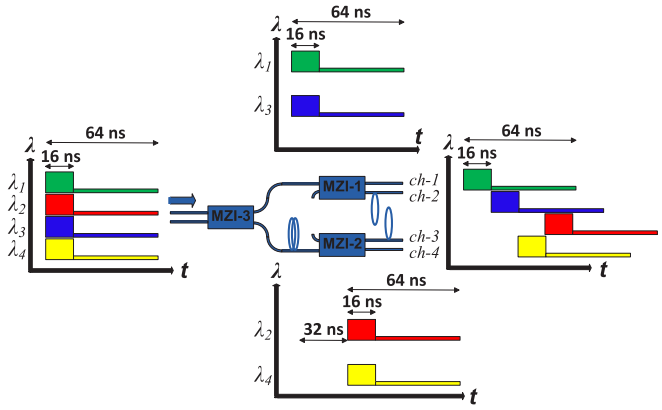


Fig. 2. Working principle of the proposed PWSM device. Four WDM channels (λ_1, λ_2, λ_3 and λ_4) containing the same data are filtered to four wavelength channels and delayed with respect to the adjacent channels by 16 ns.

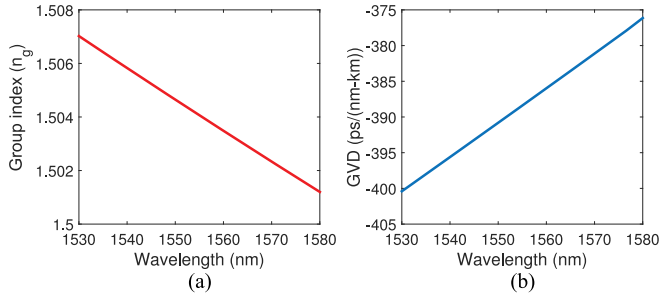


Fig. 3. Variation in the (a) group index (n_g) and (b) group velocity dispersion (GVD) of the 220 nm × 2.8 μm cross-section Si_3N_4 waveguide for the wavelength range from 1530 nm to 1580 nm.

contains information bits, where in the next 48 ns, the information bits are set to zero. The PWSM device filters the four WDM channels and time delays the adjacent channels by 16 ns. At the output of the device, a 64 ns long packet is formed over the four channels which can then be optically multiplexed and detected by an optical broadband receiver. It should be mentioned that, in this demonstration, each 16 ns segment contains the same data, whereas in [10] each of the 16 ns segments contains distinct data packet.

The optical demultiplexer section of the PWSM device has a channel separation of 400 GHz or 3.2 nm such that passive wavelength-striped process can be applied to 25 Gb/s or 50 Gb/s modulated data channels. While data rate and modulation format transparent, the current constraint of the demonstrated device is that the total packet length must be kept to 64 ns. Different delay lines need to be used for a different packet length and/or a different number of WDM channels. At higher data rate, the total number of bits per wavelength obviously increases proportionally. For example, at 25 Gb/s and 50 Gb/s data rate 1600 bits or 3200 bits can be allocated per packet, respectively, for serial to parallel or parallel to serial conversion.

The data rate of the wavelength-striped channels in the proposed device is set to 25 Gb/sec based on the 100 G Ethernet standard. In a network with four pairs of PWSM devices in the transmitter and receiver nodes, 100 G aggregated bandwidth can be achieved by the 4 × 25 Gb/sec WDM channels with time division multiplexing (TDM) interleaving [10]. At present, short reach interconnect distance from the server to switches is ∼2 m [15]. Therefore, the proposed PIC is suitable for using within the network interface cards (NIC) between the serial packet generators.

B. Design of the Long Delay Waveguides

The PWSM circuit demonstrated in this work, consists of MZI based filters incorporated with relatively long optical delay lines (ΔL_1, ΔL_2, and ΔL_3 in Fig. 1), where the longest delay line is 9.5662 m for $ch-3$ to implement 48 ns time delay. In the long length delay waveguides, the time delay mismatch between the wavelength channels due to the dispersion effect needs to be taken into consideration. We have calculated the group velocity dispersion (GVD) of the 220 nm × 2.8 μm cross-section Si_3N_4 waveguide from the group index (n_g) of the waveguide, by using the following equation:

$$D = \frac{1}{c_0}\frac{dn_g}{d\lambda}, \text{ where } c_0 \text{ is the velocity of light} \quad (1)$$

Fig. 3(a) and (b) show the FDTD simulation results of the group index and GVD of the waveguide over the wavelength range from 1530 nm to 1580 nm. The dispersion length of the waveguide for 25 Gb/sec data rate signal can be estimated from the following equation [16]:

$$L_D = \frac{2\pi c_0 T_0^2}{\lambda^2 |D|} \quad (2)$$

In (2), D is the GVD parameter of the waveguide and T_0 represents the half-width of a Gaussian pulse at $1/e$ intensity point. We assume $T_0 = 10$ ps ($T_0 \leq T_B/2\sqrt{2}$, calculated from [16]) for the 25 Gb/sec data rate signal (one bit time duration, $T_B = 40$ ps). The calculated value of the dispersion length for 25 Gb/sec data rate signal is $L_D = 200.7$ m, assuming $D = -391$ ps/(nm-km) at 1550 nm wavelength from Fig. 3(b). The longest delay line in the PWSM device is 9.5662 m (calculated in the next paragraph), which is approximately 20 times less than the dispersion length. Therefore, at 25 Gb/sec data rate, the output optical waveform from the PWSM device will not suffer distortion due to the dispersion effect.

To compensate for the time delay mismatch between the four WDM channels due to the dispersion, the required lengths of the delay lines are then determined by solving the following set of equations,

$$\Delta L_1 = \frac{c_0 \times T_3}{n_{g3}} \quad (3)$$

$$\Delta L_2 + \Delta L_3 = \frac{c_0 \times T_2}{n_{g2}} \quad (4)$$

$$\Delta L_3 = \frac{c_0 \times T_4}{n_{g4}} \quad (5)$$

Table I shows values of the input parameters (time delay, T and group index, n_g) in equations (3), (4), and (5). The group index of the waveguide at each of the wavelengths is obtained

TABLE I
DELAY WAVEGUIDE LENGTH IN THE PWSM DEVICE

Channel and wavelength	Time Delay (ns)	Group index	Delay Length (m)
1. ch-2, λ_3	$T_3 = 16$	$n_{g3} = 1.5049$	$\Delta L_1 = 3.1896$
2. ch-3, λ_2	$T_2 = 48$	$n_{g2} = 1.5053$	$\Delta L_2 + \Delta L_3 = 9.5662$
3. ch-4, λ_4	$T_4 = 32$	$n_{g4} = 1.5045$	$\Delta L_3 = 6.3809$

from Fig. 3(a). Table I also shows the calculated delay waveguide lengths.

From Table I, it is seen that to achieve a time delay of approximately 16 ns between adjacent channels, the length of the delay waveguides needs to be accurate within 0.1 mm or 100 μm. We estimate about 0.5 ps time delay mismatch for 100 μm waveguide length offset from the designed length. Therefore, considering the target data rate of 25 Gb/s (one bit duration = 40 ps), we set the length of the waveguide to be accurate up to 100 μm. Achieving this length accuracy in discrete fiber delay lines based PWSM device is challenging. However, in the Si_3N_4 waveguide based integration technology 100 μm length accuracy is achievable, considering the width of the waveguide is 2.8 μm.

C. Integration of the Delay Waveguides With the 4-Channel Demultiplexer

The optical demultiplexer without integrated delay lines has been designed and characterized in [14]. The four-channel device consists of three 2 × 2 Mach-Zehnder interferometer (MZI) based filters to demultiplex four 40 Gb/s WDM channels. A spiral-shaped 1.5 m long delay waveguide test structure is also characterized in [14] to determine the waveguide propagation loss. In this work, three spiral-shaped long delay waveguides (ΔL_1, ΔL_2, and ΔL_3) are monolithically integrated with the four-channel optical demultiplexer to design the PWSM device. The length of the optical delay waveguides is set to time delaying the 25 Gb/sec data rate channels in the multiples of 16 ns. On the other hand, the optical path delay lengths in the MZIs (L_1, L_2 and L_3) are designed to achieve a channel spacing of 3.2 nm (or 400 GHz) at the output of the PWSM device. MZI_1 requires a $\pi/2$ phase delay for effective filtering of channels λ_1 and λ_3, which is achieved by adding an extra delay length of 0.257 μm for this $\pi/2$ delay. To effectively tune the phase delay to $\pi/2$, we include a 12 mm long Cr heater (V_1 to V_6) on top of each of the MZI delay arms. The Cr heaters are monolithically integrated with the Si_3N_4 waveguide based PWSM device. The MZIs are designed using two 2 × 2 MMI-based couplers to achieve the optical broadband 3 dB coupling required for filtering in this proposed wavelength-striping technique. Fig. 4 shows the layout of one segment of the PWSM device containing the longest delay waveguide ($\Delta L_3 = 6.3809$ m) and one of the MZI filters.

The area of the PWSM device on the PIC is 4.2 cm × 4.7 cm. The input/output waveguides of the device are routed beyond this region to the edge of the chip to accommodate other test devices. The on-chip area of the longest delay waveguide ($\Delta L_3 = 6.3809$ m) is 2.3 cm × 2.3 cm. The whole PIC (area: 7 cm × 7 cm) also includes test devices such as a four-channel optical demultiplexer, MMI couplers, MZI filters, bent and straight waveguides.

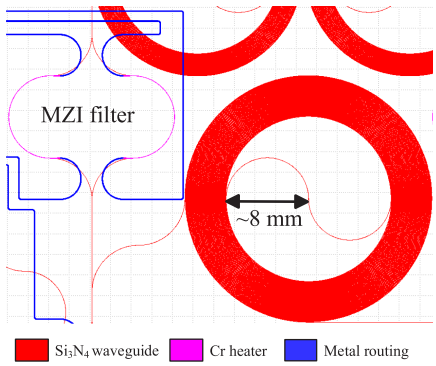


Fig. 4. Layout of the longest optical delay waveguide, $\Delta L_3 = 6.3809$ m, connected to one of the MZI filters of the PWSM circuit.

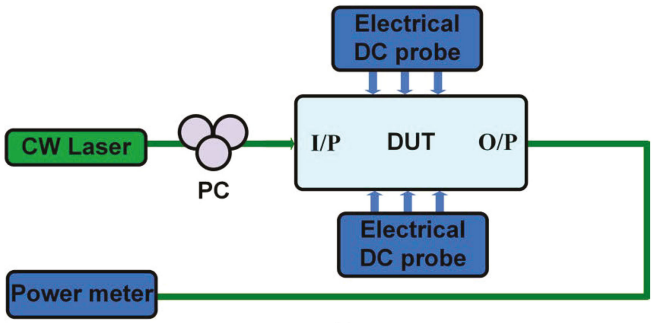
III. EXPERIMENT SETUP AND RESULTS

To characterize the PWSM device, we first determine the optical transmission response of the four wavelength channels. Next, the time delay between the adjacent channels is evaluated using a modulated optical waveform. The experimental results obtained are utilized to form a 64 ns long data packet from the four 16 ns long data segments. We also determine the BER and power penalty of the 64 ns long data packet generated by the PWSM device.

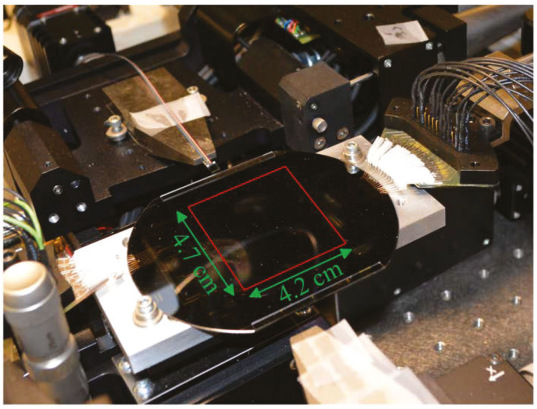
A. Optical Transmission Response of the PWSM Device

Fig. 5(a) shows the experimental setup to characterize the transmission response of the PWSM device (device under test, DUT) and to determine the insertion loss of each of the four channels of the PWSM device which are critical in this proposed system. In Fig. 5(b), the actual photograph of the PIC along with the fiber array and DC electrical probe has been shown. The optical phase shift in the delay arms of the MZI interferometers is thermally tuned to reduce crosstalk between the channels by applying a set of DC voltages for thermal heating in the corresponding delay arms. The thermal heating occurs from the electrical power loss in the resistive load of the heater. The applied DC voltages in the thermal heaters of the delay arms are $V_2 = 1.5$ V (0.31 mA), $V_3 = 4.1$ V (0.95 mA) and $V_6 = 2.4$ V (0.55 mA). The total electrical power consumption of the PWSM device from the thermal heaters is 5.68 mW. The wavelength of a continuous wave (CW) laser source is swept from 1525 nm to 1575 nm with a constant optical power at 12 dBm. A polarization controller is used at the input of the PWSM chip to reduce the polarization dependent loss in the Si_3N_4 waveguide. The optical output power from each of the four output channels of the PWSM circuit ($ch-1$, $ch-2$, $ch-3$ and $ch-4$) is recorded separately.

Fig. 6 shows the optical transmission response of each of the four channels of the PWSM device normalized to the optical output power of a reference straight Si_3N_4 waveguide. From



(a)



(b)

Fig. 5. (a) Experimental setup to measure the transmission response of the four channel PWSM device, (b) Photograph of the test setup with the PIC, fiber array and DC electrical probes. The area and location of the PWSM device on PIC is highlighted by the red rectangle.

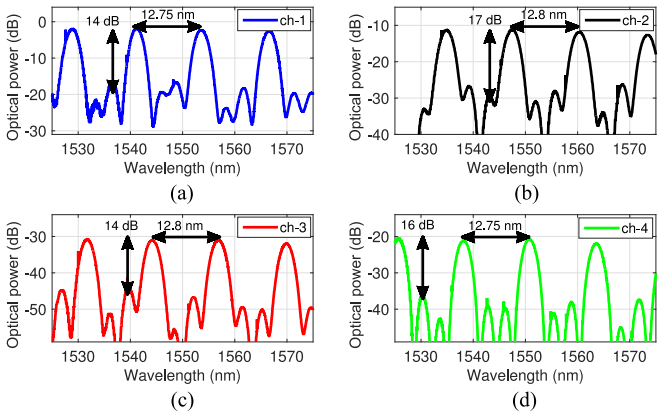


Fig. 6. Normalized transmission response of the four optical output channels (a) *ch-1*, (b) *ch-2*, (c) *ch-3* and (d) *ch-4*.

this figure, the side lobe suppression ratio for *ch-1*, *ch-2*, *ch-3* and *ch-4* are 14 dB, 17 dB, 14 dB and 16 dB, respectively, for a 50 nm wavelength range from 1525 nm to 1575 nm. The free spectral range (FSR) range for *ch-1*, *ch-2*, *ch-3* and *ch-4* are 12.75 nm, 12.8 nm, 12.8 nm and 12.75 nm, respectively. The optical insertion loss in the first channel (*ch-1*) is 1.7 dB at 1553.5 nm. From this figure, it can be seen that there is an insertion loss difference of approximately 9.7 dB between two adjacent channels. This is the incremental loss of an optical

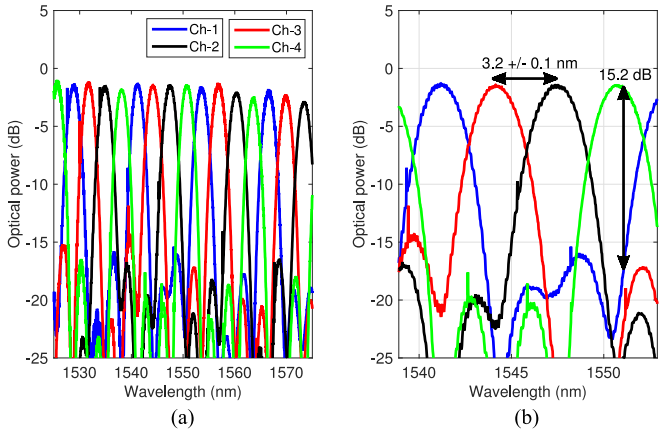


Fig. 7. (a) Overlapped transmission response of the four optical output channels. (b) Zoomed view of the optical response shows 15.2 dB crosstalk for *ch-4*.

delay of 16 ns corresponding to 3.1 dB/m propagation loss in the delays. The insertion loss is 11.4 dB for the second channel (*ch-2*), 20.8 dB for the fourth channel (*ch-4*), and 30.4 dB for the third channel (*ch-3*).

Fig. 7 illustrates the overall optical transmission response of the PWSM device by overlapping the response of each channel removing the additional insertion loss from corresponding delay lines. A narrow spectral response is shown in Fig. 7(b) from 1539 nm to 1553 nm with the transmission peaks of *ch-1*, *ch-2*, *ch-3* and *ch-4* found at 1541.1 nm, 1547.45 nm, 1544.3 nm and 1550.7 nm, respectively. This confirms a wavelength separation of 3.2 nm between *ch-1* and *ch-3*, 3.25 nm between *ch-2* and *ch-4*, and 3.15 nm between *ch-2* and *ch-3*. The FSR and wavelength separation between two channels is within the 0.1 nm range of the simulation results. The result of Fig. 7(b) is used to set wavelength of the four CW lasers within a wavelength range from 1541.1 nm to 1550.7 nm to demonstrate the proposed PWSM operation.

B. Time Delay Between Adjacent Channels

The operation of the PWSM process is demonstrated by constructing a 200 byte long serial packet (1,600 bits) from four 50 byte long packets (400 bits). Full serialization and deserialization of the whole 200 byte long packet require simultaneous operations of two different PWSM photonic circuits, where each of the PWSM circuit performs wavelength to time delay mapping in a complementary manner. As one version of the PWSM circuit was designed, the 50-byte long four WDM packets to a 200-byte long serial packet conversion process is demonstrated in this paper. To demonstrate the concept, each of the four WDM channels is modulated by a 200-byte long electrical signal, where the first 50 bytes contain data and the remaining 150 bytes are set to zero. The first 50 bytes or 400 bits contain three sets of $2^7 - 1$ PRBS bits and nineteen trailing zeros. The last 1200 bits of each data packets are set to zero. The PWSM circuit receives four WDM channels, where each of the WDM channel contains 50-byte long data at the same time segment. At the output of the PWSM circuit, four WDM channels are

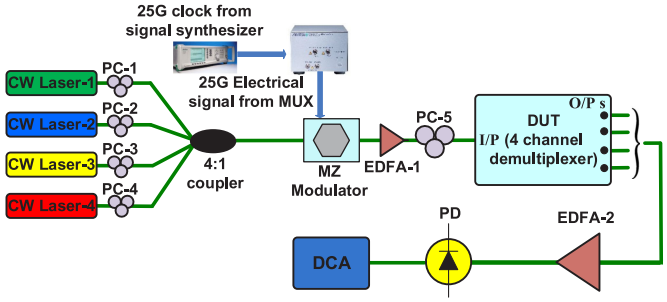


Fig. 8. Experimental setup to capture pattern locked data for each of the four channels separately. EDFA: Erbium doped fiber amplifier, PC: polarization controller, VOA: variable optical attenuator, PD: photodetector, DCA: digital communication analyzer.

simultaneously filtered, time delayed and multiplexed to form a 200-byte long data packet.

In Fig. 8, the experiment set up used to check the time delay between the adjacent WDM channels is shown. Four laser sources emitting continuous-wave (CW) light at wavelengths of 1541.1 nm, 1544.3 nm, 1547.45 nm, and 1550.7 nm are set with an optical power of 12 dBm per channel. The wavelengths of the CW signal are chosen such that they are aligned with the transmission power peaks of the four channel optical demultiplexer section of the PWSM device (Fig. 7(b)). The channels are multiplexed onto a single fiber with a 4:1 multiplexer and modulated simultaneously with a 33 GHz bandwidth lithium niobate amplitude modulator at 25 Gb/s. The optical multiplexer has 6.2 dB insertion loss. The extinction ratio of the optical modulator is approximately 14 dB. The extinction ratio of the polarization sensitive modulator is maximized for each individual wavelength by using polarization controllers prior to the 4:1 multiplexer. In this demonstration, the modulator is driven by an amplified bit sequence, representing one 200 byte long packet, generated at 25 Gb/s by a programmable pattern generator. The simultaneously modulated optical wavelengths are amplified by an EDFA (EDFA-1) and launched into the demultiplexing input port of the PWSM device. The optical output signals from each of the four optical output ports of the PWSM circuit are coupled to a single mode fiber one at a time. A second EDFA (EDFA-2) is used before the photodetector to compensate for the insertion loss of the PWSM circuit. As each of the channels has different optical losses due to the different delay lengths, the optical power amplification in the two EDFAs is set accordingly.

Fig. 9(a) to (d) shows the pattern locked data (one set of 1600 bits captured from 86100D Infiniium DCA) for each of the output channels (*ch-1* to *ch-4*), and the corresponding time delay between the adjacent channels. To accurately measure the time delay between channels, the last bit's transition of each of the received signal is shown at the right. The measured time delay between adjacent channels is within 16.010 ns $\pm$ 5 ps. Thus, the time delay offset between the adjacent channels is accurate within $\pm$5 ps (or $\pm$0.125UI at 25 Gb/s).

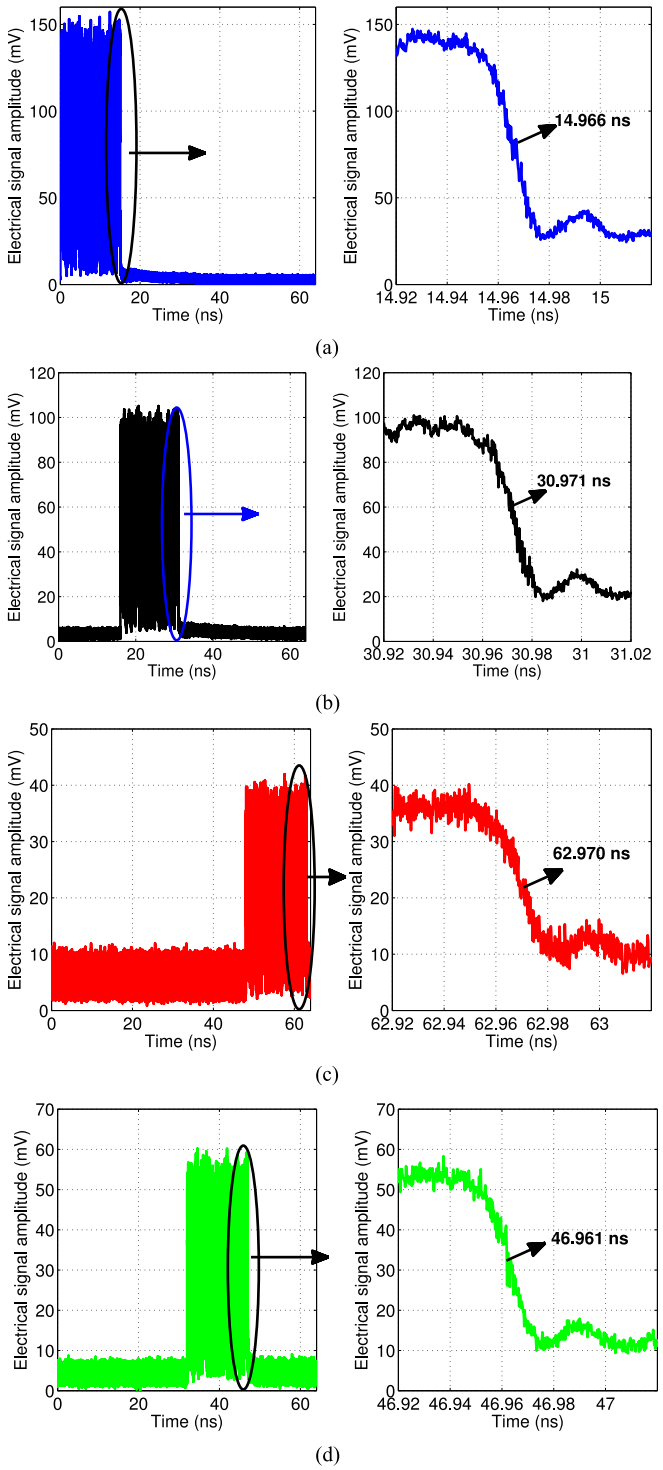


Fig. 9. 64 ns (200 bytes) long patterned locked data and the corresponding time delay for (a) *ch-1*, (b) *ch-2*, (c) *ch-3* and (d) *ch-4*.

C. Parallel-to-Serial Conversion Validation

In this section, we present the experimental method of parallel-to-serialization of the four data segments using the PWSM device. The reconstructed 200-byte serial data should be 64 ns long where each of the channel's bit information is contained within each of the 16 ns long block. Fig. 10 shows the experiment set up to validate the 200-byte long data packet from the four 50-byte long data packets. In this setup, an additional 4:1 optical coupler is inserted after the first EDFA (EDFA-1). The 4:1 optical coupler equally divides the optical power of the

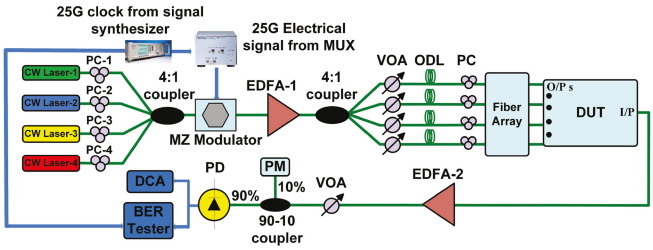


Fig. 10. Experimental setup to reconstruct the 64 ns long packet and to evaluate the BER performance of the PWSM device. PC: polarization controller, EDFA: Erbium doped fiber amplifier, VOA: variable optical attenuator, PM: power meter, PD: photodetector, DCA: digital communication analyzer.

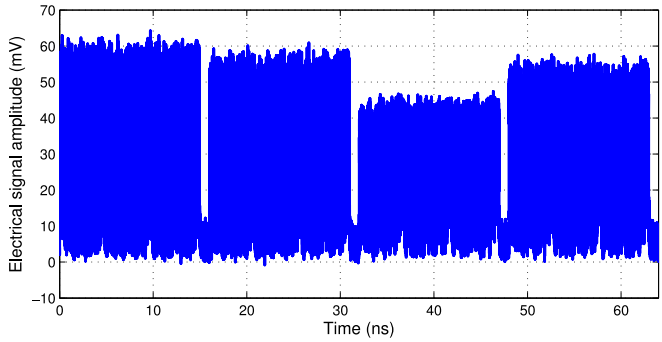


Fig. 11. Reconstructed 64 ns long packet at the output of the PWSM device from four wavelengths (λ_1 to λ_4) each carrying a 16 ns long segment of the data.

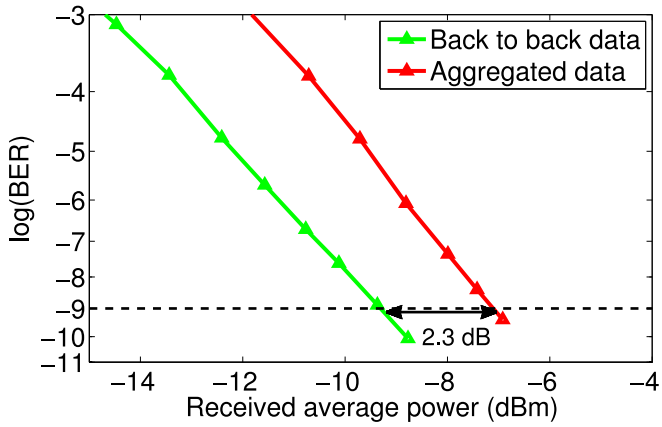


Fig. 12. Measured BER and power penalty of the 64 ns aggregated packet generated from the PWSM output with respect to the back to back generated single 64 ns long data.

signal to its four optical port. As such, each of the four optical output ports of the coupler carries all four WDM signals. The PWSM chip is designed to demultiplex a single WDM channel from each of its four input ports, and then multiplex the four channels at its output port. The delay lines inside the PWSM circuit subsequently add 16 ns delay between the adjacent channels. A fiber array with 250 μm pitch is used to simultaneously couple the four signals to the four input ports of the PWSM device. Variable optical attenuators (VOA) are used to attenuate the optical power of the channels suffering less optical loss compared to the other wavelength channels, *i.e.*, *ch-1* suffers 9.7 dB less loss than *ch-2* inside the PWSM device. Using the VOA, the optical power of the WDM channels is adjusted up to a certain limit such that the whole packet formed by the PWSM chip can be amplified using the second EDFA (EDFA-2). Polarization controllers are used before each channel of the PWSM chip. External optical delay lines (ODL) are used to compensate time delay mismatch occurred due to the small fiber length difference in the VOA, PC and fiber arrays of the adjacent channels. To compensate for the insertion loss of the device under test (DUT), a second (EDFA-2) with 5 dB noise figure is used after the chip. A variable optical attenuator is used to control the received optical power by the commercial photodetector to measure BER performance of the PWSM device in terms of the average received power at the photodetector. A 90/10 optical coupler and a power meter is used after the VOA to measure the average received power. As discussed in section II-A, in a complete PWSM based network [10], two PWSM devices in the transmitter and receiver nodes would remove the optical power non-uniformity due to the complementary oriented optical delay waveguides. In such a scenario, the optical power coupler used after the EDFA-1 in Fig. 10 would be replaced by a wavelength multiplexer integrated on the PWSM device. An AWG based optical multiplexer demonstrated using the similar Si_3N_4 waveguide based platform in [17] can be integrated with the PWSM circuit for this purpose.

Fig. 11 shows the recorded patterned locked electrical data packet from the DCA. The 64 ns long data packet contains four 16 ns block of data from the four WDM optical channels. The electrical peak to peak voltage swing varies at every 16 ns time duration as each of the four channels suffers different optical loss in the PWSM device. However, as mentioned in the above paragraph, the peak to peak voltage difference between the packet segments are reduced by using a separate optical attenuation for each channel.

The bit error rate of the constructed packet is measured after the photodetector. Since the transmitted data from the PPG and received data are different (Figs. 9 and 11), the expected 200-byte long data pattern is loaded onto the BER tester, which contains four repeated blocks of the transmitted bit patterns from the PPG. Both the PPG and BER tester are synchronized to the same clock signal from a clock synthesizer module such that the BER tester is synchronized to the PPG. Fig. 12 shows the BER of the received packet with respect to the average received power at the photodetector. The BER of the photonic link with the PWSM device is compared with a back-to-back case, where the whole 64 ns packet (four segments of 16 ns data) is used to modulate the first wavelength channel only. From the BER result in Fig. 12, a 2.3 dB power penalty is observed for the PWSM interface. The power penalty can be attributed to the uneven peak to peak voltage, time delay mismatch and varying extinction ratio of the four wavelength channels across the full 64 ns packet generated from the PWSM device (as shown in Fig. 11).

To obtain a BER performance below 1×10^{-9}, the experimental testbed requires more optical power amplification from EDFA-2 at the output of the PIC, due to the losses observed on *ch-2*, *ch-3* and *ch-4*. The optical power budget is optimized for

the best BER performance by adjusting the attenuator and both EDFAs (EDFA-1 and EDFA-2). In such context, the amplification of EDFA-2 (model: pritel-FA-20) reached its highest gain limit of 18 dB and more amplification from the EDFAs would have likely lead to lower BER measurements. Consequently, the average received optical power at the photodetector is limited to –7 dBm which provides a BER of 1×10^{-9}.

IV. Discussion

A four channel PWSM device is designed in this work using the low-loss Si_3N_4 waveguide and a 64 ns long data packet is constructed from four 16 ns long packets.

In the experimental setups, a polarization controller (PC) is used before the PWSM chip to reduce the polarization dependent loss of the Si_3N_4 waveguide, inherently polarization sensitive due to its high aspect ratio in the cross-section area. The high aspect ratio cross-section area is necessary to achieve low propagation loss in the waveguide [13]. The simulation result presented in [18] suggests that Si_3N_4 waveguide with larger cross-section area can be used to couple both TE and TM modes to the chip. At lower core waveguide cross-section area (*i.e.*, 100 nm $\times$ 2 μm) in the Si_3N_4 waveguide, the TM mode has higher bending loss (0.1 dB/cm at 8 mm bending radius) compared to the TE mode (negligible bending loss at $>$ 2 mm bending radius) increasing the minimum bending radius [18]. Therefore, beyond the minimum bending constraint, by increasing the core waveguide cross-section area (*i.e.*, 100 nm $\times$ 4 μm) both TE and TM modes can be coupled to the Si_3N_4 waveguide.

The AWG based filter on the low-loss Si_3N_4 waveguide platform proposed in [17] has lower crosstalk (30 dB) compared to crosstalk of the demultiplexer (15.2 dB) demonstrated in this work. However, the MZI based demultiplexer allows simultaneously filtering and time delaying of the optical channels with respect to their adjacent channels, which is important for the proposed wavelength-striped mapping device demonstrated in this work. For example, the integrated delay line (ΔL_3) in the PWSM device (Fig. 1) is utilized to delay both $ch-3$ and $ch-4$ by 32 ns, which reduces the footprint area of the PWSM device. In an AWG filter based PWSM device, on the other hand, two separate time delay blocks of 32 ns and 48 ns would be required for $ch-3$ and $ch-4$ increasing the footprint of the PWSM device. Another approach to decrease the crosstalk is to use a cascaded or lattice MZI based filter architecture, which improves the crosstalk between channels to approximately 20 dB in high index contrast silicon waveguide based demultiplexers [19]. In this work, we have not implemented the lattice architecture based demultiplexer so to minimize the footprint of the circuit. However, in the future designs, lattice-based MZI demultiplexer should be considered to reduce the crosstalk between the channels.

In the experimental setup, EDFAs are used to compensate for the insertion loss of the delay waveguides. In practical applications such as in data centers, semiconductor optical amplifiers (SOA) can be integrated within the PWSM device to provide the necessary optical amplification [20]–[22]. For example, a flip-chip process integration of SOAs onto silica-based waveguides has been demonstrated in [23] leading the path to the feasibility of a hybrid integration of the SOAs within the Si_3N_4 waveguide based PICs. To compensate for the insertion loss of the three channels ($ch-2$, $ch-3$ and $ch-4$) with delay lines, three SOAs would be needed. The power consumption of a SOA providing sufficient gain can easily be a few hundreds of mW (*e.g.*, 455 mW for 14 dB in [22]) leading to a non-trivial total power consumption of over 1 W for the proposed PWSM device. As such, it becomes key to decrease the insertion loss of the delay waveguides for practical applications. One possible approach is using the Si_3N_4 waveguide demonstrated in [24], with 0.5 dB/m propagation loss. The insertion loss of the longest delay waveguide can then be reduced to 4.8 dB leading to lower power consumption from the integrated SOAs and scalability, *i.e.*, to increase the number of channels from four to eight.

In [11], a theoretical model of the eight-channel PWSM device based space-time interconnection architecture (STIA) is shown to be more energy efficient than the 10 Gb/sec 48 port Ethernet switch [25]. An eight-channel STIA's power budget includes power consumption by an eight-channel laser array, one modulator driver, one receiver and two SOAs. The two SOAs at the transmitter and receiver links are required to gate the wavelength-striped WDM packets generated by the PWSM device. However, the model of the PWSM device in the STIA is designed with the 0.5 dB/m propagation loss Si_3N_4 waveguides [11]. Therefore, no additional SOAs were needed to compensate for the optical power mismatch among the channels. The integrated PWSM device proposed in this work requires off-chip EDFAs to compensate the optical power mismatch among the channels, which increases the power budget of the experimental setup. The proof of concept of forming a 64 ns long data packet demonstrated in this work will be helpful to design the PWSM device with 0.5 dB/m propagation loss Si_3N_4 waveguides in future.

In this work, the delay lengths of the PWSM device are designed to form a fixed length data packet for 25 Gb/s data rate channels which limit the flexibility of the network in the need of dynamic resource allocation or change in the data rate and traffic patterns. However, the PWSM device itself draws only 5.68 mW power, which is low compared to the active elements such as lasers, modulator drivers, receivers and SOAs. A detailed analysis on the power budget of the PWSM device based STIA switches compared to the Ethernet switches is presented in [1], [11]. At lower traffic or lower level of network utilization, energy consuming active devices such as SOAs in the STIA switch remain in the idle mode, increasing the energy efficiency of the network. At higher traffic levels, the energy consumed by the PWSM device remains constant, and the energy consumed by the SOAs increase linearly with server utilization. Therefore at the expense of network flexibility the STIA based optical switches offer energy efficient and scalable network architecture.

V. Conclusion

The performance results of the four channel PWSM circuit reported in this article suggest that current complexities of

electronic serialization and parallelization of data packet can be done passively in the optical domain. Integrated optical delay lines on low-loss Si_3N_4 waveguide platform facilitate the serializing/deserializing of long length packet on PIC (*i.e.*, 320 bits long packet in [10] vs 1600 bits long packet in this work).

From the experimental result presented in this paper, we find that 9.7 dB loss difference exists between the adjacent optical channels due to the 3.1 dB/m loss in the delay waveguides which can be compensated through optical amplification. This incremental loss difference between the adjacent channels limits the scalability of the PWSM process in terms of the number of channels. However, in [24] ~0.5 dB/m propagation loss in the Si_3N_4 waveguide has been demonstrated by changing the waveguide cross-section (6.5 μm $\times$ 50 nm) and by increasing the minimum bend radius to 9.8 mm with the PECVD top cladding. The Si_3N_4 waveguide based PWSM device proposed in this work is designed adopting a similar fabrication technology used to design the 6.5 μm $\times$ 50 nm cross-section area waveguide exhibiting 0.5 dB/m propagation loss in [24]. Hence, the propagation loss of the integrated delay waveguides can be further reduced by changing the waveguide cross-section geometry and by increasing the bending radius. Such approach would lead to a loss difference between two adjacent channels drastically reduced by more than a factor of six. In other words, the loss of the 16 ns optical delay lines would only be 1.5 dB making the proposed interface a practical solution for optical passive serial-to-WDM and WDM-to-serial process.

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