# Digital Inverse Multiplexing for Transmitters With Symbol Rates Over DAC Bandwidth Limit

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*(Top-Scored Paper)*

***Abstract*—Broadband signal generation technology plays a pivotal role in increasing the data rate of optical transceivers. To overcome the bandwidth limitation of digital-to-analog converters (DACs), techniques that generate a single broadband signal by multiplexing the outputs of multiple DACs in the analog domain have emerged as an early solution. Nonetheless, broadband signals experience impairments due to deviations from the ideal DAC multiplexing process. Utilizing a digital-analog symmetric modelling of the DAC multiplexing process, we propose an all-electronic bandwidth doubling scheme that incorporates an analog multiplexing device (bandwidth doubler) and a novel digital pre-processing scheme called digital inverse multiplexing. This can compensate for signal impairments due to the practical DAC multiplexing process. We confirmed that digital inverse multiplexing with a predistortion function can improve the signal-to-noise ratio by 3.7 dB in 132 Gbaud coherent signals utilizing an indium phosphide-based integrated bandwidth doubler and complementary metal-oxide semiconductor (CMOS) DACs with only 32 GHz bandwidth. With probabilistically-shaped 64- and 144-ary quadrature amplitude modulation signals, we achieved 1.47 Tb/s (11.1 bits/symbol) back-to-back signal generation and detection and 1.42 Tb/s (10.7 bits/symbol) transmission over a 100 km standard single-mode fiber. These results demonstrate the potential of our digital inverse multiplexing scheme to achieve ultra-broadband transmitters.**

***Index Terms*—Bandwidth extension, digital signal processing, digital-to-analog converter (DAC), quadrature amplitude modulation (QAM).**

## I. Introduction

INCREASING the symbol rate is a key strategy for achieving optical transceivers with higher data rates that support the surging rate demands of client signals [1]. Current transceivers that aim to increase the data rate face limitations due to the (generalized) signal-to-noise ratio (SNR), attributed to amplified spontaneous emission noise from optical amplifiers and Kerr-induced nonlinear interference that occurs within optical fibers. Nevertheless, according to the Shannon-Hartley theorem [2], maintaining the SNR while increasing the symbol rate can proportionally improve transmission capacity. This strategy is beneficial for digital coherent systems [3], [4], [5], the main focus of this work, as well as for low-cost intensity-modulation/direct-detection (IM/DD)-based systems [6], [7], [8], irrespective of their transmission distance. Various high data rate experiments have been conducted with symbol rates exceeding 100 Gbaud [3], [4], [5], [6], [7], [8], [9], [10], [11], [12], [13], [14], [15], [16], [17], [18], [19], [20], [21], [22].

One bottleneck of symbol rate is the bandwidth (BW) of the analog-to-digital converters (DACs) at the transmitter. Most commercial coherent transceivers employ complementary metal-oxide semiconductor (CMOS) DACs co-integrated with CMOS digital signal processing (DSP) application-specific integrated circuits (ASICs), and efforts to increase the BW of CMOS DAC are ongoing [15], [16]. In addition, DACs based on silicon germanium (SiGe) Bipolar CMOS (BiCMOS) [3], [4] and indium phosphide (InP) [23] technologies in conjunction with baseband interleaving techniques are also actively researched and hold the promise of higher BW, although we emphasize that the co-integrability advantage of CMOS DACs with DSP ASICs is so important that it has been making the CMOS DACs the primary choice for commercial transceivers.

Simultaneously, as an early solution to overcome the DAC BW limitation, researchers are exploring a method of generating single-carrier broadband signals using multiple sub-DACs [24]. Through digital pre-processing with broadband active analog devices for signal up-conversion to intermediate frequencies, it is possible to multiply the overall DAC BW in proportion to the number of sub-DACs used. This multi-DAC configuration, when integrated with optical front-end modules, can also shorten the electrical wiring over which broadband signals are transmitted, thereby reducing high-frequency losses [18]. Various schemes have been implemented, including those in the electrical domain (digital-preprocessed analog-multiplexed DAC (DP-AM-DAC) [24], digital BW interleaving (DBI) [25], and BW doubler [26]) and in the optical domain (time interleaving [27], frequency

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TABLE I
OVER 100 GBAUD SINGLE-CARRIER ALL-ELECTRONIC COHERENT SIGNAL GENERATION EXPERIMENTS WITH CMOS DACS

| Reference | DAC multiplicity | Multiplication scheme | Band rate [Gbaud] | Net bit rate [Tbit/s] | Information rate [bits/symbol] |
|---|---|---|---|---|---|
| **This work** | **2** | **BW doubler** (InP integrated) | **132** | **1.47** | **11.1** |
| [14] | 2 | BW doubler (InP integrated) | 120 | 1.04 | 8.7 |
| [17] | 2 | DP-AM-DAC (InP integrated) | 144 | 1.14 | 7.9 |
| [21] | 3 | DBI (discrete) | 200 | 1.58 | 7.9 |
| [9] | 1 | - | 100 | 1.16 | 11.6 |
| [10] | 1 | - | 105 | 1.11 | 10.6 |
| [15] | 1 | - | 138 | 1.00 | 7.2 |
| [16] | 1 | - | 140 | 1.00 | 7.1 |

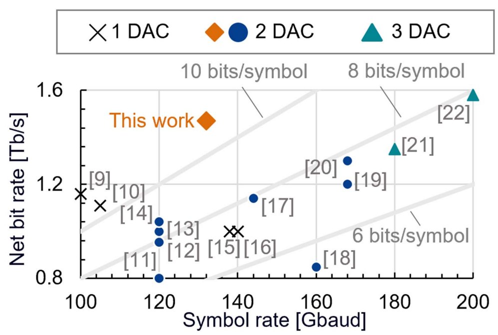



Fig. 1. Recent demonstration of >100Gbaud and >800 Gb/s all-electronic coherent signal generation demonstration with CMOS DACs.

interleaving [28], phase interleaving [29], and carrier-suppressed return-to-zero optical time-division multiplexing [30]). Recent "hero" experiments have demonstrated record single-carrier data rates of 2.52 Tb/s [30] and 2.26 Tb/s [4], relying on optically and electrically multiplexed multi-DAC configurations, respectively.

However, unavoidable deviations from the ideal multiplexing occur during the multiplexing process, resulting in the degradation of signal quality. These impairments include frequency-dependent intensity and phase imbalances between electrical signal lanes, or crosstalk from higher-order harmonic components of the intermediate frequency or the residual DC component. As a benchmark, Table I and Fig. 1 summarize recent demonstrations of all-electronic coherent signal generation over 100 Gbaud and 800 Gb/s based on CMOS DACs (the table shows the results with the highest information rate for each multiplexing scheme). The information rate in terms of bits/symbol is defined as (net bit rate (NBR)) / (symbol rate). In particular, transmitters with BW doublers [11], [12], [13], [14] have demonstrated the transmission with information rates up to 8.7 bits/symbol in wavelength division multiplexing (WDM) transmission [11], [13], [14], and long-haul transmission [11]. On the other hand, conventional single-CMOS-DAC configurations have demonstrated $>$ 100 Gbaud transmission with $>$ 10 bits/symbol. Transceivers employing multiplexed DACs can become more practical by mitigating the impairments due to the multiplexing process and increasing the information rate.

In this paper, as an extension of our recent work presented at the 49th European Conference on Optical Communications (ECOC2023) [31], we introduce a newly developed digital pre-processing scheme called digital inverse multiplexing for transmitters employing BW doublers. We show that through digital-analog symmetric modeling of the multiplexing process, a digital pre-distortion (DPD) function can be "naturally" integrated into the entire multiplexing process, compensating for the complicated frequency-dependent imbalance and crosstalk during analog multiplexing. We have demonstrated 132-Gbaud signal generation using 32-GHz BW CMOS DACs and BW doublers. Extending our work [31], we also demonstrated entropy-optimized 64- and 144-ary probabilistically-shaped (PS) quadrature amplitude modulation (QAM) signal generation and transmission on a fiber link to show the full potential of our method. A back-to-back NBR of 1.47 Tb/s (11.1 bits/symbol) and a 100 km transmission of 1.42 Tb/s (10.7 bits/symbol) were achieved with our method, showing simultaneous improvement in symbol rate and information rate compared with demonstrations using the same BW doublers [11], [12], [13], [14]. Notably, these information rates are comparable with those of state-of-the-art high-symbol-rate demonstrations using a conventional single-CMOS-DAC configuration [9], [10].

The remainder of this paper is as follows: Section II provides a principle of digital-analog symmetric implementation of the BW doubler with digital inverse multiplexing. Section III presents the experimental setup and results. Section IV concludes the paper.

## II. Principle of Digital Inverse Multiplexing

In this section, the principle of digital inverse multiplexing is explained. The multi-DAC configuration requires digital pre-processing that aligns with the multiplexing mechanism of the analog device, and digital inverse multiplexing is one type of such pre-processing designed for the BW doubler device. The BW doubler was initially proposed in a previous study [26], and digital inverse multiplexing shares similarities with the pre-processing presented in that study. The most notable feature of digital inverse multiplexing is that it is formulated to be symmetric with the analog multiplexing process, which makes it easy to embed the DPD in it, as explained in the following.

Fig. 2 shows an overall picture of the DAC BW multiplexing model used in this study. Suppose assuming the aim is to generate a real signal $s(t)$ as the output. Let the BW of the signal be $f_{B/2}$ (when the signal is a Nyquist-shaped single-carrier signal, $f_{B/2} \simeq B/2$ with the symbol rate B.) The signal can be either

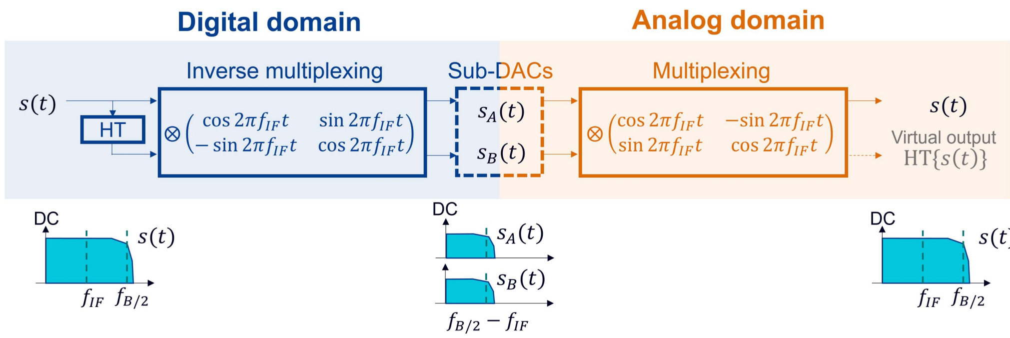



Fig. 2. Principle of BW doubler incorporating digital inverse processing.

in-phase (I) /quadrature (Q) components of a coherent signal or an IM signal.

We define real signals $s_A(t)$ and $s_B(t)$ as

$$\begin{pmatrix} s_A(t)\\ s_B(t)\end{pmatrix} = \begin{pmatrix}\cos 2\pi f_{IF}t & \sin 2\pi f_{IF}t\\ -\sin 2\pi f_{IF}t & \cos 2\pi f_{IF}t\end{pmatrix}\begin{pmatrix} s(t)\\ \mathrm{HT}\{s(t)\}\end{pmatrix}, \tag{1}$$

where $f_{IF} > 0$ is arbitrary intermediate frequency, and HT is the Hilbert transformation that satisfies

$$FT\ \{\mathrm{HT}\{s(t)\}\} = \begin{cases} is'(f) & (f<0)\\ 0 & (f=0)\\ -is'(f) & (f>0)\end{cases}, \tag{2}$$

with Fourier transformation $\mathrm{FT}\{s(t)\} = s'(f)$. By their definition, $s_A(t)$ and $s_B(t)$ satisfy

$$\begin{aligned} s_A(t) &= \frac{e^{i2\pi f_{IF}t}}{2}\left(s(t) - i\mathrm{HT}\{s(t)\}\right)\\ &\quad + \frac{e^{-i2\pi f_{IF}t}}{2}\left(s(t) + i\mathrm{HT}\{s(t)\}\right)\\ s_B(t) &= \frac{e^{i2\pi f_{IF}t}}{2}\left(is(t) + \mathrm{HT}\{s(t)\}\right)\\ &\quad + \frac{e^{-i2\pi f_{IF}t}}{2}\left(-is(t) + \mathrm{HT}\{s(t)\}\right). \end{aligned} \tag{3}$$

As can be confirmed from the definition of the Hilbert transform (2), the high-frequency components cancel each other, so $s_A(t)$ and $s_B(t)$ have a BW of $|f_{B/2}/2 - f_{IF}| + f_{B/2}/2$ reduced from $f_{B/2}$. With $f_{IF} = f_{B/2}/2$ , it has the minimum BW $f_{B/2}/2$.

As the inverse equation of (1),

$$\begin{pmatrix} s(t)\\ \mathrm{HT}\{s(t)\}\end{pmatrix} = \begin{pmatrix}\cos 2\pi f_{IF}t & -\sin 2\pi f_{IF}t\\ \sin 2\pi f_{IF}t & \cos 2\pi f_{IF}t\end{pmatrix}\begin{pmatrix} s_A(t)\\ s_B(t)\end{pmatrix} \tag{4}$$

is valid. Thus, it is possible to recover $s(t)$ from $s_A(t)$ and $s_B(t)$. In the ideal operation of this multi-DAC configuration, (1) is computed in the digital domain ("digital inverse multiplexing"), the BW-reduced $s_A(t)$ and $s_B(t)$ are converted to electrical signals using sub-DACs, and then the first row of (4): $s\ (t) = s_A\ (t)\cos 2\pi f_{IF}t - s_B(t)\sin 2\pi f_{IF}t$ is achieved using specialized analog devices to regenerate $s(t)$ ("analog multiplexing"). Note that, as one can see from (4), this scheme can be interpreted as IQ modulation in radio frequencies, so it is also called RF-IQM in several publications [32]. In the following, $f_{IF} = f_{B/2}/2$ is used to obtain the maximum DAC BW extension. We would also like to mention that (4) can be rewritten as

$$\begin{pmatrix} s(t)\\ \mathrm{HT}\{s(t)\}\end{pmatrix} = \begin{pmatrix}1 & 0 & 0 & -1\\ 0 & 1 & 1 & 0\end{pmatrix}\begin{pmatrix} s_A(t)\cos 2\pi f_{IF}t\\ s_A(t)\sin 2\pi f_{IF}t\\ s_B(t)\cos 2\pi f_{IF}t\\ s_B(t)\sin 2\pi f_{IF}t\end{pmatrix}, \tag{5}$$

which will be used later.

To achieve the multiplexing process (4), the BW doubler device, whose schematic is shown in Fig. 3(a), has been developed, which consists of two high-speed linear selectors known as analog multiplexers (AMUX). By inputting $s_A(t)$ and $-s_A(t)$ to the AMUX, $s_A(t)$ undergoes square-wave modulation, so it becomes $(4/\pi)s_A(t)\cos\omega_{IF}t + (4/3\pi)\cos 3\omega_{IF}t + \cdots$. The third- and higher-order components are strongly attenuated since they are usually out of the device's BW, and only $(4/\pi)s_A(t)\cos\omega_{IF}t$ remains. With the $\pi/2$ phase shift of the trigger, a signal proportional to $s_B(t)\sin\omega_{IF}t$ is generated as well in another branch, and these are combined by a combiner to produce $s(t)$. The device is fabricated using indium phosphide heterojunction bipolar transistor (InP-HBT) technology [26], [33]. The chip size of the IC is 2 × 2 $\mathrm{mm}^2$ and power consumption is 1.05 W under a supply voltage −4.5 V. The metal package size of the IC is 13.6 × 13.6 × 5 $\mathrm{mm}^3$.

In the actual device, the following deviations from ideal operation can mainly occur. The first is the frequency-dependent phase and intensity imbalance between $s_A(t)\cos\omega_{IF}t$ and $s_B(t)\sin\omega_{IF}t$. The second is the imbalance between $s_A(t)$ and $-s_A(t)$, or $s_B(t)$ and $-s_B(t)$. The third is the DC component, or second harmonic component that can occur in the AMUX. The final is the signal reflections that occur at the RF interfaces. Note that frequency-independent phase imbalances include skew between each electrical lane.

The first and final deviation factors correspond with unexpected components such as $s_A(t)\sin 2\pi f_{IF}t$, $s_B(t)\cos 2\pi f_{IF}t$ being mixed into the signal with memory. This can be generalized to the crosstalk of components including

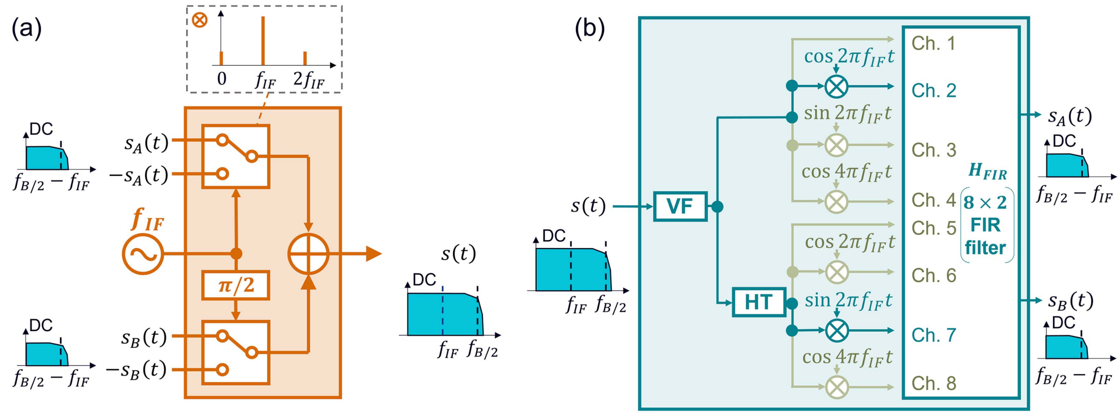



Fig. 3. Schematic representations of analog/digital signal processing. (a) Analog multiplexing with bandwidth doubler. (b) Digital inverse multiplexing.

$s_A(t)$, $s_B(t)$, $s_A(t)\cos 4\pi f_{IF}t$, $s_B(t)\cos 4\pi f_{IF}t$, etc., encompassing all other factors. With the aforementioned considerations, (5) can be generalized as:

$$\begin{pmatrix} s(t) \\ \mathrm{HT}\{s(t)\} \end{pmatrix} = H_{MUX} * \begin{pmatrix} s_A(t) \\ s_A(t)\cos 2\pi f_{IF}t \\ s_A(t)\sin 2\pi f_{IF}t \\ s_A(t)\cos 4\pi f_{IF}t \\ \vdots \\ s_B(t) \\ s_B(t)\cos 2\pi f_{IF}t \\ s_B(t)\sin 2\pi f_{IF}t \\ s_B(t)\cos 4\pi f_{IF}t \\ \vdots \end{pmatrix}, \quad (6)$$

where $H_{MUX}$ denotes the impulse response matrix of the device and $*$ denotes the convolution operation. To ensure the symmetry of the input and output vectors of (6), it can further be generalized as:

$$\begin{pmatrix} s(t) \\ s(t)\cos 2\pi f_{IF}t \\ s(t)\sin 2\pi f_{IF}t \\ s(t)\cos 4\pi f_{IF}t \\ \vdots \\ \mathrm{HT}\{s(t)\} \\ \mathrm{HT}\{s(t)\}\cos 2\pi f_{IF}t \\ \mathrm{HT}\{s(t)\}\sin 2\pi f_{IF}t \\ \mathrm{HT}\{s(t)\}\cos 4\pi f_{IF}t \\ \vdots \end{pmatrix} = H'_{MUX} * \begin{pmatrix} s_A(t) \\ s_A(t)\cos 2\pi f_{IF}t \\ s_A(t)\sin 2\pi f_{IF}t \\ s_A(t)\cos 4\pi f_{IF}t \\ \vdots \\ s_B(t) \\ s_B(t)\cos 2\pi f_{IF}t \\ s_B(t)\sin 2\pi f_{IF}t \\ s_B(t)\cos 4\pi f_{IF}t \\ \vdots \end{pmatrix}, \quad (7)$$

where $H'_{MUX}$ denotes the generalized impulse response matrix.

To address the impairments, we can extend digital inverse multiplexing to include the inverse process of the deviation; in other words, we can embed a DPD in digital inverse multiplexing to equalize $H'_{MUX}$ by implementing the necessary components of the following equation:

$$\begin{pmatrix} s_A(t) \\ s_A(t)\cos 2\pi f_{IF}t \\ s_A(t)\sin 2\pi f_{IF}t \\ s_A(t)\cos 4\pi f_{IF}t \\ \vdots \\ s_B(t) \\ s_B(t)\cos 2\pi f_{IF}t \\ s_B(t)\sin 2\pi f_{IF}t \\ s_B(t)\cos 4\pi f_{IF}t \\ \vdots \end{pmatrix} = H_{MUX}^{-1'} * \begin{pmatrix} s(t) \\ s(t)\cos 2\pi f_{IF}t \\ s(t)\sin 2\pi f_{IF}t \\ s(t)\cos 4\pi f_{IF}t \\ \vdots \\ \mathrm{HT}\{s(t)\} \\ \mathrm{HT}\{s(t)\}\cos 2\pi f_{IF}t \\ \mathrm{HT}\{s(t)\}\sin 2\pi f_{IF}t \\ \mathrm{HT}\{s(t)\}\cos 4\pi f_{IF}t \\ \vdots \end{pmatrix}, \quad (8)$$

where $H_{MUX}^{-1'} = FT^{-1}(FT(H'_{MUX})^{-1})$.

Fig. 3(b) shows the DPD-embedded digital inverse processing. Here, we assume a sampling rate of 1 sample/symbol pre-processing. Also, the sampling rate is assumed to be $B$ with $f_{IF} = f_{B/2}/2$ . This configuration contains a Hilbert transformation, a static $8 \times 2$ multiple-input/multiple-output (MIMO) finite impulse response (FIR) filter, and a Volterra filter (VF) [34]. Before being inputted to the FIR filter, the signal is multiplied by factors of 1, $\cos 2\pi f_{IF}t$, $\sin 2\pi f_{IF}t$, $\cos 4\pi f_{IF}t$. These multiplication factors correspond with the crosstalk components previously described, and the overall working of the FIR filter can be described as

$$\begin{pmatrix} s_A(t) \\ s_B(t) \end{pmatrix} = H_{FIR} * \begin{pmatrix} s(t) \\ s(t)\cos 2\pi f_{IF}t \\ s(t)\sin 2\pi f_{IF}t \\ s(t)\cos 4\pi f_{IF}t \\ \mathrm{HT}\{s(t)\} \\ \mathrm{HT}\{s(t)\}\cos 2\pi f_{IF}t \\ \mathrm{HT}\{s(t)\}\sin 2\pi f_{IF}t \\ \mathrm{HT}\{s(t)\}\cos 4\pi f_{IF}t \end{pmatrix}. \quad (9)$$

Here, $H_{FIR}$ is the impulse response matrix of the FIR filter, which approximates the corresponding components of $H_{MUX}^{-1'}$. The sufficiency of these inputs is discussed in Appendix A. The optimal tap number of the filter should be determined for the system, since it strongly depends on the response of the system, especially on the timescale over which signal reflections in the

RF interface signal in the electric circuit occur. Components of $H_{FIR}$ can be determined using least-squares fitting with known transmitted and received signals, similar to conventional DPDs [34].

The drift of the RF clock frequency $f_{IF}$ must be much smaller than the finest spectral features of the Fourier-transformed impulse responses of the device $FT(H_{MUX})$ to prevent the performance degradation, since the drift, which is the frequency shift of the components on the right-hand side of (6), leads to a mismatch between the signal characteristics and the DPD. It will be necessary to implement electrical stabilization techniques for the clock signal generator, such as electrical phase-locked loops synchronized to an internal reference oscillator. Recalibration of the filter will also be required when the performance degradation occurs.

The VF is also used to compensate for remaining nonlinearity that impose penalties on the multiplexed $s(t)$ and cannot be compensated for by the FIR filter, such as intensity saturation. The memory length of the VF should be determined based on the target performance (reach, rate, etc.), degree of nonlinearity, and computational complexity. Note that compensation for residual nonlinearity can be achieved through means other than VF, such as low-complexity look-up tables [35].

A comparison of our digital inverse multiplexing-embedded DPD with a similar work proposed for a multi-DAC configuration (DBI) [36] is as follows: First, our configuration can compensate for DC and second-harmonic components, which cannot be treated by the previous method. Second, the previous work showed its feasibility in the numerical simulation, in contrast to our work showing the experimental results shown later in this paper.

## III. Experiment

In this section, we describe a demonstration experiment of the proposed method. Here, BW doubler-based analog multiplexing in conjunction with digital inverse multiplexing is used to generate a coherent signal using two band doublers to produce a 132 Gbaud signal.

### A. Experimental Setup

The experimental system is described in Fig. 3(a). Here, the signal is first processed by digital inverse multiplexing in DSP on the transmit side; the VF is a 1 sample/symbol 3rd-order VF with memory lengths of 21, 15, and 9. These relatively large lengths are chosen to demonstrate high-accuracy nonlinearity compensation. The frame length is 264000. The signal is Nyquist-shaped with a roll-off factor of 0.01. A 4-ch CMOS-based arbitrary waveform generator (AWG) with a sampling rate of 96 GSa/s and a BW of 32 GHz is used as the sub-DACs. $s_A(t)$ and $s_B(t)$ are resampled and fed into the AWG. The electrical signals from the AWG are converted to 132 Gbaud with two BW doublers [26], [33] corresponding to I and Q signals, respectively. Note that the BW doubler (64 GHz bandwidth) used in this experiment are identical to those used in previous experiments [11], [12], [13], [14], [26], [33]. In this experiment, the clock for the BW doubler ( $f_{IF}$= 33 GHz) was generated by DACs of another 96 GSa/s AWG containing a frequency-stabilizing phase-locked loop and synchronized with the AWG for signal generation. The frequency of the signal light from a laser diode (LD) is 194.0 THz, and the signal is modulated by a lithium-niobate based IQ modulator (IQM) with a bandwidth of 22 GHz. After modulation, the signal is amplified by an erbium-doped fiber amplifier (EDFA). In the experiments described in Section III-C, polarization division multiplexing (PDM) is emulated by a polarization maintaining delay-line and a polarization beam combiner. In this experiment, wavelength-selective-switch-based optical equalization (OEQ) [37] is used to roughly compensate for the frequency response of the transmitter. At the receiver side, the signal is amplified by another EDFA, and the signal is received by a 256 GSample/s oscilloscope with a bandwidth of 110 GHz. In this experiment, we implemented both self-homodyne and intradyne configurations: we used self-homodyne reception for the experiments described in Section III-B, and to test the proposed method under more realistic transmission conditions, we used intradyne reception for the experiments described in Section III-C. The received signal is demodulated in the DSP using an 8 $\times$ 2 frequency domain adaptive MIMO equalizer (AEQ) [38], which takes the received chromatic dispersion-compensated I/Q signals and their complex conjugates as inputs to accurately compensate for transceiver IQ impairments such as IQ skew. It is important to note that this MIMO AEQ at the receiver-side DSP should not be confused with the FIR filter implementing $H_{FIR}$ within the proposed digital inverse multiplexing (shown in Fig. 2(b)) at the transmitter-side DSP. The carrier frequency/phase is estimated using a digital phase-locked loop with pilot symbols. For the evaluation of the bit rate performance of the system with entropy and code-rate optimization [39], rate-adaptive coding [39], [40] with punctuation of QAM is assumed and processed offline [41] to evaluate the signal quality including the NBR. DVB-S2 low-density parity check code [42] with a puncturing method is used for soft-decision forward error correction (FEC). The code rate of 0.9922 and bit error rate threshold of 5e-5 are assumed for the outer hard-decision FEC [43]. The pilot overhead is 1.64%. The NBR is calculated from the FEC code rate, and the achievable bit rate (ABR) is calculated from the normalized generalized mutual information (NGMI) of the demodulated signal, as

$$C = B\frac{H_{4D}-2(1-R)\log_2 M}{1+P_{pilot}/100}, \tag{10}$$

where $H_{4D}$ is the signal 4D entropy, R is the code rate or NGMI, M is the constellation size before constellation truncation [44], and $P_{pilot}$ is the pilot overhead. The log-likelihood ratios of the demodulated signals were calculated by a bit-metric decoder [45] to carry out decoding or evaluate NGMI.

### B. Verifying Digital Inverse Multiplexing

We experimentally verify the operation of digital inverse multiplexing without the VF. First, the FIR filter implementing $H_{FIR}$within the proposed digital inverse multiplexing was operated by varying the tap number from 1001 to 6001 to determine the optimal one. We used single-polarization 16 QAM

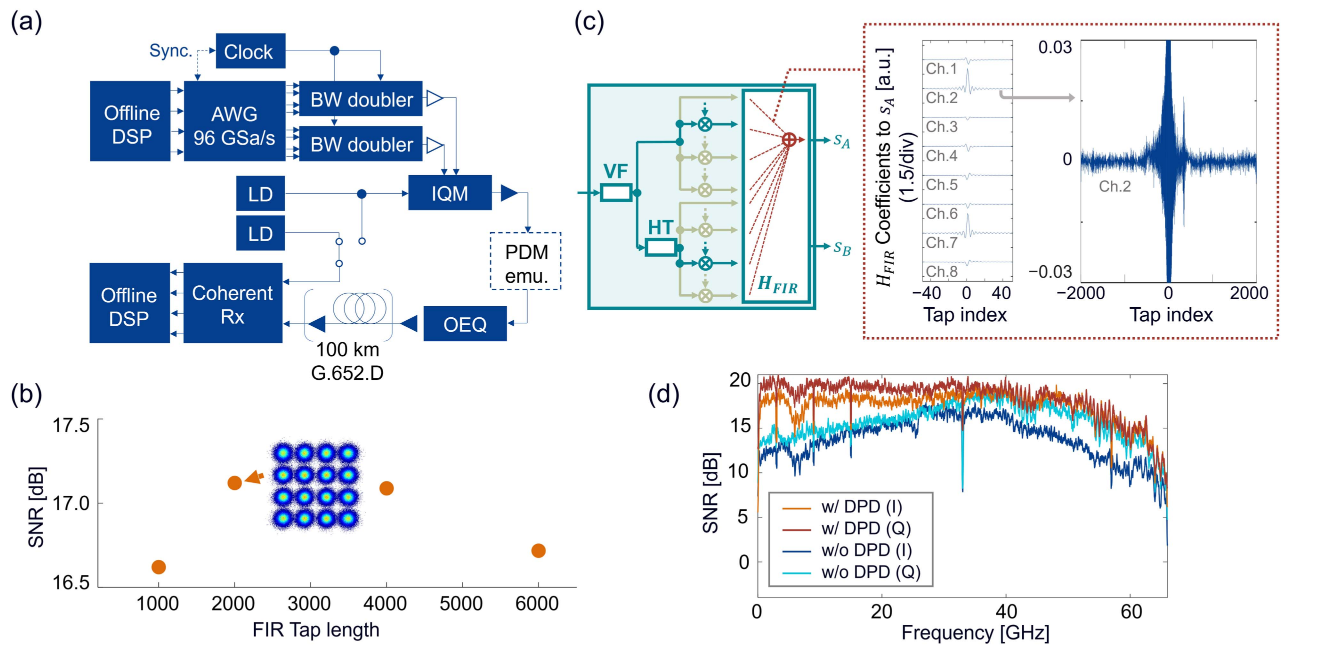


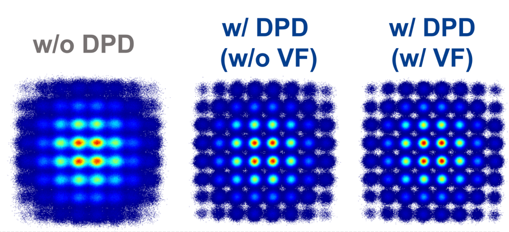

Fig. 4. (a) Experimental setup. (b) Demodulated SNR with various tap number. (c) $H_{FIR}$ coefficients for generating $s_A(t)$ at tap number 4001. (d) Frequency-resolved SNR.

as the signal format. The demodulated SNR of the signals for each tap number is shown in Fig. 4(b). The best performance was obtained at tap number 2001. As an example, the $H_{FIR}$ coefficients for generating $s_A(t)$ at tap number 4001 are shown in Fig. 4(c)(correspondences between the channel number and the input signals are shown in Fig. 3(b)). The use of finite signals to determine tap coefficients results in fitting errors that limit the performance of the digital inverse multiplexing. The tap coefficients did not indicate the presence of noticeable signal interference beyond 1000 taps from the centerburst. In this case, the optimal tap number was 2001, where the fitting error and the filter time width are balanced. The optimal tap number can be shorter in carefully designed transmitter systems with smaller signal reflections.

The frequency-resolved SNR at tap number 2001 is also shown in Fig. 4(d). For comparison, we generated signals without the DPD function by setting the $H_{FIR}$ coefficients of Chs. 2 and 7 as impulse shape, and those of all other channels as zero. Note that the SNR in the low-frequency region is low without the DPD. It can be attributed to interference components $s_A(t)$ and $s_B(t)$ in (6), as indicated by the finite amplitude of tap coefficients of Chs. 1 and 5 in Fig.4(c). The SNR increased at almost all frequencies with the DPD, including the low-frequency region, by compensating for the signal interference, as indicated by the tap coefficients.

### C. Entropy-Optimized QAM Signal Generation and 100-km Transmission

Next, we generated the PDM PS signals. First, we used the PS-64 QAM format and set the signal entropy per 4D symbol to 10.57. Fig. 5 shows the results for three cases: without DPD, with DPD using only the FIR filter $H_{FIR}$, and with the FIR filter $H_{FIR}$ and VF. To avoid the effect of overfitting of the signal pattern, the coefficients of the VF are determined using independent PS-64QAM signals with an entropy of 10.57. The demodulated SNR is improved by 3.0 dB without VF reflecting thanks to the FIR filter $H_{FIR}$ of digital inverse multiplexing. Also, 3.7 dB SNR improvement is confirmed with the VF, demonstrating its effectiveness in mitigating the impact of residual nonlinear impairments. This SNR improvement resulted in an increased NBR by 180 Gb/s with VF, which corresponds to approximately a 16% improvement in NBR. Note that the asymmetry of the "without DPD" constellation in the vertical and horizontal directions is due to the characteristic difference between the two devices, as shown in Fig. 4(d).



| | w/o DPD | w/ DPD (w/o VF) | w/ DPD (w/ VF) |
|---|---|---|---|
| SNR [dB] | 14.30 | 17.33 | 18.05 |
| ABR [Tb/s] | 1.18 | 1.32 | 1.34 |
| NBR [Tb/s] | 1.13 | 1.30 | 1.32 |
| Code rate | 0.8456 | 0.9540 | 0.9664 |

Fig. 5. Results of PS-64 QAM signal generation and detection.

To confirm the full potential of BW doubler with digital inverse multiplexing, signals were generated and received under back-to-back conditions while varying the entropy of PS [39] and reducing the pilot overhead. Here, 64 QAM and 144 QAM were used as the QAM templates; PS-144 QAM was generated by truncation of 256 QAM. In this experiment, the pilot overhead

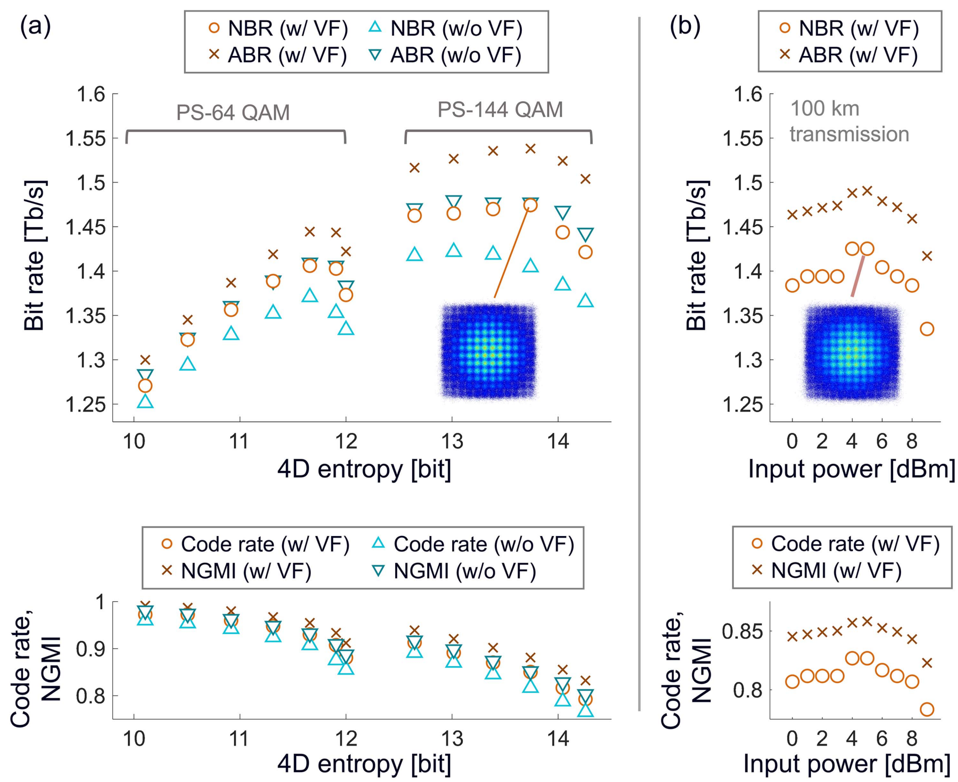



Fig. 6. (a) Back-to-back PS-QAM signal reception results with variable 4D entropy. (b) Results of 100 km signal transmission.

was set to 1.59%. The results are shown in Fig. 6(a). The best NBR of 1.47 Tb/s was achieved when the 4D entropy was 13.73. The code rate in this case was 0.8505. Transmission experiments were also conducted using this modulation format over 100 km of G.652.D fiber. Fig. 6(b) shows the results of transmission while changing the incident power to the fiber from 0 to 8 dBm. Note that the NBR curve shows discontinuity because of the discrete nature of the code rate. Under these conditions, the highest NGMI was obtained at an incident power of 5 dBm, and the net bit rate was 1.42 Tb/s (code rate 0.8268) thanks to the SNR improvement by digital inverse multiplexing. The corresponding information rates were 11.1 bits/symbol (back-to-back) and 10.7 bits/symbol (100 km transmission).

## IV. Conclusion

This paper introduces digital inverse multiplexing, a digital pre-processing scheme for BW doublers. Digital inverse multiplexing is based on the modeling of the inverse process of the BW doubler and can incorporate a DPD function to compensate for signal impairments occurring during the multiplex process. As a demonstration of digital inverse multiplexing with linear and nonlinear DPD function, 132 Gbaud coherent signal generation using 32 GHz CMOS DACs was performed. The results showed that there were a 3.0 dB SNR improvement with linear DPD only, and a 3.7 dB improvement with combined linear and nonlinear DPD. In addition, 1.47 Tb/s back-to-back signal reception and 1.42 Tb/s 100 km signal transmission were demonstrated, showing its superior information rate performance. These results indicate the convincing promise of our scheme as a means of realizing future broadband optical transmitters.

## Appendix A
## Sufficiency of FIR Filter Input Channel

This appendix explains why a set of multiplication factor $\{1,\ \cos 2\pi f_{IF}t,\ \sin 2\pi f_{IF}t,\ \cos 4\pi f_{IF}t\}$ is sufficient for the input of the FIR filter within digital inverse multiplexing in this work. Remembering we assumed a sampling rate that corresponds to 1 sample/symbol and $f_{IF} = f_{B/2}/2 = B/4$, the simplest explanation is as follows: under these assumptions,

$$\begin{cases} \cos[(4N_A+1)\,2\pi f_{IF}\tau] = \cos\,[(4N_A+3)\,2\pi f_{IF}\tau] \\ \quad = \cos 2\pi f_{IF}\tau \\ \cos\,[(4N_A+2)\,2\pi f_{IF}\tau] = \cos 4\pi f_{IF}\tau \\ \cos 8N_A f_{IF}\tau = \ 1 \\ \sin[(4N_A+1)\,2\pi f_{IF}\tau] = \ -\ \sin\,[(4N_A+3)\,2\pi f_{IF}\tau] \\ \quad = \sin 2\pi f_{IF}\tau \\ \sin[(4N_A+2)\,2\pi f_{IF}\tau]\ = \sin 8N_A\pi f_{IF}t = 0 \end{cases} \tag{11}$$

satisfies for all $N_A \in \mathbb{N}$ and ssampling points $\tau = M_A\ \ /B$, where $M_A \in \mathbb{N}$, so multiplication factors $\{1,\ \cos 2\pi f_{IF}t,\ \sin 2\pi f_{IF}t,\ \cos 4\pi f_{IF}t\}$ for each $s_A$ and $s_B$are necessary and sufficient for the compensation for crosstalk between all harmonic components.

Another explanation from the perspective of the frequency domain can also be made. We denote the components of the low-frequency and high-frequency halves of $s_A$ or $s_B$ as $s'_L(f)$ and

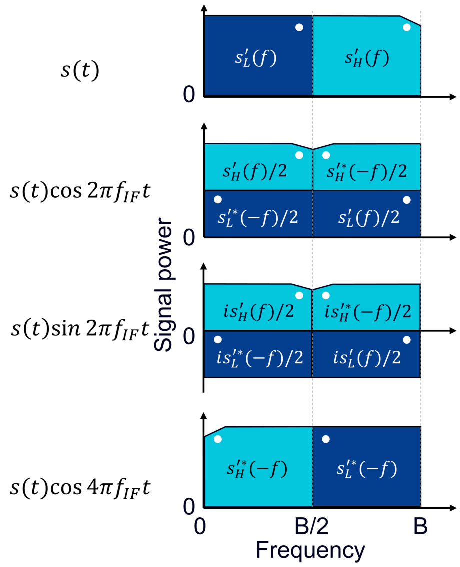



Fig. 7. Frequency-domain representation of input signals to FIR filter of the digital inverse multiplexing.

$s'_H(f)$ as shown in Fig. 7. Taking aliasing into account, $s_A$ or $s_B$ multiplied by each of $\{1, \cos 2\pi f_{IF}t, \sin 2\pi f_{IF}t, \cos 4\pi f_{IF}t\}$ can be illustrated as shown in the figure. Here, asterisks above the symbols denote their complex conjugate. Since both $\{s'_L(f), (s'^*_L(-f) + s'_H(f))/2, i(s'^*_L(-f) - s'_H(f))/2, s'^*_H(-f)\}$ and $\{s'^*_L(-f), (s'_L(f) + s'^*_H(-f))/2, i(s'_L(f) - s'^*_H(-f))/2, s'_L(f)\}$ can be regarded as bases of the linear space spanned by $\{s'_L(f),\ s'_H(f),\ s'^*_L(-f), s'^*_H(-f)\}$, using them as inputs of the FIR filter can compensate the possible linear crosstalk between $s'_L(f),\ s'_H(f),\ s'^*_L(-f)$, and $s'^*_H(-f)$.

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