Broadband 1 x 4 Silicon Nitride Photonic Switch Fabricated on a Hybrid Electrothermal and Electrostatic MEMS Platform

Bruno Barazani, Annabelle Gascon, Cedrik Coia, Frederic Nabki, and Michaël Ménard

***Abstract*—This study demonstrates a monolithic 1 x 4 optical switch composed of a planar micro-electro-mechanical system (MEMS) integrated with silicon nitride (SiN) waveguides. The switching motion is induced by an optimized cascaded chevron electrothermal actuator, which produces an analog, precise, and large stroke for low voltages. Nanoscale displacement measurements show a repeatability on the order of 10 nm and a total switching displacement of $\sim$12 μm for about 10 V. To reduce the insertion losses, a parallel plate electrostatic actuator closes the gap between the waveguides after the switching motion. The optical transmission, measured for 10 devices, is roughly the same across the entire 1520–1620 nm wavelength range. The average optical losses are 4.0 $\pm$ 1.9, 4.4 $\pm$ 2.0, 4.9 $\pm$ 1.9, and 4.1 $\pm$ 1.2 dB for ports 1 to 4 respectively, while the average optical crosstalk is smaller than -35 dB. The relatively compact switch (< 1 mm^2), considering its large displacement, is built on a silicon-on-insulator wafer with a customized fabrication process flow developed by AEPONYX Inc. We believe that this device can lead the way to a new class of small and robust MEMS integrated silicon photonic devices able to operate over a wide wavelength span and to provide a large tuning range for low voltages. Future work will focus on reducing the switch optical losses and on achieving near zero power consumption with the addition of mechanical latches.**

***Index Terms*—Electrothermal actuators, MEMS, optical switch, silicon photonics.**

I. Introduction

SILICON photonics has emerged as one of the most disruptive technologies of the last two decades. The drastic reduction in cost and size achieved through microfabrication are the main reasons for the fast growth of this field [1], [2]. Silicon photonics (SiP) benefits from the well-established physical-chemical processing techniques developed by the semiconductor industry [3]. The main applications of SiP include telecom/datacom [4], sensors [5], light detection and ranging (LiDAR) [6], and neuromorphic computing [7].

In a silicon photonic chip, light travels inside waveguides passing through combinations of splitters, couplers, combiners, and gratings engineered to produce optical devices such as filters, switches, and modulators. The tuning of these devices typically relies on electro-optic (EO) and thermo-optic (TO) effects, which modify the refractive index of the materials forming the waveguide. As summarized in [8], [9], although EO effects are fast, they produce changes of low magnitude, requiring large or resonant photonic structures. TO effects, on the other hand, can provide larger refractive index changes but they have high power consumption and are usually slower. Micro-electro-mechanical systems (MEMS) can provide a much larger tuning range than both EO and TO effects by moving, bending, stretching, and/or compressing waveguides with low power consumption [8], [10], [11]. In addition, MEMS can be integrated with silicon photonics components, forming monolithic optical devices that can operate on wide bandwidths for both light polarizations [12], [13]. Further, these devices can achieve near zero power consumption with the addition of latches or bi-stable structures [14], [15].

Overall, MEMS technology can add value to optical systems through miniaturization, chip integration, precise alignment, and fast responses [16], [17]. In this context, the ever-growing need for fast, compact, low power consumption, and high-radix (i.e., high port count) switching matrices has propelled the development of MEMS-based optical switches. Free-space optical devices composed of 3D MEMS micromirror arrays provide high port count and low losses, but exhibit fabrication and packaging challenges [18], [19], [20], [21]. Integrated MEMS silicon photonics chips can provide much more robust switching solutions. One of the first designs of this kind was a 1 x 2 planar optical switch, where a movable waveguide would bend to butt-couple with two fixed outputs waveguides [13]. The switch was about 2 mm long so that the electrostatic force could bend the suspended waveguide. When in the ON state, the waveguides offset and separation were 2 μm and 5 μm, respectively. Cascaded versions of the same device were implemented [22] as well as versions with latches and different waveguide core materials [23].

In another approach, researchers developed a MEMS phase-shifter that consisted of a Mach-Zehnder interferometer (MZI)

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with a fixed silicon waveguide in one arm and a moving one in the others [24]. A tiny electrostatic comb-drive displaced the movable waveguide to change the optical length of the MZI. The area of the device was smaller than 100 μm^2, and it produced a displacement of 1 μm for an actuation voltage of 31 V. In another demonstration, a 2 x 2 hybrid (not monolithic) optical switch used bi-stable mechanical switching structures to prevent the need of continuously applying a voltage [15]. A pair of electrostatic comb-drives, requiring an actuation voltage larger than 36 V, built in the device layer of a silicon-on-insulator (SOI) wafer, displaced polymer waveguides bonded on the top of a moving platform. A 50 x 50 switch matrix was implemented using evanescent coupling between silicon waveguides [25]. The coupling occurred when a moving waveguide was deflected $\sim$1 μm downwards toward the fixed waveguide by electrostatic actuation at 14 V. An improved version of this switch achieved broadband and a polarization insensitive matrix with a port count of 240 x 240 at the expense of a substantially more complex fabrication process and a total die area of 4 x 4 cm^2 [26], [27]. Recently, our research group demonstrated a crossbar optical switch composed of a rotational platform driven by a circular comb-drive with latches [28]. The SiN waveguides were deposited on top of the MEMS device layer of a SOI wafer in a monolithic stack configuration. A parallel plate actuator reduced the gap between movable and fixed waveguides to minimize the losses. Both switch and gap actuators required voltages larger than 100 V and the total area of the device was $\sim$1 mm^2.

This short summary highlights that the great majority of the MEMS integrated silicon photonic switches utilize electrostatic actuators, which typically rely on high actuation voltages and soft suspensions to achieve large displacements. In a 2D optical switch, this leads to large footprints and out-of-plane misalignments (offsets and tilts). In addition, electrostatic actuators commonly work in a pull-in regime that results in non-tunable digital alignment. Conversely, electrothermal actuators provide high forces at low actuation voltages [29], [30], paving the way for a more compact, robust, and analog switching function with the possibility of achieving large displacements via mechanical amplification [30], [31]. Alternatively, electrothermal actuators can work as phase-shifters by inducing high stress and deformations on the waveguide. Complementary latches and heat sinks can minimize power consumption and temperature increases, respectively.

This work presents the implementation of a 1 x 4 optical switch with a low actuation voltage and a large range of motion provided by an electrothermal actuator with optimized shape and dimensions. The actuator is carved into the device layer of a SOI wafer, onto which SiO_2-SiN-SiO_2 waveguides are deposited and patterned with a customized microfabrication process flow developed by AEPONYX Inc. This stack configuration allows for the separation of mechanical (silicon) and optical (SiN) functions, preventing undesirable compromises between them [28], [32]. Compared to silicon waveguides cladded with SiO_2, waveguides with a SiN core are transparent over a wider wavelength range, from the visible to the mid-infrared, which significantly increases the breadth of their applications [33], [34], [35].

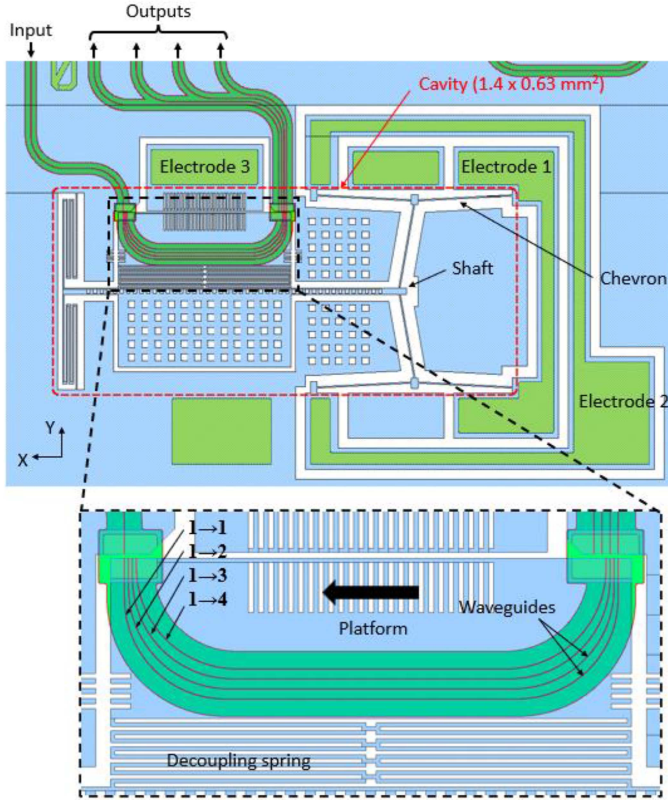


Fig. 1. Layout of the 1 x 4 MEMS optical switch. The platform moves in the X direction to switch to a different configuration: 1→1, 1→2, 1→3, or 1→4. Once the waveguides are aligned, the platform moves in the Y direction to close the gap between them to reduce the optical losses.

Section II of this manuscript describes the mechanical and the optical designs of the 1 x 4 switch. Sections III and IV discuss the fabrication process and testing methodology, respectively. Section V presents the experimental results of the electro-mechanical and optical characterizations. Section IV presents a discussion about the merits of the device and how it can be improved.

II. Design

The 1 x 4 translational optical switch consists of an X-Y MEMS positioner able to support and move optical waveguides with high precision. The MEMS is etched in the device layer of an SOI wafer on the top of a previously defined cavity in the handle part of the wafer, which allows the MEMS to move. The waveguides are formed in a stack of optical layers deposited onto the SOI device layer.

Fig. 1 shows the top view of the MEMS actuator, which moves to the left when electrical current flows through the beams forming the chevrons inducing heat and thermal expansion. The shaft is connected to a platform through a serpentine spring, also referred to as the decoupling spring, which is highly compliant in the Y direction. As the platform moves in the X direction, the set of 4 C-shaped waveguides it carries aligns with the fixed input and output waveguides, implementing the 4 different configurations of the switch, as illustrated in Fig. 2. Note that the pitch

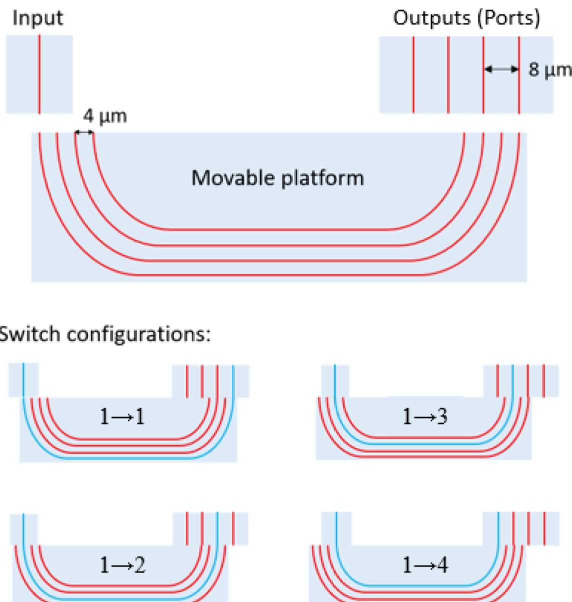
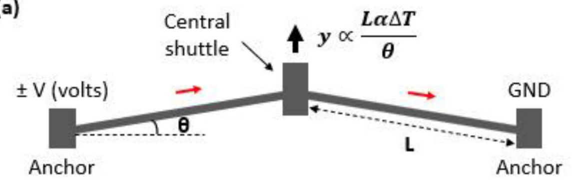
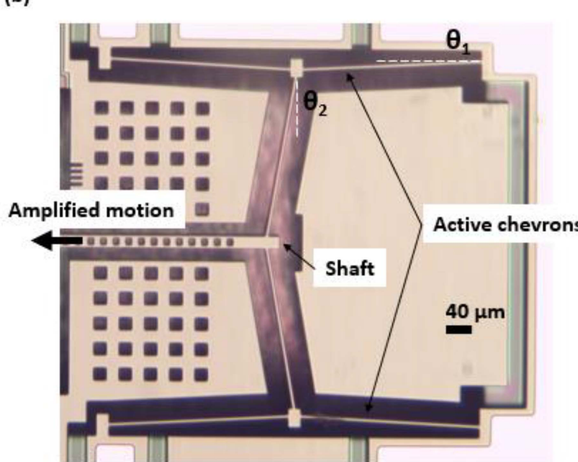


Fig. 2. On top, the switch at the 1→1 configuration with the gap opened. Below, all the switch configurations. The blue line shows the active light path. To achieve the optical coupling at all 4 configurations, the platform needs to travel a total distance of 12 μm.





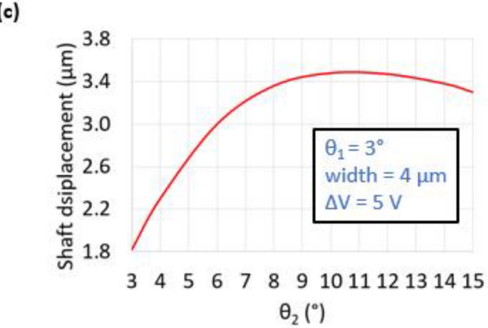


Fig. 3. (a) Schematics of a chevron actuator moving the central shuttle upwards. (b) Microphotograph of the fabricated cascaded chevron actuator composed by two active chevrons linked by a passive chevron amplifier. (c) Displacement of the shaft vs. θ_2 for a voltage difference of 5 V.

between the waveguides is 4 μm since smaller distances could lead to unwanted optical coupling either through evanescent coupling or through stray illumination of adjacent waveguides at the interface between the fixed and the moveable waveguides. Once aligned at one of the configurations, an electrostatic force, generated between the platform and a fixed electrode, pulls the platform along the Y direction, closing the air gap between the waveguides, thus reducing optical losses. During this gap closing action, the motion of the platform is independent of the rest of the MEMS, as all the deformation occurs at the serpentine spring, while the shaft remains still due to its much higher stiffness in the Y direction.

A. MEMS

The 2D MEMS positioner consists of an electrothermal actuator combined with an electrostatic actuator. The entire device fits into a cavity of 1.40 x 0.63 mm^2 and is suspended by 6 anchor points. This section describes both actuators and shows simulation results of their performance.

1) Electrothermal Actuator: The electrothermal actuator is composed of a set of chevron actuators arranged in a configuration that produces large displacements at low voltages. In the chevron actuator (Fig. 3(a)), electrical current flows from one extremity to the other generating heat due to the Joule effect. The temperature increase in the beams of the chevron leads to thermal expansion, which propels the central shuttle. The total distance travelled by the central shuttle is proportional to the length of the beam 'L', the thermal expansion coefficient 'α' of the material, the temperature gradient 'ΔT', and the inverse of the chevron angle '1/θ' [36]. Chevrons actuators are known to provide high force but low displacements [29]. The proposed design consists of two active chevrons, facing each other, connected by a third chevron, which works as a passive mechanical amplifier, as shown in Fig. 3(b). Since the active chevrons are identical and are driven by the same voltage difference (see Fig. 1), they evenly compress the middle chevron, which pushes the shaft of the device to the left. As a result, the cascaded chevrons greatly amplify the motion at the detriment of the force exerted on the shaft.

The dimensions and angles of the chevrons are optimized to maximize the displacement considering the design restrictions. One critical design condition, besides the size of the cavity, is the thickness of the device layer, which is 59 μm to allow the attachment of standard optical fibers (125 μm of diameter) with their centers at the same height of silicon nitride layer. This is because the height of the silicon nitride is approximately 62.2 μm starting from the buried oxide layer, where lies the u-groove cavity. The 62.2 μm is composed of the 59 μm from the device layer plus 3.2 μm from the bottom cladding.

TABLE I
DESIGN PARAMETERS OF THE CASCADED CHEVRON ACTUATOR

Design parameter	Value
Device thickness	59 µm
Beam width	4 µm
θ_1	3°
θ_2	10°
Beam length (active chevrons)	285 µm
Beam length (amplifier chevron)	256 µm

Electro-thermo-mechanical simulations of the chevron actuator, done in COMSOL Multiphysics, show that a smaller beam width leads to higher displacements. However, values smaller than 4 μm can induce buckling instability [37], [38] and may become a challenge for fabrication. Therefore, the width of the beam is fixed at 4 μm while the angle of the active chevrons 'θ_1' is fixed at 3°, as smaller angles could also lead to buckling instability [30]. Finally, as can be seen in Fig. 3(c), sweeping the angle of the chevron amplifier 'θ_2' from 3° to 15° at a constant voltage difference between electrodes 1 and 2 (see Fig. 1), demonstrates that the largest displacement of the shaft occurs for a 'θ_2' of approximately 10°. Table I summarizes the main design parameters of the electrothermal actuator.

After optimization of the dimensions and angles, the actuator was simulated in CoventorMP using the MemMech analysis and electro-thermo-mechanical physics. The values used for the silicon electrical resistivity and internal stress were set as 0.0185 Ω.cm and 15 MPa tensile, respectively. The other silicon properties were taken from the materials database of SOIMUMPs [39], which is a general-purpose process that micromachines MEMS on SOI wafers. All material properties were set as constants.

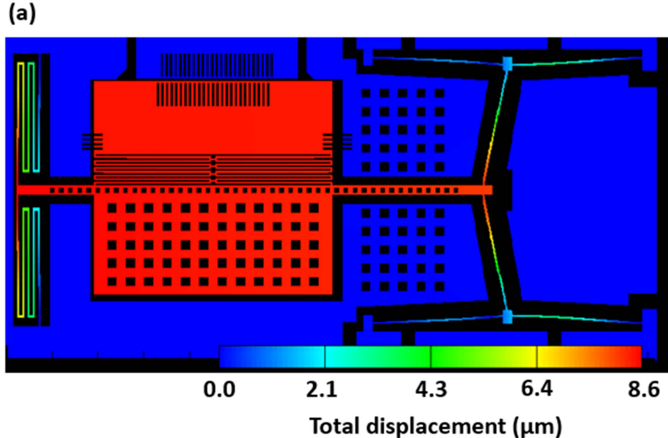
Heat conduction was the only heat transfer mode considered since convection and radiation are known to be negligible at the micro scale for temperatures below 500 °C [30], [36], [40]. Heat conduction through silicon and through air were implemented. The temperature of the silicon around the suspended structure and the external temperature of air below and above the device were set at 20 °C. The top and bottom faces of the device were selected to exchange heat with air. The heat flux equation used to dictate the heat conduction through air is:

$$q = \frac{k_{air}}{L} \left(T_{air} - T \right), \tag{1}$$

where q is the heat flux, $k_{air} = 0.05$ W/(mK) is the thermal conductivity of air, $L = 100$ μm is the air layer thickness, $T_{air} = 20$ °C is the external temperature of air, and T is the temperature at the silicon surface.

Fig. 4(a) presents a color map, with a deformation scale of 1:1, of the simulated total displacement when the applied voltage is 10 V. The image shows an amplified output motion of 8.6 μm to the left, which is fully transferred to the platform. Fig. 4(b) shows the total displacement of the platform as a function of the applied voltage.

Fig. 5(a) presents the temperature color map of the device when a voltage is applied on the chevrons. The maximum



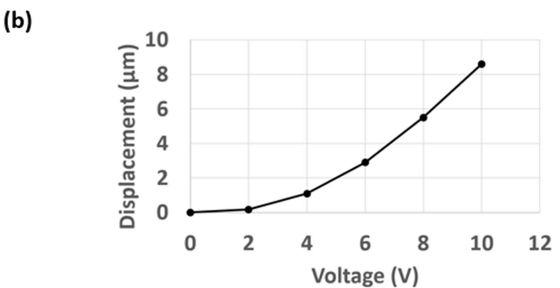
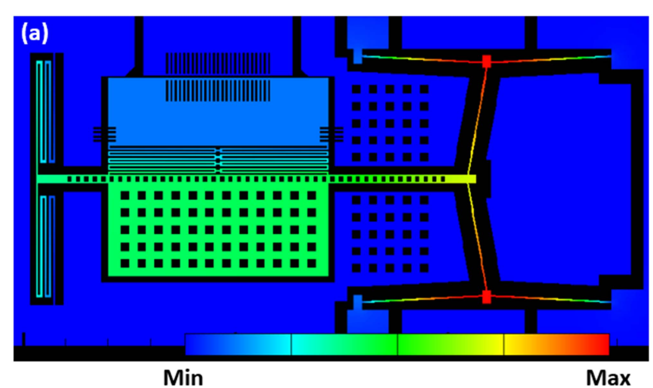


Fig. 4. (a) Color map of the simulated displacement for an input voltage of 10 V at both active chevrons. The deformation scale is 1:1. (b) Total displacement of the platform as a function of the applied voltage.



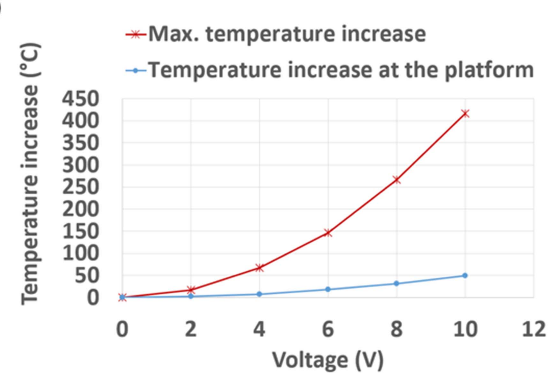


Fig. 5. (a) Color map of the temperature distribution when a voltage difference is applied on the chevrons. (b) Maximum temperature increase, and temperature increase at the platform as a function of the applied voltage.

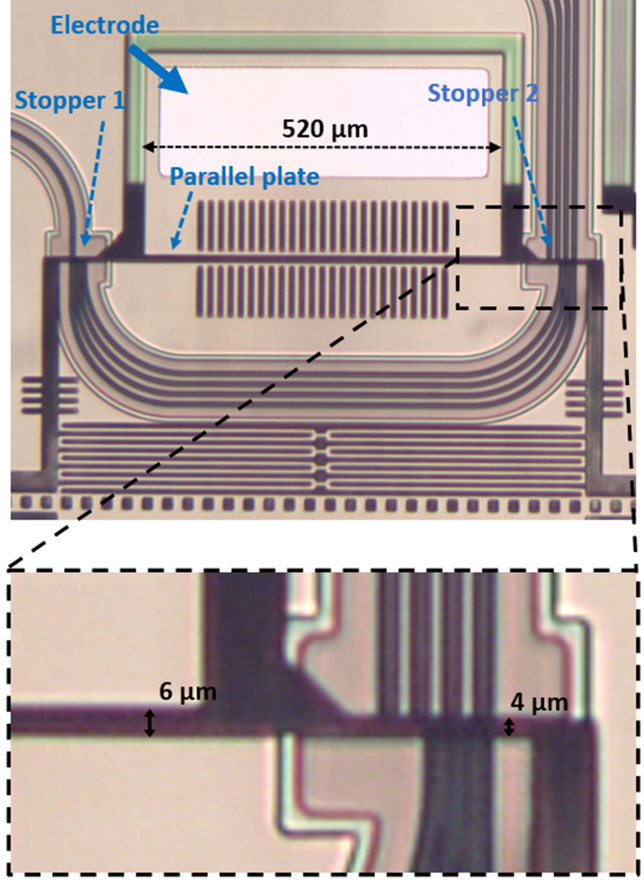


Fig. 6. Micrograph of the fabricated parallel plate electrostatic actuator. The electrostatic force pulls the platform upwards until it collides with the stoppers. In the magnified inset, the electrostatic gap of 6 μm and the stopper gap of 4 μm can be seen.

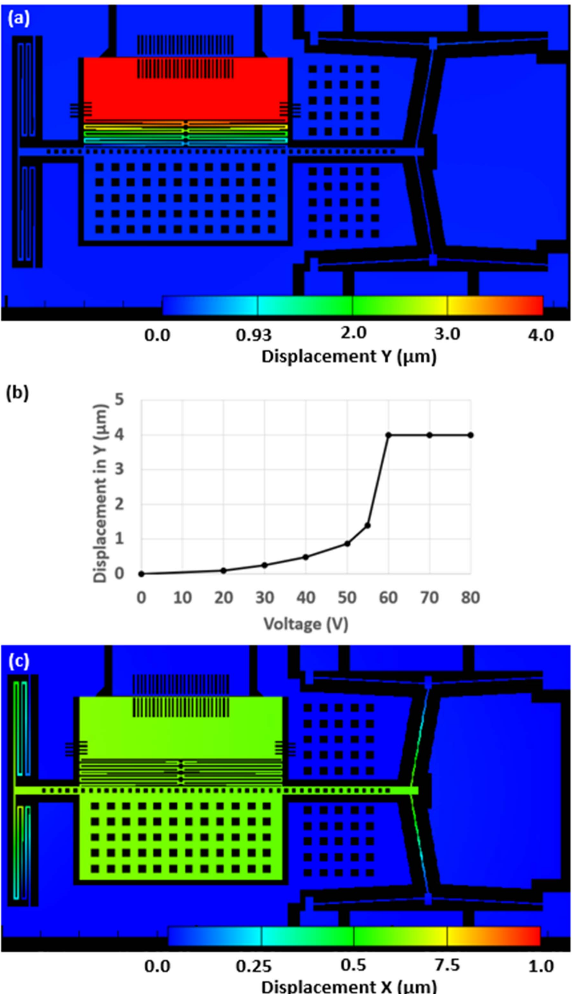


Fig. 7. (a) Color map of the displacement in Y for actuation voltage of 80 V. (b) Displacement in Y of the platform as a function of the applied voltage. (c) Color map of the displacement in X for actuation voltage of 80 V.

temperature occurs at the center of the active chevrons (i.e., the heat sources), while the temperature at the platform (bluish) is close to the external or minimum temperature of the system.

Fig. 5(b) shows the maximum temperature increase and the temperature increase on the platform as a function of the applied voltage. At 10 V, the maximum temperature increase is around 415 °C at the chevrons while the temperature at the platform increases by 50 °C. Note that the large perforated rectangular mass attached to the shaft works as a heat sink whereas the holes reduce the damping and the total mass of the suspended structure.

2) Electrostatic Actuator: The electrostatic actuator consists of a parallel plate capacitor defined by the 59 μm-deep walls of the movable platform and the opposing anchored electrode. An electrostatic gap of 6 μm separates the two electrodes, and two grounded stoppers, lying 4 μm away from the moving platform, prevent direct electrical contact between them, as can be seen in Fig. 6. Note that the ground stoppers are where the waveguides meet i.e., where the optical coupling occurs. This actuator therefore operates in the pull-in regime as the platform snaps to the stoppers when the electrostatic force induces a displacement larger than ~ 2 μm (1/3 of the electrostatic gap). When the platform is pulled-in, the gap is reduced to 0 μm in the optical coupling region, while a 2 μm gap remains between the electrodes.

A large directional compliance is required to prevent misalignments between the waveguides when the gap is closed, i.e., the platform must move only in the Y direction.

To prevent rotation, the serpentine spring that connects the platform to the shaft is designed with a much lower stiffness in the Y direction than that of the structure that connects the shaft to the substrate. The former was designed with an elastic constant of 12 N/m in the Y direction whereas the latter was designed with an elastic constant of 694 N/m in the Y direction. This stiffness ratio of about only 2% implies that the serpentine spring would incur 98% of the total deformation caused by the electrostatic force.

The performance of the actuator was simulated in CoventorMP using the CoSolveEM (coupled electromechanics) analysis. Fig. 7(a) shows a color map with a deformation scale of 1:1 of the simulated displacement in Y when the applied voltage at the electrode is 80 V. The image shows that the platform moves by 4 μm in the Y direction while the rest of the device shows

negligible motion since almost all the deformation in Y occurs in the decoupling spring. Fig. 7(b) shows the Y displacement of the platform as a function of the applied voltage at the electrode while the device is set to the ground potential. The graph shows that the actuator snaps for voltages between 55 and 60 V leading to a complete closure of the gap between the waveguides on the platform and the input/output fixed waveguides. Finally, Fig. 7(c) shows the color map of the simulated X displacement when the applied voltage at the electrode is 80 V. The image indicates a residual platform displacement of about 500 nm to the right.

Although not done in this study, the pull-in voltage could be reduced by adding an extra set of parallel plates actuators at the center of the platform in the middle of the "C" shaped waveguides. Another approach would be to further decrease the stiffness of the decoupling spring by adding an extra set of "H" shaped springs.

B. Optical Circuit

The light travels in single-mode waveguides built with a SiO_2-SiN-SiO_2 (bottom cladding-core-top cladding) optical stack (Fig. 8(a)), which lies on top of the silicon. The optical routing consists of two optical circuits, in which light comes in and out via surface grating couplers (SGCs), as shown in Fig. 8(b). In the main optical circuit, light is inserted into input channels 1 or 2, travels through the MEMS switch, and comes out from one of the four output channels. Note that the two SGC inputs merge at the Y branch resulting in a single input channel at the MEMS switch. The two inputs were implemented because of the fixed pitch of our array of photodetectors, which is twice the distance between the SGCs. Therefore, input 1 is used to measure outputs 1 and 3, while input 2 is used to measure outputs 2 and 4.

In the reference optical circuit, light is inserted into one of the reference input channels and comes out from the reference output channel. The reference optical circuit has a similar length, the same Y branch, and the same number of bends as the main optical circuit and it is used to measure the optical losses of the circuit without the MEMS. Measurements of the optical losses of both optical circuits allow for the de-embedding of the optical losses of the MEMS switch, which occur predominantly in the two optical gaps.

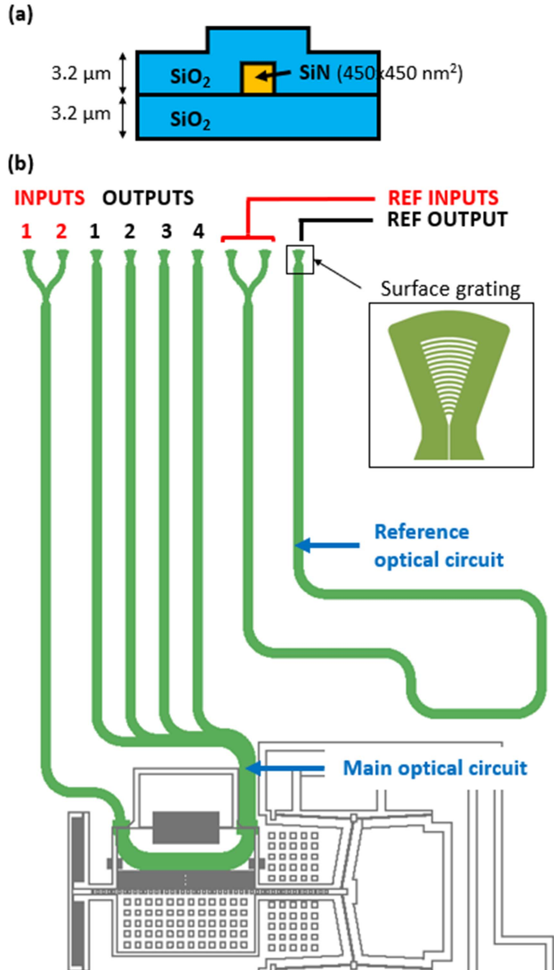


Fig. 8. (a) Waveguide optical stack SiO_2-SiN-SiO_2 and (b) Optical routing composed by a main optical circuit and a reference optical circuit (i.e., having no MEMS). The inset shows a magnified view of the SGC.

III. Materials and Fabrication

The device is fabricated using a custom combination of conventional microfabrication processes such as chemical vapor deposition (CVD), photolithography, wet etching, and plasma etching. The process flow was developed by AEPONYX Inc. using the foundry services and installations of the Collaborative Center for MiQro Innovation (C2MI). The starting material is a silicon-on-insulator (SOI) wafer with prefabricated MEMS cavities etched into the handle layer. The SOI stack comprises a thin buried oxide (BOX) layer of 1 μm sandwiched between a 725 μm thick handle layer and a 59 μm thick device layer. The latter consists of a p-doped silicon with electrical resistivity in the 0.007–0.03 Ω.cm range.

Fig. 9 illustrates the main steps of the fabrication process flow, starting with the formation of the optical stack. First, the bottom clad layer is deposited by low pressure chemical vapor deposition (LPCVD) of tetraethyl orthosilicate (TEOS), followed by a high temperature annealing. The SiN layer is also deposited by LPCVD, where the silicon content has been optimized to provide a good compromise between low propagation losses and low stress. A photoresist is then deposited and patterned with UV lithography. After development, the SiN is etched with reactive ion etching (RIE) to achieve near-vertical sidewall. The top clad is then deposited by plasma enhanced chemical vapor deposition (PECVD) of TEOS. The outer edges of the waveguides are defined by etching the oxide forming the cladding (top and bottom). This step clears the oxide everywhere on the device layer, except over the waveguide cores, which become enclosed by 6 μm of oxide on each side. This reduces the mechanical stress induced by the optical stack on the silicon device layer.

After the patterning of waveguides, an AlCu layer is deposited and patterned into electrical pads for MEMS actuation. Next, another etch step defines the two optical gaps along the MEMS

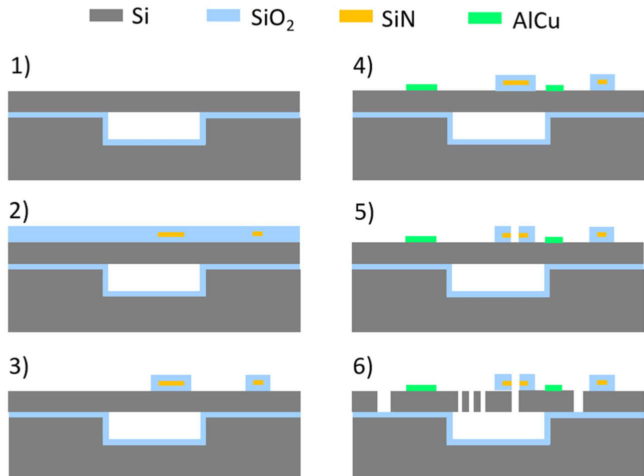


Fig. 9. Main steps of the fabrication flow. 1) SOI wafer with pre-made MEMS cavities. 2) Deposition and patterning of the SiO_2-SiN-SiO_2 optical stack. 3) Definition of the waveguides. 4) Deposition and patterning of the metal pads. 5) Etching of optical gaps. 6) Etching of the device layer to define the MEMS and to electrically isolate the electrodes.

platform while a SiO_2 hard mask protects the MEMS structures and isolates the electrodes. Fig. 10 shows SEM images of the device after fabrication. The image on the top shows the gap between the waveguides from the top while the image on the bottom shows the chevron shuttle from an angle of 15°.

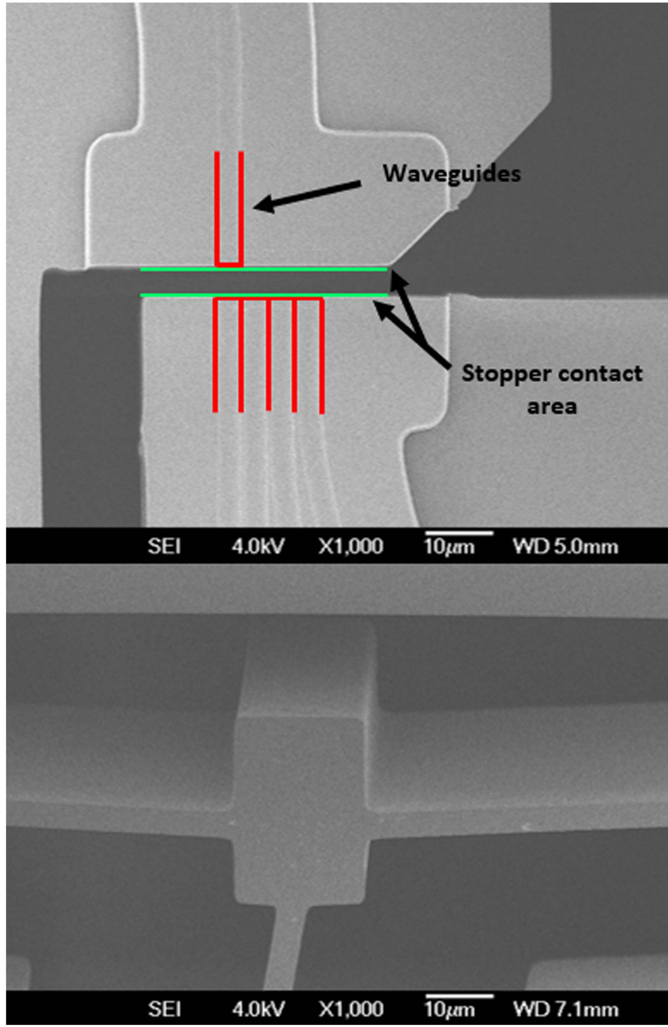


Fig. 10. SEM micrograph from the top of the air gap between waveguides (top), and SEM micrograph with a 15° tilt of the chevron shuttle (bottom).

IV. Test Setups

A. Probe Station

A probe station equipped with 4 probes and a high-resolution camera (Basler Ace2000-340kc) was used to conduct measurements of the electrical resistivity and of steady state displacements. The test setup and the measurements of the electrical resistivity of the wafers can be seen in the Appendix section.

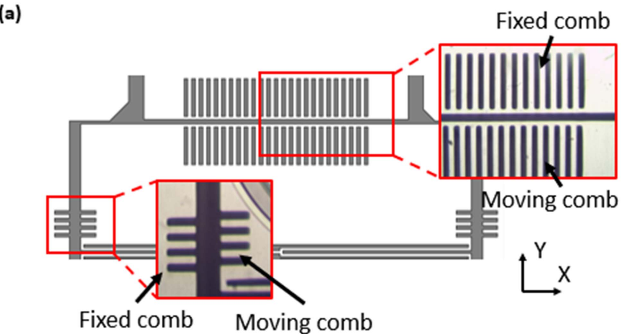
To measure the displacement of the platform as a function of the applied voltage, a Fast Fourier Transform (FFT) algorithm analyzes a sequence of micrographs taken at different actuation voltages. This method was proposed in [41], where measurements of MEMS displacements with sub-nanometer resolution were demonstrated.

Two probes are used to apply a DC voltage to induce motion in the X or in the Y direction (i.e., the X and Y actuators are assessed independently). One of the probes is fixed at ground potential while the electrical potential on the other is increased from zero to 10 V for the chevrons, and from 0 to 75 V for the parallel plate actuator. To obtain the images, the chip is placed under a microscope, equipped with a high-resolution camera. The camera captures images for each voltage increment. To measure the motion of the platform, the microscope is focused on the comb structures, shown in Fig. 11(a), using a magnification of approximately 40x. The combs consist of periodic slits, with a pitch of 10 μm, carved in the silicon device layer. The combs in the center of the platform are used to measure the displacement in the X direction while the combs on the sides of the platform are used to measure the displacement in the Y direction.

Once all the images are captured, the algorithm averages the pixel intensity of all rows parallel to the comb slits in a selected cropped area to generate a 1D periodic signal with a known spatial wavelength of 10 μm, as shown in Fig. 11(b). The FFT, then, finds the phase of the generated signal and calculates the displacement of the structure considering the phase shift from the initial image. The frame motion is eliminated by repeating this procedure for a cropped area at the fixed comb and subtracting this displacement from the one of the moving comb.

B. Photonic Probe Station

A photonic probe station (Maple Leaf Photonics) was used to perform the optical characterization of the photonic device by measuring the optical transmission on the output channels of the switch. An optical signal of 9 dBm passes through a 1 x 2 splitter, enters an optical fiber, and is inserted at the chip with an optical power P_{in}. The input and output optical fibers are positioned at an angle of 30 $\pm$ 5° in relation to the chip and approximately 50 μm above it. In the XY plane, the fibers are aligned on the top of the surface grating couplers



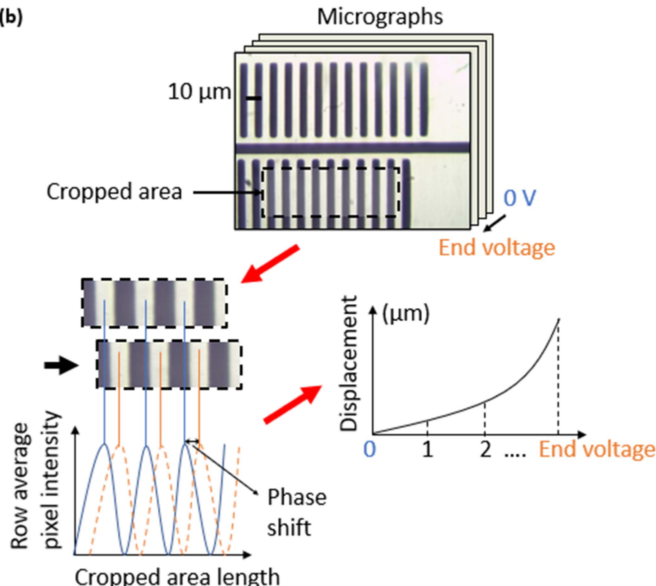


Fig. 11. (a) Comb structures located around the platform and used for optical displacement measurements. (b) The image analysis algorithm generates the pixel intensity profile of the cropped area, finds the phase shift between the images, and calculates the platform displacement.

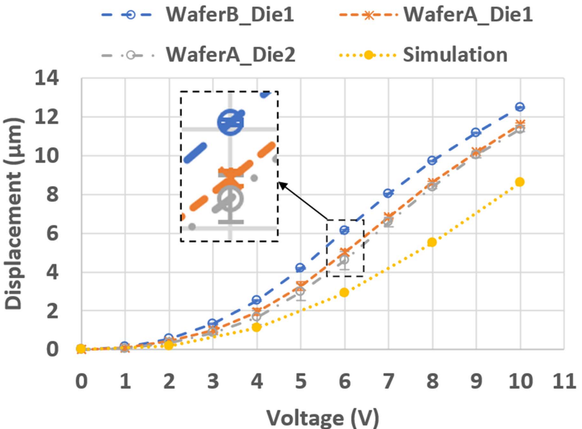


Fig. 12. Displacement in the X direction vs. applied voltage. Each point is an average of 4 measurements, error bars are the standard deviations.

(SGCs), which are used to transfer the optical signal in and out of the waveguides. Photodetectors connected to the output fibers measure the intensity of the optical signal and provide the optical power ratio (P_{out}/P_{in}) in decibels (dB) scale. The test procedure consists of measuring the transmission of the MEMS optical circuit and of the reference optical circuit (Fig. 8(b)) over the wavelength range from 1520 to 1620 nm (185–197 THz). Only light with TM polarization was used as an input signal for these tests. To drive the MEMS, electrical probes were used to apply DC voltages at the MEMS electrodes.

In the X direction, to set a specific switch position, an initial coarse alignment is done considering the displacement vs. voltage calibration measured with the probe station. Then, a fine alignment is conducted by changing the voltage in steps of 0.1 V until the optical power at the output is maximized. In the Y direction, a constant voltage of 80 V (larger than the pull-in voltage) is applied to close the gap between the waveguides.

For each of the 10 devices tested, all switch configurations (see Fig. 2) were measured once with the gap opened and once with the gap closed. To determine the optical crosstalk between the output channels, 6 of the 10 devices had ports 2, 3, and 4 measured when the input signal was aligned with port 1, i.e., in 1→1 configuration. The reference structure was measured one time for each device tested.

V. Experimental Results

A. Electro-Mechanical Characterization

The mechanical characterization assesses the MEMS steady-state response to a DC voltage input. The X and Y motions of the device were measured independently using the probe station. To move the MEMS in the X direction, electrode 2 was set to ground potential, while an electrical potential was applied on electrode 1 (see Fig. 1). To move the MEMS in the Y direction, electrode 2 was set to ground potential, while an electrical potential was applied on electrode 3. Single MEMS devices were tested 4 times, one measurement starting immediately after the other, to check their repeatability. In addition, the MEMS design was tested in 3 different dies from two wafers, labeled A (2 dies) and B (1 die), to assess the impact of fabrication variations on the MEMS performance. Wafers A and B were processed separately.

1) X Direction: Fig. 12 shows the displacement in the X direction (see Fig. 1) vs. applied voltage in the 0–10 V range. Each point on the graph is an average of 4 measurements of a single device, and the error bars (sometimes not visible because of the scale of the graph) are the standard deviations. Each curve in the graph represents the measured data from a specific die on the wafers. The actuator from dies 1 and 2 from wafer A move 11.61 ± 0.07 μm and 11.34 ± 0.01 μm at 10 V, respectively. The actuator from wafer B moves 12.48 ± 0.04 μm at 10 V. The larger displacement of the actuator from wafer B is due to the lower electrical resistivity of the wafer (see the Appendix for a discussion on this topic). Fig. 13 shows micrographs of a MEMS switch when no voltage is applied (top) and when 10 V is applied on electrode 1 to actuate the chevrons (bottom). In the micrograph on the top, the MEMS is in its initial position. In the micrograph on the bottom, the MEMS shaft and the platform

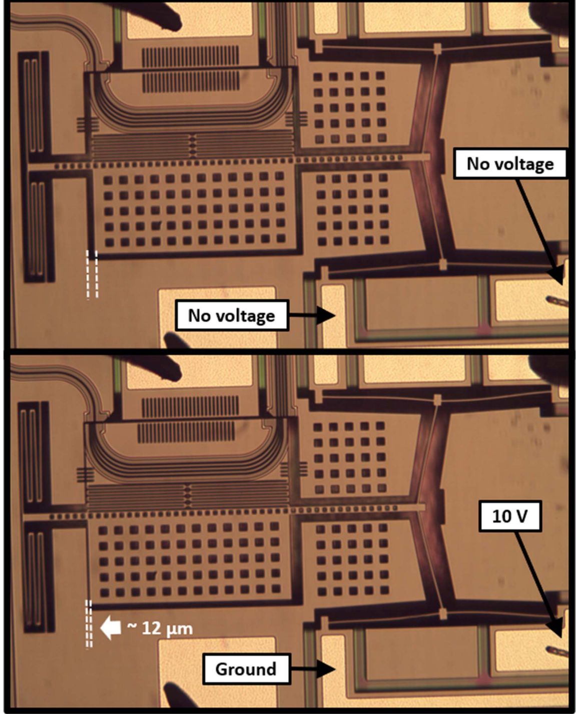


Fig. 13. On the top, micrograph of the switch when no voltage is applied. On the bottom, a micrograph of the switch when a voltage of 10 V is applied to drive the chevrons.

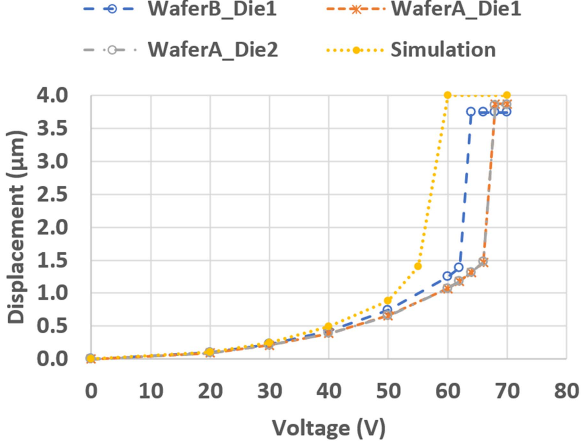


Fig. 14. Displacement of the platform in the Y direction vs. applied voltage. Each point is an average of 4 measurements. The standard deviations, not shown in the graph, are in the order of a few nanometers.

are displaced by approximately 12 μm to the left, resulting in a noticeable deformation of the chevrons and of the spring that connects the shaft to the substrate.

2) Y Direction: Fig. 14 shows the displacement of the platform in the Y direction vs. the applied voltage. Each point on the graph is an average of 4 measurements of a single device. The standard deviations, not shown on the graph, are typically on the order of a few nanometers. The devices measured from wafer A show similar performance as their curves overlap quite well with each other. For those devices, the last measured displacement before the pull-in is 1.47 μm at 66 V. The platform snaps and hits the stopper at 68 V as it moves 3.85 μm. The device measured from wafer B shows a lower pull-in voltage in the 62-64 V range, its last measured displacement before pull-in is 1.39 μm, and the total displacement is 3.75 μm.

B. Optical Characterization

This analysis determines the MEMS switch optical losses and crosstalk for the broad 1520–1620 nm (185–197 THz) wavelength range. The MEMS switch insertion losses are calculated by subtracting the transmission of the main optical circuit from the transmission of the reference optical circuit (see Fig. 8(b)).

A total of 7 devices from wafer A and 3 devices from wafer B were measured. The same MEMS device was measured on each of these dies (different dies from the Electromechanical Characterization). Measurements taken in one die were not repeated. The first batch of measurements was conducted in 4 dies of wafer A. Three months later, 3 dies from wafer A and 3 dies from wafer B were measured. The second batch included transmission measurements for all ports at the 1→1 switch configuration for the calculation of the crosstalk.

1) Optical Transmission and Switch Losses: Fig. 15 shows the raw optical transmission at the output port for each switch configuration (for gap open and for gap closed) and at the output of the reference optical circuit. The curves show the average transmission values of 10 devices and their 10 respective references. The low values of raw transmission, even for the reference circuit without the MEMS switch, are mainly due to the losses of the SGCs. Other sources of losses are the Y branch junction and the propagation losses. The variation of the transmission with the wavelength complies with the fact that the insertion angle was fine-tuned to maximize the transmission at 1580 nm. The transmission oscillations are potentially due to parasitic reflections in the optical circuits.

Fig. 16 shows the average MEMS switch losses of the 10 devices for all 4 configurations along the full 1520–1620 nm wavelength range. The MEMS switch losses are overall flat throughout the full measured spectra, especially when the gap is closed.

Note that the losses are slightly lower for longer wavelengths due to the lower confinement of the optical mode, which leads to higher coupling efficiency across the optical gap. The average losses of each output port when in ON state (aligned and with the gap closed) is in the 3-6 dB range. The average insertion loss in the ON state over the four switch configurations is 4.3 $\pm$ 0.4 dB. Variations of the insertion losses for different ports can be explained by a combination of factors: i) a small angular misalignment between the fiber array and the output SGCs; ii) the limited voltage step of 0.1 V, which may not have been small enough to reach optimal alignment for all ports; iii) the small length variations between the routing waveguides connected to each output port; and iv) the presence of small point defects and/or roughness at the interface between the fixed and moveable waveguides. On average, closing the air gap between the waveguides eliminates approximately 9 dB of insertion loss. Table II summarizes the applied voltages on the actuators and

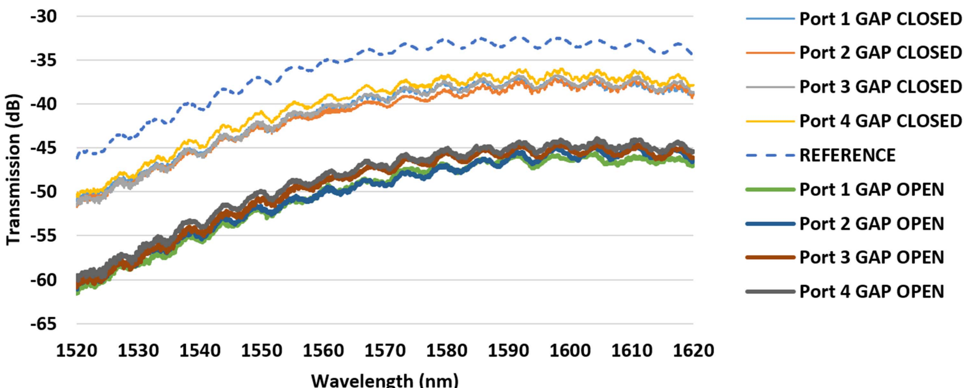


Fig. 15. Optical transmission at the outputs of each switch configuration and of the reference optical circuit (average of 10 devices and 10 reference optical circuits).

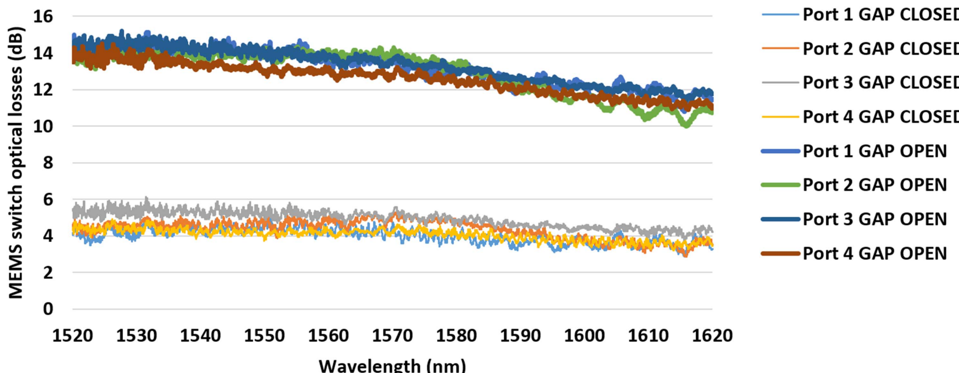


Fig. 16. Normalized losses for each switch port (average of 10 devices).

TABLE II
ACTUATION VOLTAGES AND AVERAGE OPTICAL LOSSES FOR THE FULL SPECTRA FOR EACH SWITCH CONFIGURATION

Configuration	Electrode 1 (ground)	Electrode 2 (chevrons)	Electrode 3 (parallel plate)	Average MEMS insertion losses (dB)
1→1	0 V	0 V	0 V (gap open)	13.2 ± 2.1
			80 V (gap closed)	4.0 ± 1.9
1→2	0 V	5.3 ± 0.1 V (wafer A) 5.2 ± 0.1 V (wafer B)	0 V (gap open)	12.9 ± 1.9
			80 V (gap closed)	4.3 ± 2.0
1→3	0 V	7.5 ± 0.1 (wafer A) 7.2 ± 0.1 (wafer B)	0 V (gap open)	13.3 ± 1.5
			80 (gap closed)	4.9 ± 1.9
1→4	0 V	10.2 ± 0.2 (wafer A) 9.7 ± 0.3 (wafer B)	0 (gap open)	12.6 ± 1.5
			80 (gap closed)	4.1 ± 1.2

the average optical losses across 1520–1620 nm on the output port of each switch configuration.

2) Crosstalk Between Channels: Fig. 17 shows the optical transmission on all ports when the switch is aligned for port 1 (1→1 configuration), and the gap is closed. The data represent the average values for a sample size of 6 MEMS devices (3 from each wafer). Since the noise floor of the equipment is −75 dB, the crosstalk between port 1 and the other ports is on average smaller than −35 dB. Although the crosstalk was not measured for the other switch ports, we expect similar results since the pitch between waveguides is the same for all configurations (see Fig. 2).

VI. DISCUSSION

The challenge in implementing MEMS SiP devices is to find the optimal compromise between precise motion, large displacement, small footprint, and low actuation voltage. Most MEMS integrated optical switches are driven by electrostatic actuators, which are known for low power consumption and fast response; however, they generate small forces, which leads to large actuation voltages even for small displacements, and large footprint to increase the electrostatic force. Therefore, most of these devices show displacements smaller than 5 μm and actuation voltages larger than 10 V [15], [24], [25], [28],

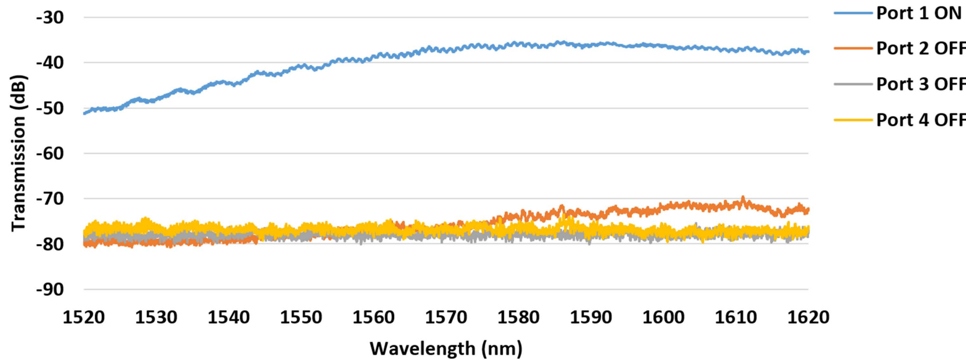


Fig. 17. Optical transmission for all 4 ports, measured simultaneously, when the switch is aligned for port 1, and the gap is closed (average of 6 devices).

[42], [43]. This study shows that it is possible to implement a relatively high radix, low voltage, small, and robust integrated optical switch using electrothermal actuators made with SOI wafers. We have demonstrated up to 12 μm of displacement for actuation voltages as low as 10 V in a $\sim$1 mm^2 footprint.

Another difficulty in the implementation of MEMS SiP devices is to integrate the optical layers to the MEMS process flow, and to cope with the residual stresses that they introduce. These stresses lead to mechanical misalignments [8], which become significant in larger and less stiff suspended structures. We have achieved stable mechanical structures through the removal of the oxide cladding (except over the waveguide) and the use of a stiffer electrothermal actuator for switching.

From a manufacturing point of view, current state-of-art integrated MEMS optical switches that feature a large port count [27] and/or low optical losses [15] rely on a highly complex fabrication flow. The switch from [27] requires 20 photomasks and multiple waveguide layers, resulting in a large matrix that occupies a 4 x 4 cm^2 die. The switch from [15] undergoes a complex wafer bonding step to connect waveguides made of polymer to the MEMS wafer in a hybrid fabrication process. Our switch relies on a monolithic process flow, single waveguide layer, and a total of 6 photomasks, including the one used for the cavities. This results in a switch with simpler process flow that could achieve high port count if laid out in a cascaded configuration.

Concerning insertion losses, 3-6 dB is a better result compared to previous devices proposed by our group. The crossbar [28] and the 1 x 3 [43] switches showed insertion losses of 12–15 dB and 4–6 dB respectively. Other MEMS integrated switches based on butt-coupling waveguides have reported insertion losses below 3.5 dB [13], [15], [22], [23], however, those are not integrated with silicon nitride waveguides. Although this first device demonstration does not provide ideal optical transmission, many adjustments, discussed below, can be made to address this issue.

The gap closing mechanism proved to be greatly effective as it reduced the losses by approximately 9 dB. However, our previous work [43] showed that the etching profile of the optical stack is not perfectly vertical, such that when the gap is closed, the two waveguides are still separated by $\sim$1 μm. Note that despite the resulting added losses, this separation prevents from damaging the waveguide facets when the gap closes. In addition, the optical transmission is affected by the roughness of the sidewalls of the gap. Therefore, improvements in the gap etching recipe to obtain a more vertical angle and lower sidewall roughness should help reduce the optical losses even more. Part of the remaining losses at the gap can also be attributed to out-of-plane misalignments (offset and tilt) [42], [43], which are mainly induced by the residual stresses of the optical layers on the top of the platform. In this context, the thick silicon layer of 59 μm is particularly helpful as it increases the elastic constant in the Z direction. Misalignments in the X or switching direction also increase the losses. Nonetheless, the electrothermal actuator allows analog control of the position in this direction; and therefore, the implementation of a closed loop control of the switching position can potentially suppress this source of loss.

From a design perspective, adjustments on the layout of the spring that anchors the shaft would prevent potential misalignments in X occurring during the gap close actuation according to simulations results shown in Fig. 7(c). In addition, switch solutions with a single gap instead of two could reduce the optical losses by 50%. Furthermore, springs with stiffer designs should help reduce out-of-plane misalignments, which leads to lower losses as well.

With respect to the operation speed, integrated MEMS switches have achieved switching times as low as 0.5 ms [15], 0.4 ms [13], 0.2 ms [23], or even 0.5 μs [23] for non-butt-coupling switches. Note that those switches are not integrated with SiN waveguides. As mentioned before, this fast response is characteristic of electrostatic actuators. However, when the voltage is removed, mechanical oscillations can take several milliseconds to cease due to the low stiffness of the springs. Preliminary measurements done using a vibrometer show that the response time of the switch is dictated by the electrothermal actuator, which provides a steady response in less than 3 ms with no overshoot when heating or cooling.

VII. Conclusion and Future Perspectives

This work presented the design, fabrication, and characterization of a compact SOI 1 x 4 MEMS optical switch that can travel a total distance of 12 μm for an actuation voltage as low as 10 V. The thick mildly doped silicon device layer provides reliable electrothermal actuation, mechanical robustness, and facilitates the alignment of optical fibers for butt coupling. The optimized design geometry, formed by cascaded chevrons, amplifies the switch displacement, and thermally isolates the

heat sources from the waveguides. To reduce optical losses, a parallel plate electrostatic actuator, composed of a spring with large directional compliance, closes the air gap between the movable platform and the input and output waveguides.

Simulation results of the motion of the device and of the temperature profile during actuation were provided. For the switching motion, discrepancies between simulations and measurements could be reduced by implementing temperature dependent silicon properties, especially for the electrical and thermal conductivities. For the gap closing motion, the small shift between simulations and measurements is mainly due to fabrication bias, which affects the separation between the plates forming the electrostatic gap. Nanoscale displacement measurements validate the simulations and allow precise calibration of the performance of the actuators. Measurements of devices from different dies and wafers show their robustness to fabrication variations.

Results from the optical characterization confirm that the switch is functional, repeatable, and provides a flat response for all 4 channels over the broad wavelength range of 1520–1620 nm, which is the largest span that we could measure with our tunable laser. All four switch channels show similar optical losses, which, on average, is 4.3 ± 0.4 dB, whereas the crosstalk between channels is smaller than -35 dB. With over a 100 nm of optical transmission bandwidth, we consider that our device is broadband. Furthermore, since the waveguides are made of silicon nitride and silicon dioxide and that the geometry of the waveguides (i.e., the dimensions of the core and the thickness of the cladding) can be modified without changing the actuators, our design could be readily adapted to operate anywhere from the visible to the mid-infrared.

Future work will focus on the analysis of the topography of the MEMS to investigate the alignment in the vertical direction and possible tilt at the optical gaps, as well as on the transient response of both actuators to evaluate the switch response time. Future designs will target electrothermal switches with only one optical gap, which would lower the optical losses by half. To minimize the power consumption, latch mechanisms could be incorporated to lock the device on a switched configuration. Measurements of the temperature distribution will be done to confirm the simulation results. According to the simulations, the long length of the cascaded electrothermal actuators helps to isolate the heat from the platform. Future design optimizations of the heat sink would allow to completely suppress any heating close to the waveguides.

The proposed design paves the way for a new generation of compact MEMS SiP devices that can provide a large turnability range for low actuation voltages and that are suitable for broadband applications, including visible light. Potential applications include datacenters, telecommunications, and sensors.

Appendix

A. Resistivity Measurements

Fig. 18 shows a micrograph of the electrical structure, located near the MEMS, used to conduct the measurements of the electrical resistivity of the device layer. The probes are placed over the electrical pads in a 4-point-probe configuration that allows measurements of electrical resistance (R) with high precision. Probes A and B input electrical current while probes C and D measure the voltage drop along the silicon block of length L = 100 μm, height H = 59 μm, and width W = 50 μm. Once the electrical resistance of the silicon block is known, it is possible to estimate the electrical resistivity (ρ) of the wafer in the vicinity of the test structure using the equation

$$\rho = R\frac{WH}{L}. \tag{2}$$

Fig. 19. shows the measured voltage as a function of the applied current on the 4-point probe structure on wafers A and B. The measured electrical resistances are numerically equivalent to the slopes of the linear fits, which are 5.2 Ω and 4.7 Ω for wafers A and B, respectively. Therefore, the resistivity of the wafers A and B, which was calculated by using (2) and the layout dimensions of the silicon block, are 0.0185 Ω.cm and 0.0168 Ω.cm, respectively. Note that just one die from each wafer was measured in this test.

The lower resistivity of wafer B leads to a higher current and, consequently, to a higher power consumption for the same applied voltage. Since the displacement of the chevron actuator is directly proportional to the power consumption [36], the actuators from wafer B provide a larger displacement for the same applied voltage, as can be seen in Fig. 12.

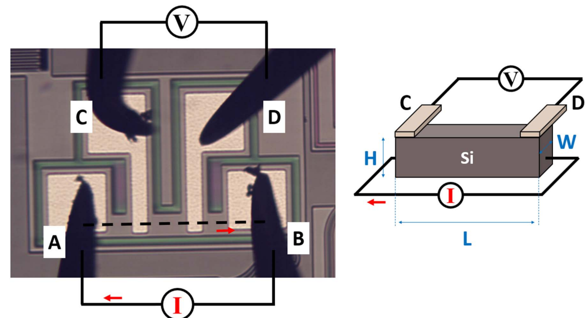


Fig. 18. On the left, micrograph of the 4-point probe structure used for resistivity measurements. On the right, a 3D depiction of the silicon block that causes the voltage drop between the C and D probes.

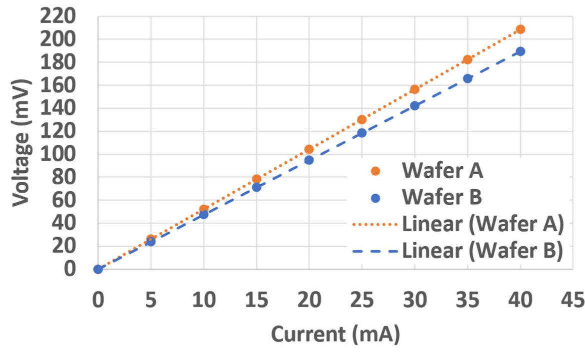


Fig. 19. Measured voltage as a function of the applied current on the 4-point probe structure for wafers A and B.

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