4×100Gb/s PAM4 Multi-Channel Silicon Photonic Chipset With Hybrid Integration of III-V DFB Lasers and Electro-Absorption Modulators

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***Abstract*—A silicon photonic based transmitter and receiver chipset for 4×106Gb/s 400 GBASE-DR4 data rates is presented. Each channel of the transmitter chip reaches high extinction ratio and optical modulation amplitude (OMA) with a low TDECQ penalty in full compliance with the IEEE standard. The receiver chips possess high responsivity with low polarization dependent loss. The use of discrete III-V arrayed components hybridized onto the silicon platform and passive alignment of single-mode fibers provides a low-cost, compact and scalable solution extendable to even higher aggregate rates and channel count.**

***Index Terms*—Silicon photonics, Datacenter, distributed feedback laser (DFB), Electro-absorption modulators (EAM), pulse-amplitdue modulation (PAM)-4.**

I. Introduction

With demand for high-speed optical interconnects in datacenters, high-performance computing and emerging AI/ML applications increasing, cost-effective, compact, and scalable solutions are required. In the past decade, parallelism and bit rate per lane grew the aggregate data rates from 1×10Gb/s to 4×10Gb/s, 4×25Gb/s and recently to 4×100Gb/s and 8×100Gb/s in a single optical module (i.e. QSFP-DD [1] and OSFP [2] form factors). This has been achieved by increasing the baud rate (10, 25 and 50 GBd), the lane count (1,4,8, either through more wavelengths, more fiber channels or both), and changing the modulation format from one bit per symbol (Non-Return-to-Zero (NRZ)) to two bits per symbol (Pulse-Amplitude-Modulation 4 (PAM4)) [3]. To address this growing demand for bandwidth, while maintaining competitive costs, silicon photonic (SiPh) based solutions have been presented using both Mach-Zehnder modulators (MZMs) [4], [5], [6], [7], ring resonators (RR) [8], [9], [10], [11] for transmitters and integrated germanium photodiodes for receivers [12]. Electro-absorption modulators (EAMs) integrated in a Si Photonic platform have been demonstrated [13], using monolithically grown SiGe quantum-well stacks, though no PAM4 signaling has been published to our knowledge. The SiPh solutions offer an advantage in terms of low-cost material and manufacturing platforms, however, the most widely adopted solution in the market utilizes externally modulated lasers (EMLs) comprised of a single (typically InP) chip with separate laser and EAM sections paired [14] with discrete photodiodes. To differentiate from III-V chips which combine lasers with MZM (e.g. for coherent transmitters), we will refer to the chips combining lasers and EAMs as electro-absorption modulated lasers (EAMLs) in this paper. The EAML solutions typically have each channel placed on its own RF carrier and actively aligned with a lens to a fiber, scaling channel count becomes costly and at the extremes not dense enough to fit the module form factors. EAML solutions have the optical output and RF input at the same side of the chip adding to the challenge of forming an array [15], [16], which are difficult to yield, and complicated and need costly RF design to the bring the RF input to the modulator. Typical SiPh solutions also run into scaling challenges either with size of the MZM based solutions or bandwidth for the RR based solutions. On the receiver side, conventional InP and SiPh based solutions require actively aligned lenses or fibers to achieve good responsivity and low polarization dependence, and in some cases require polarization diversity components [17] to deal with the strong polarization dependence of the SiPh platform.

In this publication, the performance of a differentiated transmitter (Tx) and receiver (Rx) chip set solution, utilizing the best aspects of both Si and III-V platforms, is discussed. Details of the design and the Si Photonics platform can be found in [18]). On the transmit side, the SiPh platform is designed for low loss integration with both III-V elements and optical fiber. All components are passively aligned [19], [20], reducing cost and

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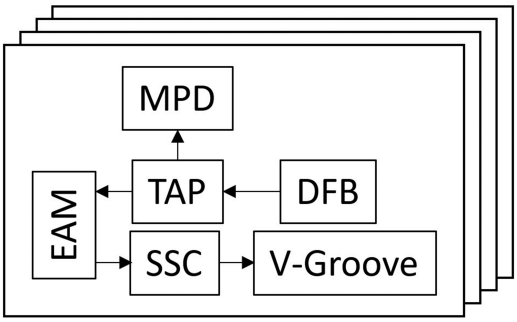

Fig. 1. TxPIC Schematic.

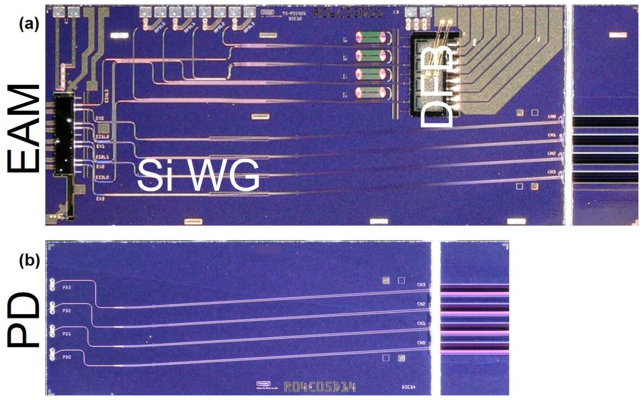

Fig. 2. Top view of PICs (a) Transmitter, (b) Receiver.

Fig. 3. Top view EAM array.

complexity of transceiver assembly. By the use of arrayed lasers and arrayed modulators, the platform easily scales lane count in a compact form factor. The silicon photonics Tx chip, which uses quad EAM U-bend arrays [20], [21] and quad DFB arrays passes the 400 GBASE-DR4 Tx spec requirements [22]. By separating the EAM from the laser, a scalable and dense arrayed solution is achieved, with an even higher channel count obtainable either through attaching multiple arrays to our Si photonic integrated circuits (PICs) or scaling the number of devices in the array. Compared to traditional EAML solutions, our device separates the RF input from the optical output reducing any RF loss and power consumption needed to bring the electrical signal to the optics. The Tx PIC exhibits more than 4 dB dynamic extinction ratio (ER), +1 dBm fiber coupled Optical Modulation Amplitude (OMA) and less than 2.0 dB TDECQ when directly driven by a commercial-off-the-shelf (COTS) DSP with built-in EML driver, at 106.25Gb/s and an SSPRQ pattern as defined in the IEEE802.3 standard [22]. The compact silicon photonics Rx chip, uses high speed monolithic Germanium waveguide photodiodes (Ge PDs) [18], [23] and the same low-loss passive fiber coupling section as our Tx chip, enabling high fiber responsivity and low Polarization Dependent Loss (PDL). The receiver is then formed when the Rx PIC is wire bonded to a COTS transimpedance amplifier (TIA). This receiver exhibits a pre-FEC BER of better than 2.4×10^{-4} at less than -6.5 dBm OMA (for all channels on in the worst case cross-talk condition) when it is tested with the COTS DSP at 106.25Gb/s PAM4 for a PRBS31Q as defined in the IEEE802.3 standard [22]. Separating the components of the widely adopted EAML and combining with our low-loss passive alignment SiPh platform provides the power efficiency and cost effectiveness necessary to scale the channel count and bandwidth for pluggable optical modules or other form factors such as Co-Packaged Optics.

The paper focuses on the performance results achieved from the Tx and Rx PICs and first briefly discusses chip architecture and some key features of the hybrid assembly which will enable low-cost high-volume production in Section II. Section III reviews the component level and DC performance of the PICs and Section IV discusses system level test results conforming to specifications set out in the IEEE 802.3 standard. The final section discusses how the solution can scale to 8 channels and other embodiments enabling next generation aggregate data rates and requirements.

II. Architecture and Assembly

The Tx PIC, with a schematic shown in Fig. 1, and top view shown in Fig. 2(a), contains 7 key components. First are recessed cavities in the silicon for attach of the III-V die. The cavities contain mechanical stops as a height reference for flip-chip bonding and the waveguide interfaces are designed for low-loss and low back-reflection. Next a tap coupler and monolithically integrated Ge waveguide MPDs are used to provide optical power monitors for actively controlling the DFB drive current under APC (Automatic Power Control) operation. Integrated Ge temperature sensor diodes are used to monitor the chip temperature and allow temperature control to ensure performance of DFB and EAM during operating life. Low-loss waveguide crossings enable efficient routing into and out of the U-bend EAMs. At the output of the PIC a spot-size converter (SSC) transforms the $3\,\mu$m silicon mode to a $13\,\mu$m mode optimized for coupling to SMF fibers. The facet at the fiber interface is optimized for low back reflection. Finally, V-grooves are etched and lithographically aligned to the wavguide facet, to enable self-aligned passive fiber attach coupling light from the output of the SSC to the fiber.

The receive chip shown in Fig. 2(b) includes the V-grooves, SSC, fiber interface facet and routing to a high-speed Ge waveguide PD array which is monolithically integrated into the Si in the same manner as the MPDs and temperature sensors for the Tx PIC. The design and fabrication of the components has been previously discussed in [18].

The EAM array is comprised of 4 devices each consisting of a tight U-bend waveguide, as seen in Fig. 3, resulting both in a short device for high-speed operation and a tight channel pitch to minimize die size. Bringing both input and output to the same side of the die enables bonding with a small optical gap to a single side of the die and minimizes coupling loss independent of any dicing tolerances. The waveguides at the EAM input and output are well matched to the Si PIC, which contains a height converter [24], further reducing coupling losses and improving bonding alignment tolerances. The facets are designed to reduce back reflection into the laser to below the required level. Isolation trenches separate the die on the quad array ensuring low electrical crosstalk.

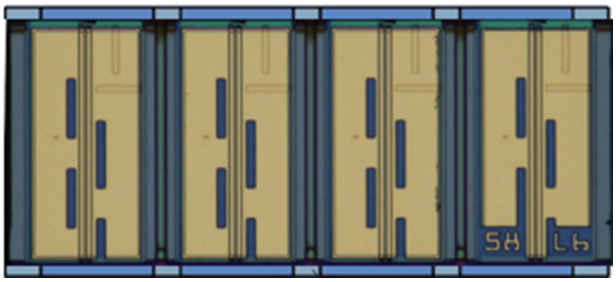

Fig. 4. Top view DFB array.

Fig. 4 shows the quad DFB array chips which is processed using the same standard III-V manufacturing techniques as the EAM array. The DFB design is optimized for high single mode yield and back reflection tolerance. Both InP die include mechanical reference layers in the epitaxial layer stack to make contact with the mechanical stops in the Si cavity on the PIC to control the vertical alignment during flip-chip bonding.

Post-fabrication, the silicon wafers are electrically tested and sent through automated wafer-level optical inspection (AOI) to create maps of known good die (KGD). The photodetectors on the Rx chips are also characterized for bandwidth and responsivity at wafer-level test (WLT). The receiver parts are then ready for singulation and fiber attach while the Tx PICs can be sent for wafer level flip-chip bonding of DFB array and EAM array. The InP wafers also undergo wafer-level AOI and WLT post-fabout and are singulated in preparation for bonding.

Bonding relies only on machine vision of fiducials on both the Si PIC and InP die for in-plane passive die alignment. The local eutectic solder reflow ensures good electrical and thermal connection between the die and compresses the III-V die against the Si pillars for vertical alignment, and enables consecutive bonding of multiple III-V chips. The III-V die make direct thermal contact with the Si to ensure proper heat sinking. The tool alignment 3σ tolerance is specified to $\pm 0.5\ \mu\mathrm{m}$, further reducing coupling loss between InP and Si die. After bonding, index matching gel is dispensed to fill any gap remaining between the die with a refractive index matched to the ARC (Anti Reflection Coating) design for each part.

After die singulation, SMF fiber attach (pigtailing) is a passive process. Due to the mode size at the output of the SSC the low NA (numerical aperture) of the output enables a loose tolerance with respect to the longitudinal placement of the fiber relative to the facet. A fiducial lane at the end of the chip provides a visual guide for alignment of fiber. The V-grooves provide complete lateral, yaw and pitch alignment for the fibers. The interface is designed for a fiber with a straight cleaved facet. A glass cap is used to mechanically push and secure the fibers into the V-grooves which are then bonded in place with epoxy. The epoxy is selected so that it is index matched to the fiber mode index as it fills the gap between the fiber facet and the Si facet, in order to minimize the reflections from the straight cleaved fiber facet.

III. DC Measurements

A. Rx PIC

The Rx PICs are measured at wafer level for diode IV characteristics and opto-electronic S_{21} bandwidth measurements. The responsivity is also measured at wafer level and a sample of parts are pigtailed and measured for responsivity. The results of those pigtailed measurements are used to calculate a calibration factor needed for converting the WLT measured fiber-coupled responsivity. Histograms of the WLT measurement results on a sample of Rx PICs are shown in Fig. 5. The fiber-coupled responsivity has a median value for the worst-case polarization of $0.67\mathrm{A/W}^{-1}$ with a typical PDL (not shown) of 0.5 dB of which about 0.3 dB is attributed to the SSC PDL. The bandwidth, into a 50Ω load, of the devices measured has a median value of 38.3 GHz, sufficient for 53GBaud PAM-4 operation. The dark current for the devices is typically around $0.1\ \mu\mathrm{A}$ and more than 95% of measured parts are lower than $1\ \mu\mathrm{A}$.

B. Tx PIC

The DFB are measured and screend at wafer level for electro-optic and spectral characteristics of each device on the wafer. Parts are screened for threshold current, side mode suppression ratio (SMSR) and mode hops. As shown in Fig. 6(a), the wafer-level yield for channel SMSR $> 30\,\mathrm{dB}$ is $> 97\%$ when excluding the die at very top and bottom of the wafer which do not have a grating written. The DFBs demonstrate single mode behavior above threshold as seen in the plot of Fig. 6(b) with very high SMSR across the full range of drive currents.

On a sample basis, DFB die are mounted p-side up on carriers to characterize the die-level facet output power. The power is measured using an integrating sphere and typical powers are $22\,\mathrm{mW}$ at $55\,^{\circ}\mathrm{C}$ for $100\,\mathrm{mA}$ drive current and $35\,\mathrm{mW}$ at $150\,\mathrm{mA}$ drive current. The distribution of power measured from the sample of parts is shown in Fig. 7(a) as a function of temperature showing a power change with temperature having a slope of $-0.29\,\mathrm{mW}^{\circ}\mathrm{C}^{-1}$ at $150\,\mathrm{mA}$ drive current. The distribution of optical powers at $55\,^{\circ}\mathrm{C}$ and $100\,\mathrm{mA}$ is shown in Fig. 7(b). Only a small sample of die are measured for facet power since die-level measurements exclude parts from being used for flip-chip bonding.

In characterizing a completed, bonded Tx PIC, the optical coupled power is measured by both the monitor photodiodes and by monitoring the fiber output power with $0\mathrm{V}$ bias on the EAM. In Fig. 8(a) we see typical I-I curves for the MPD photocurrent as a function of laser drive current showing low threshold current (not impacted by the flip-chip bonding) and linear slope efficiency out to $150\,\mathrm{mA}$. The distribution of MPD currents from measured parts at $100\,\mathrm{mA}$ DFB drive current at $55\ ^{\circ}\mathrm{C}$ has a median value of about $1\,\mathrm{mA}$, as shown in Fig. 8(b). This amount of photocurrent implies the coupled on-chip power is at least $16.3\,\mathrm{mW}$ for $100\,\mathrm{mA}$ DFB drive current, based on the designed tap coupler and an internal MPD responsivity of $1.05\mathrm{A/W}$. The coupled chip power is dependent on both the facet output of the laser and the coupling efficiency between the InP chip and the Si PIC. Combining with the data on the facet power shown in Fig. 7 from the DFB measurements, we estimate the median PIC to DFB coupling loss of 1.3 dB. The measurements are in good agreement with the simulated results, shown in Fig. 9, where the simulated distribution for the worst channel coupled of the quad-array DFB with all stack-up, etch, and both linear and angular bonding tolerances. The simulated best-case coupling efficiency is 0.9 dB and the median value is 1.2 dB. The measured LIV in Fig. 10 demonstrates coupled output power in the fiber of up to more than $4\,\mathrm{mW}$ at $150\,\mathrm{mA}$ laser drive current.

The EAM WLT electrically probes a sample of die monitoring series resistance and dark current to confirm the diode's behavior. The median series resistance is measured at $20\,\Omega$. This low value is sufficient for supporting high-speed RF performance.

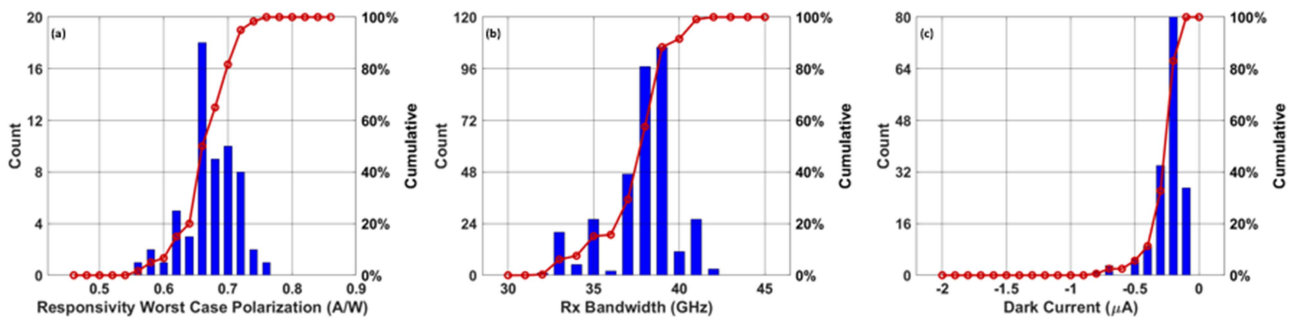

Fig. 5. Rx PIC DC Measurement Results.

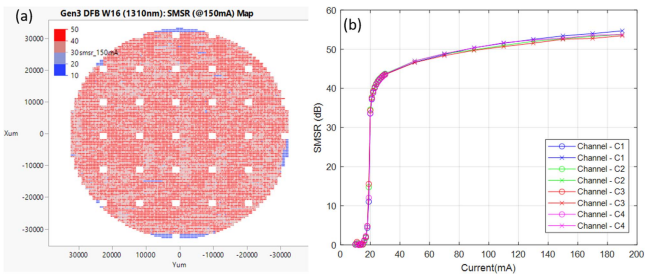

Fig. 6. DFB Wafer Level DC Measurement Results. (a) SMSR wafer map, (b) SMSR change with laser current on a sample.

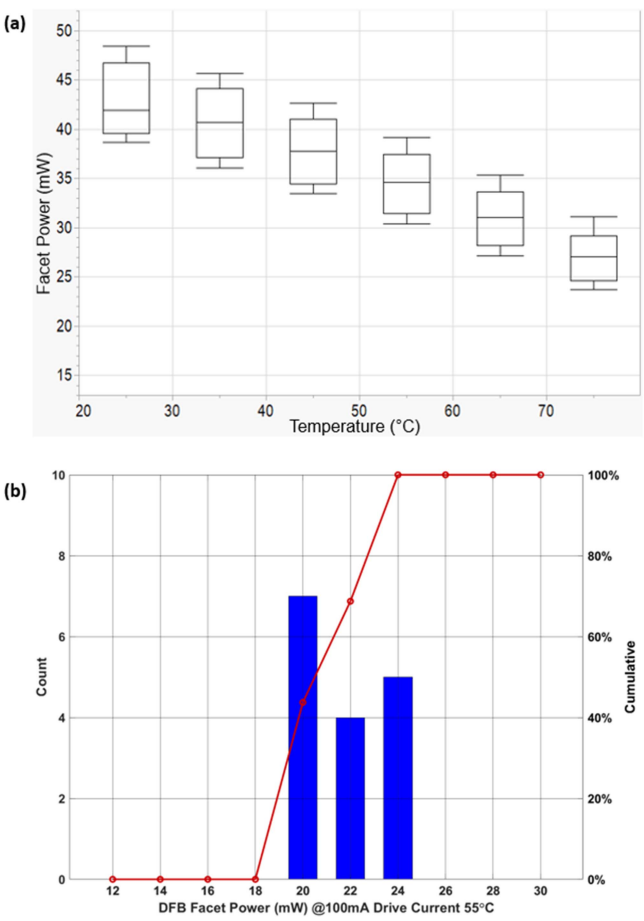

Fig. 7. DFB Facet Power measurements. (a) Performance over Temperature, (b) Distribution at 55 °C and 100 mA.

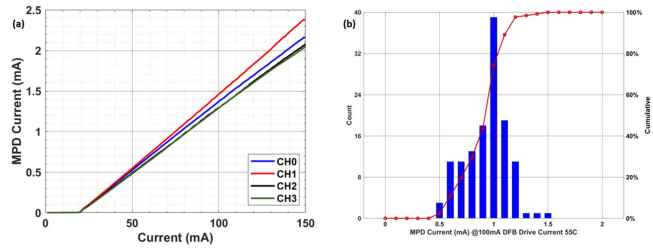

Fig. 8. MPD Measurement Results (a) MPD current in function of laser current, (b) Distribution at 55°C and 100 mA.

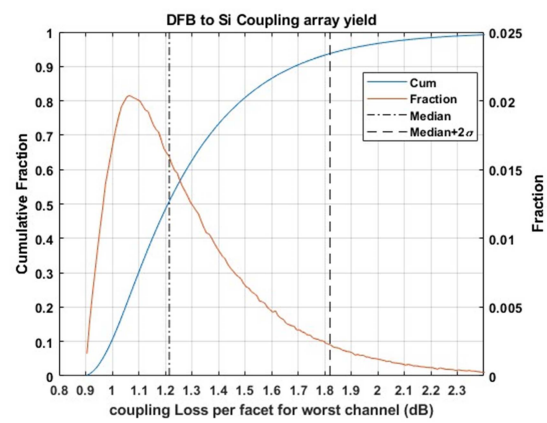

Fig. 9. DFB Coupling Simulation Results.

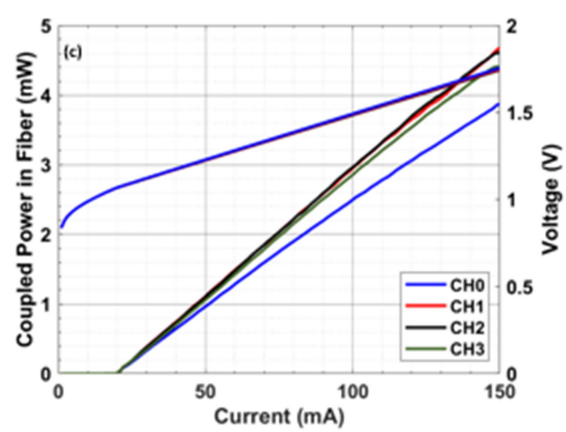

Fig. 10. Measured Tx PIC LIV of fiber coupled power at 55°C and 0V bias on the EAM.

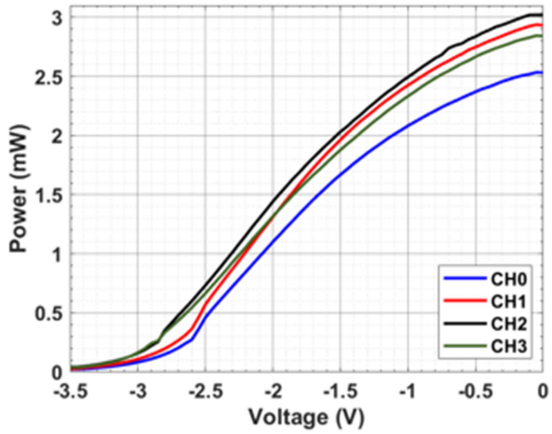

Fig. 11. Measured Tx PIC fiber coupled power in function of EAM bias at 55°C and 100 mA laser current.

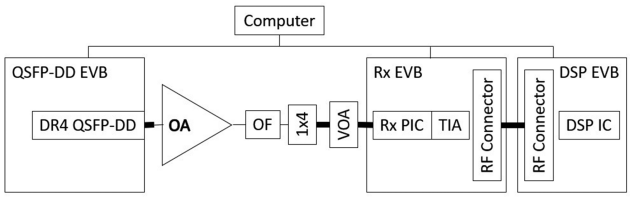

Fig. 12. High Speed Test Setup.

Typical dark current values are less than 2 nA. Die level measurements are used to confirm electrical isolation between channels in the array which is shown to be greater than 10 MΩ. Optical characterization of the modulator is done post integration with the Si PIC and DFB.

The DC optical performance of the EAM is measured by sweeping the reverse bias while maintaining the DFB current at 100 mA. The transfer curves of a typical array are shown in Fig. 11. At a −1.75 V bias, the device exhibits about 6 dB of static extinction ratio with 1.5 V_{pp} swing voltage, consistent with the output of COTS DSPs, and the fiber coupled output power is about 2 dBm at that bias point.

IV. High Speed Measurements

A. Rx Chip

The Rx PICs were characterized for BER performance in a link testbed (shown in Fig. 12) using a commercial TIA, and DSP evaluation board, both for the 400GBASE-DR4 market. A custom Rx evaluation board (RxEVB) was designed for the RxPIC and the TIA, so that they can be co-located and wire bonded directly with short wire bonds (≈ 350 μm length). The differential outputs of the TIA were routed to a parallel 8x high speed connector and connected to the DSP EVB, which has a similar parallel high-speed connector, through approximately 8" of RF cables. Both the presence of the cables and the PCB trace length cause additional losses that would not be present in a transceiver design, however the DSP equalizer was still able to produce good BER results. A commercial 400GBASE-DR4 QSFP-DD transceiver on an evaluation board (EVB) was used as a reference transmitter and operated as a pattern generator producing a PRBS31Q pattern. A single channel of the QSFP-DD output is connected to the input of an optical amplifier (OA) and followed by an optical filter (OF). This signal is then split into 4 optical fibers. The power in each of the 4 fibers is then controlled by a 4-channel programmable variable optical attenuator (VOA). The presence of the optical amplifier enables the test setup to go to overload conditions of + 4.2 dBm OMA on all channels simultaneously. The OMA in each fiber after the programmable attenuator was calibrated for each of the programmed attenuation levels. The QSFP-DD channel used had a measured outer ER of 4.7 dB, an SECQ of 1.0 dB and a linearity RLM of 0.985.

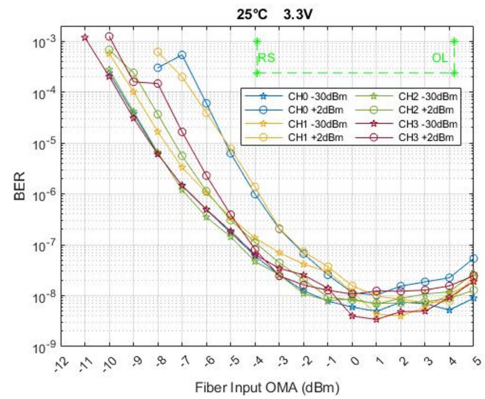

Fig. 13. Measured RxPIC/TIA BER curves 25 °C.

BER measurements were performed using the error detection and counting features in each of the 4 DSP channels while varying the optical power incident on the channel under test in steps of 1 dB, from −12 dBm to +5 dBm in OMA using the programmable attenuator. The other 3 channels were kept at a constant attenuation to emulate a desired level of optical crosstalk penalty with aggressor channels set to either −30 or +2 dBm OMA. For each optical input power, the DSP error counter is reset after a wait time, typically 10 − 15 s, to allow the adaptive equalizer to adjust to the new signal level. The error accumulation runs for 30 s and the BER is calculated from the total number of errors.

Bathtub curves of BER as a function of received fiber OMA are shown in Fig. 13 for 25°C and 3.3 V supply. Each channel is shown with no crosstalk (−30 dBm on the aggressor channels) and typical max power on the aggressor channels (+2 dBm), also shown are the IEEE Receiver Sensitivity spec (RS) and overload spec (OL). For a transmitter with 1 dB SECQ, the minimum required receiver sensitivity is −3.9 dBm OMA at a BER of 2.4×10^{-4}. Under crosstalk operation the measurement shows that this spec is achieved with at least 2.5 dB margin. Data center links will always operate at a received power higher than the receiver sensitivity. The BER level at that input power with crosstalk is around 10^{-6} on 2 of the channels, dropping to 10^{-8} at higher power levels, and around 10^{-7} on the other 2 channels, and similarly dropping to 10^{-8} at higher power levels. Under overload conditions of +4.2 dBm, the achieved BER has slightly increased, but still better than 6×10^{-8}. A typical operating input power range in data centers is −2 to +2 dBm, where the achieved BER is better than 7×10^{-8}.

B. Tx Chip

To characterize the bandwidth of the device, the modulator pads on the PIC are contacted with a high-speed RF probe which is connected to a vector network analyzer. For a 50 Ω source the bandwidth of the EAM bonded to the PIC is > 25 GHz across

TABLE I
KEY PERFORMANCE MEASUREMENT RESULTS FOR EACH CHANNEL OF A DR4 TXPIC WITH -1.9V EAM BIAS

Channel	Laser Current	EAM Current	AOP	ER	OMA	TDECQ	OMA-TDECQ
Units	mA	mA	dBm	dB	dBm	dB	dBm
IEEE spec			≥ -2.9	≥ 3.5	≥ -0.8	≤ 3.4	≥ -2.2
0	130	7.2	1.16	4.33	0.93	1.87	-0.94
1	130	7.9	1.61	4.42	1.47	1.81	-0.34
2	150	8.4	2.76	4.13	2.34	1.75	$+0.59$
3	150	8.75	1.99	4.22	1.68	1.60	$+0.08$

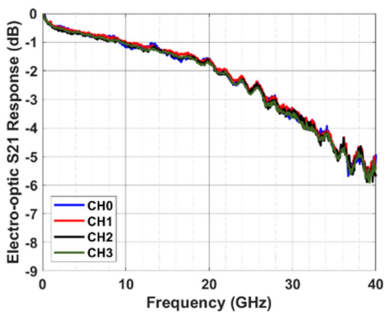

Fig. 14. Measured TxPIC S_{21}.

the range of operating bias points. A representative E-O S_{21} plot is shown in Fig. 14 for all 4 channels.

Tx PIC high-speed large signal measurements were performed with the PIC sitting on a temperature-controlled stage. A multi-channel DC probe is used for contacting the lasers, MPDs and TSs, and an RF probe for contacting the EAM pads and connect to the output from a COTS DSP eval board or an AWG (Keysight M8196 A). When using the AWG, the signal from the AWG is followed by an RF amplifier as the EAM required voltage swing is higher than the output swing capabilities of the AWG. The calibration correction features of the AWG are used in this case to calibrate out the frequency dependent electrical losses of the RF cables, RF amplifier and biasT (the RF probe losses are not calibrated out). When using the DSP eval board as a source, the eyes are post-processed removing the eval board's frequency response using de-embedding files provided by the DSP supplier (the cable losses and the probe losses are not de-embedded and hence add some uncorrected degradation to the measurement). The laser is driven with an SMU current source with the MPD and temperature sensor diodes monitored for photocurrent and voltage respectively. The EAM is biased with a SMU voltage source through the DC input of a high speed BiasT either externally connected to the output from the AWG or embedded in the DSP eval board. When modulating with the AWG the output waveform is calibrated and set to $1.5\,\mathrm{V}_{pp}$ swing. When driving directly from the DSP capable of providing $1.5\,\mathrm{V}_{pp}$ swing, tap settings from the available built-in look-up tables (LUTs) are optimized for a small sweep around the predicted EAM bias point and a low laser drive current. Each channel is then measured for the optimal conditions using a small sweep of both laser drive current and EAM bias. The output fiber is connected to a clock recovery unit (CRU Keysight N1078a), which taps off 50% of the power, and a sampling oscilloscope (DCA Keysight 1092) for verifying compliance with the IEEE standard by driving with a 53.125 GBd PAM-4 SSPRQ pattern. The DCA measurements are calibrated to the power coming out of the fiber before the CRU unit. The DCA reports the OMA, AOP, dynamic ER and TDECQ which are recorded for each EAM bias and laser drive current.

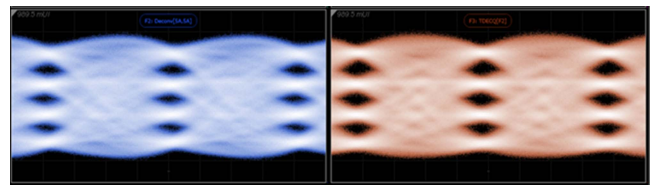

Fig. 15. Measured TxPIC PAM-4 Eye. *left:* De-embedded; *right:* post-Rx equalizer.

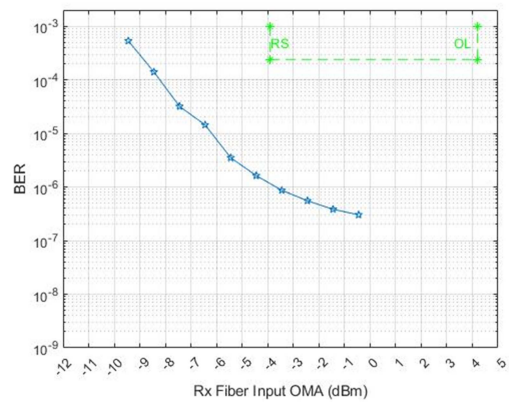

Fig. 16. Link Test Measurement Results.

For a TxPIC with a laser wavelength of $1311\,\mathrm{nm}$ operating at $55°\mathrm{C}$, an EAM bias of $-1.9\,\mathrm{V}$ and more than $7\mathrm{mA}$ photocurrent gives a dynamic extinction ratio of $> 4.1\,\mathrm{dB}$ for all channels when driven with the DSP EVB. The outer OMA for each channel is greater than $+0.9\,\mathrm{dBm}$ and the TDECQ penalty is less than $2\,\mathrm{dB}$ for all channels. The sample eye diagram of the de-embedded signal received by the DCA is shown in Fig. 15 on the left. The post receiver equalizer eye used for TDECQ calculations is shown to the right. A summary of the results is shown in Table I highlighting the key metrics for each channel.

A link test using the receiver EVB and one of the transmitter channels, operating at $55°\mathrm{C}$, was performed to confirm the BER performance of the chipset solution. The transmitter output is connected to a VOA, which has an excess loss of about 1.5 dB, and then to the receiver input. Since the power is sufficient to reach the floor of the receiver bathtub curve, no amplifier is used for simplification of the measurement. Power recorded on the plot in Fig. 16 is in the fiber before coupling to the Rx PIC. The DSP output used to modulate the EAM is set to the PRBS31Q test pattern consistent with receiver sensitivity measurements. Fig. 16 shows a floor value of 3×10^{-7} BER and received power of $-8.5\,\mathrm{dBm}$ at 2.4×10^{-4} BER consistent with the expected penalty from the TDECQ difference between the TxPIC and the reference transmitter used for the receiver PIC evaluation when there is no cross-talk.

V. Conclusion

We demonstrate a SiPh based 400GBASE DR4 Tx/Rx chipset compatible with COTS DSP and TIA ICs. The integration platform allows for simple passive fiber attach for ease of packaging into a transceiver. The hybrid integrated III-V devices (DFB arrays and U-Bend EAM arrays), allow for improved manufacturing throughput and low cost by enabling packaging of only known-good die, using a vision assisted passive align and attachment process. Furthermore, the platform is extendable while maintaining a small footprint by increasing either the number of quad EAM and DFB arrays, the channel count per array or both as well as the number of lanes on the SiPh and integrated PDs on the Rx side. PICs with 8 lanes of 100Gb/s PAM4 have been fabricated and are presently in test and characterization. Use of SiPh multiplexers and de-multiplexers [18] enables the platform in a WDM architecture. Additionally, having both PDs and contacts to the modulators at the edge of the chip opposite the optical output enables tight integration with high-speed electronics in, for example, co-packaged optics applications.

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