







Demonstration of Silicon-Photonics Hybrid Glass-Epoxy Substrate for Co-Packaged Optics

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Abstract—To realize a new package substrate for co-packaged optics, a silicon-photonics hybrid glass-epoxy substrate was demonstrated. In the substrate, silicon photonics dies working as optical/electrical conversion engines are embedded. Additionally, it includes optical redistribution composed of polymer waveguides and mirror-based optical coupling structures between the polymer and silicon waveguides. A demonstration sample was designed for a total bandwidth of 10 Tbps using silicon photonics dies with arrayed waveguide gratings, wavelength splitters, and polarization splitters/rotators for 16-ch wavelength division multiplexing (WDM). It was fabricated using unique key technologies, such as silicon photonics embedding, micromirror fabrication, and single-mode polymer waveguide fabrication. Its wavelength multiplexing operation and signal transmission characteristics were evaluated. As a result, the hybrid substrate was discovered to be capable of 112 Gbps pulse amplitude modulation 4 (PAM-4) transmission with a 16-ch WDM function because the transmitter dispersion and eye closure quaternary (TDECQ) values of less than 3.4 dB were obtained and 16-ch WDM spectrum were clearly visible. To the best of our knowledge, the working of such a hybrid substrate was demonstrated for the first time. This demonstration implies that the hybrid substrate is feasible, and the above-mentioned novel technologies are crucial to its development.

Index Terms—Co-packaged optics, hybrid package substrate, micro mirror, optical redistribution, silicon photonics, single-mode polymer waveguide.

I. INTRODUCTION

DATA movement in high-performance computing systems and large-scale data centers is a critical concern. Increasing the data rates of conventional electrical links leads

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to low latency tolerance, high power consumption, and poor signal integrity, particularly for long-distance interconnects. Co-packaged optics (CPO) have attracted significant attention because they can considerably reduce the length of high-data-rate electrical links [1]. For example, Broadcom and Tencent have recently partnered to accelerate the commercialization of CPO network switches. The switch is an application-specific integrated circuit (ASIC) package in which silicon (Si) photonics dies are co-packaged and over 100 optical fibers are connected to it. Such massive parallel optical input/outputs (I/Os) are required for high-performance LSIs, such as the upcoming high-capacity switch ASICs with data transmission rates of 25.6 and 51.2 Tbps.

We previously proposed a novel package substrate, referred to as an active optical package (AOP) substrate, as a novel CPO solution [2]. A bird's-eye view and cross-sectional schematic of the AOP substrate are shown in Fig. 1. The AOP substrate is based on a silicon photonics hybrid glass-epoxy substrate, which is a conventional glass-epoxy package substrate in which Si photonics dies are embedded as optical/electrical conversion engines. The electrical I/Os of the Si photonics dies are connected via thin-film metallization (electrical redistribution). Its optical I/Os are connected to standard single-mode fibers (SMFs) via optical redistribution, which is composed of polymer waveguides and micro mirrors, as shown in Fig. 1. We have developed some of its key technologies, such as micromirror integration [3], Si photonics die embedding [4], and mirror-based optical coupling between Si and polymer waveguides [2].

Recently, we demonstrated a Si-photonics hybrid glass-epoxy substrate using the above-mentioned key technologies to realize an AOP substrate [5]. In this article, additional fabrication results of the micro mirror, planarization process, and polymer waveguide for demonstration sample are provided. Moreover, measurement results of the 16-ch optical spectra, insertion loss, eye diagrams, and transmitter dispersion and eye closure quaternary (TDECQ) are provided. Based on these results, we present additional discussions about the loss and transmission characteristics of demonstration sample.

II. DESIGN

The demonstration sample was designed as a package substrate with a maximum capacity of 10 Tbps. As shown in Fig. 2, two Si photonics dies are embedded in the sample. Three sets of 16-ch wavelength multiplexing (MUX) / demultiplexing (DeMUX) devices [6], [7] were placed in each die for the

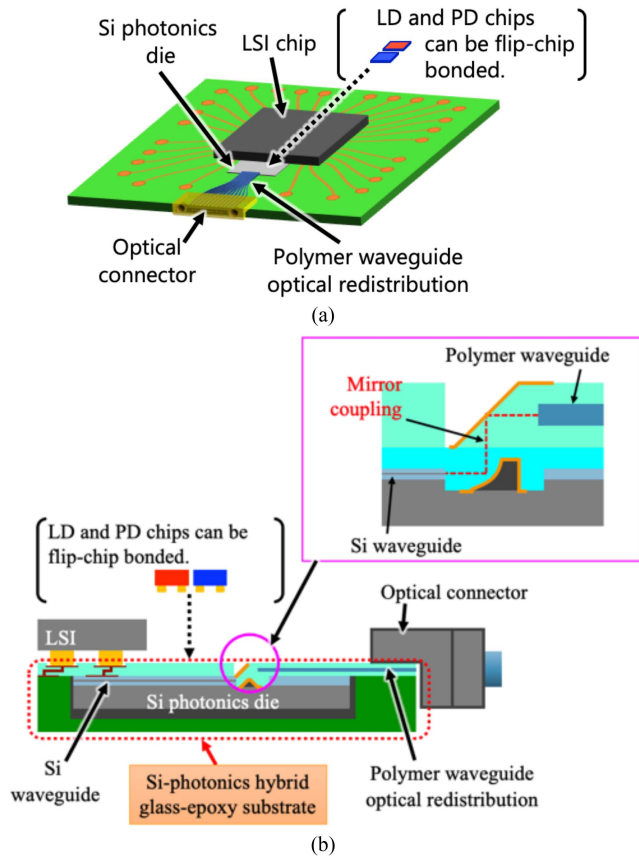


Fig. 1. (a) The bird's-eye view and (b) cross-section schematic of the CPO using the AOP substrate. For the CPO using the LD and PD chips, the substrate can also be used as an optically functional platform.

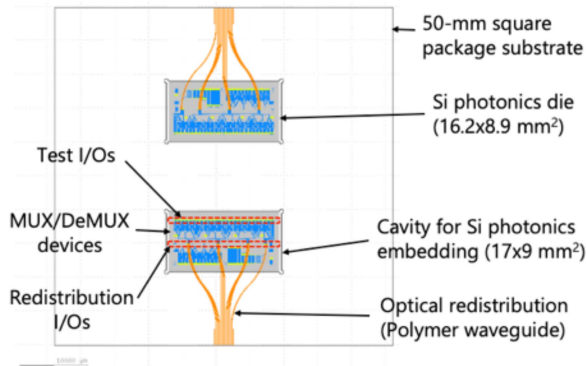


Fig. 2. Demonstration sample layout of the Si-photonics hybrid glass-epoxy substrate.

transmitter (TX) and receiver (RX). Therefore, 96 channels were present in the single-package substrate. At a data rate of 112 Gbps, the sample achieves a total bandwidth of 10 Tbps. Arrayed waveguide gratings (AWGs) and interleaver were placed in the die for 16-ch wavelength MUX/DeMUX. Polarization splitters and rotators were placed on the RX to achieve polarization diversity. The detail parameters for polarization rotator/splitter, interleaver, and AWG are described in previous works [6], [7]. Wavelength-multiplexed signals on the die were input/output

via a spot-size converter (SSC) and a bottom-side mirror. The multiplexed signals from the Si photonics were delivered to the edge of the package substrate via the optical redistribution layer or vice versa. Six optical redistributions were placed on each die. By the optical redistributions, the non-uniform-pitch optical I/Os of the dies were arranged to meet the standard $250\text{-}\mu\text{m}$ fiber array pitch. In this study, active devices such as modulators and photodetectors were not placed in the dies. Free space vertical coupling test I/O ports were used as a replacement for these devices in order to evaluate the optical signal transmission characteristics of hybrid substrates. In the evaluation, the optical signals were delivered from/to external optical equipment such as a modulator and oscilloscope. Despite the fact that Si photonics active devices were not placed in the substrate in this work, this optically passive hybrid substrate can be used as a WDM platform for CPO using laser diode (LD) and photodetector (PD) chips, as shown in Fig. 1.

The total footprint of the aforementioned Si photonics devices was $10 \times 3 \text{ mm}^2$ for each die. However, the die size was $16.2 \times 8.9 \text{ mm}^2$. This was due to the fact that other test element groups (TEGs), such as the other AWGs and reference devices, were also placed in the die. For the glass-epoxy substrate, we used a high-Tg (glass transition temperature) and low-CTE (coefficient of thermal expansion) material, MCL-E-705G(L), from Showa Denko Materials Co., Ltd. The substrate dimensions were 50 mm^2 . Two cavities were used for embedding the Si photonics dies. The cavity size was $17 \times 9 \text{ mm}^2$. The selected glass-epoxy substrate has CTE of $3\text{--}4 \text{ ppm}/^\circ\text{C}$ which is equivalent with that of Si. Therefore, thermo-mechanical deformation is negligible for the polymer waveguides which go over glass-epoxy substrate and Si die. Additionally, temperature dependence of polymer waveguides and mirror coupling structure were evaluated in previous work, and the temperature tolerance was verified [8], [9].

III. FABRICATION

A. Process

The fabrication process for the demonstration sample is illustrated in Fig. 3. First, the bottom mirrors were integrated into a Si photonics die, as detailed in [3]. Subsequently, the Si photonics dies were embedded in a glass-epoxy substrate. The embedding process is described in [4]. Subsequently, the surface was planarized using a transparent resin, and a polymer waveguide bottom cladding layer was formed. The waveguide cores were then fabricated using lithography. Finally, the top cladding and topside mirrors were fabricated using lithography.

B. Results

Fig. 4 shows a photograph of the embedded Si photonic dies after the bottom-side mirror integration. Bottom-side mirrors were fabricated in the optical coupling areas for polymer waveguide optical redistribution and test I/O ports. For the optical redistribution, the fabricated mirror angle was 40° and curvatures were 40 and $27 \mu\text{m}$ in the a-a' and b-b' directions, respectively. For the test I/O ports, the fabricated mirror angle was 38° and

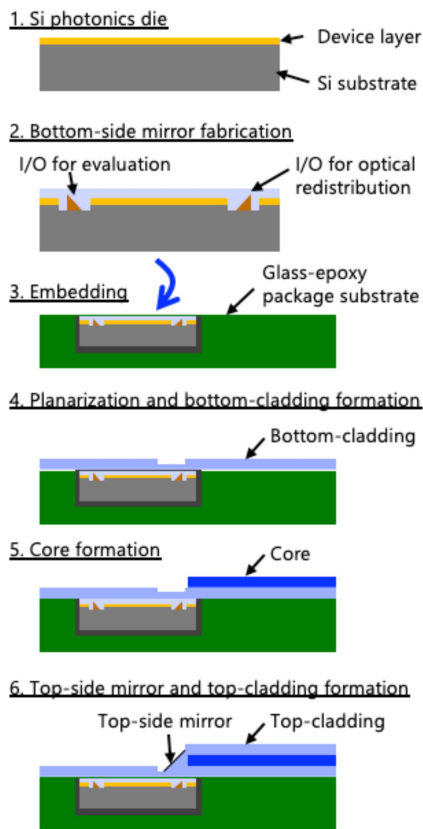


Fig. 3. Fabrication process of the Si-photonics hybrid glass-epoxy substrate.

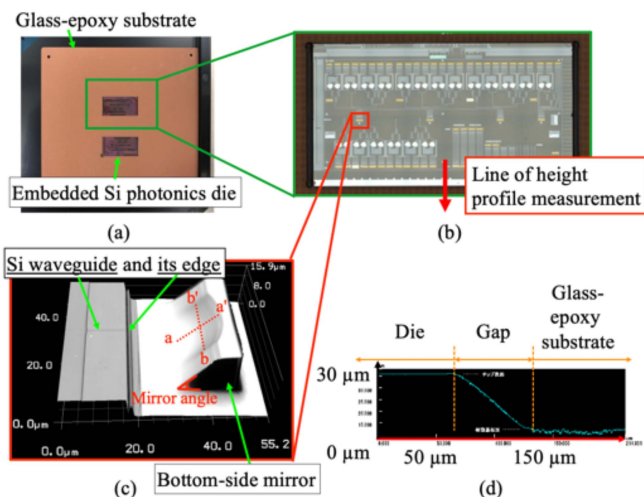


Fig. 4. (a) Photograph of the Si-photonics die embedded glass-epoxy substrate, (b) photograph of the embedded Si photonics die, (c) 3D surface profile of the bottom-side mirror measured by laser microscopy, and (d) a surface profile near the die edge.

curvatures were 36 and 28 μm in the a-a' and b-b' directions, respectively. Unfortunately, the optimum angle and curvatures (45°, 60 μm in the a-a' direction and 30 μm in the b-b' direction) were not obtained in this demonstration sample. Therefore, the optical coupling losses for the polymer waveguides and test I/O ports were large. The surface profile near the die edge is shown

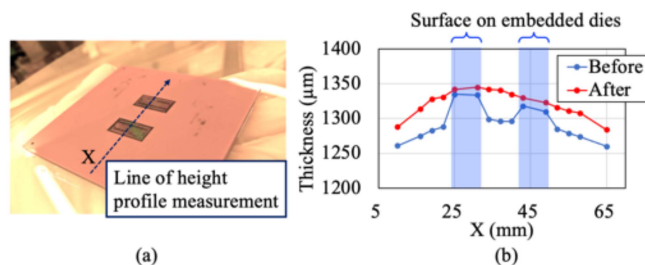


Fig. 5. (a) Photograph of the die-embedded glass-epoxy substrate after the planarization process. (b) Measured surface profile on a line X before and after the planarization.

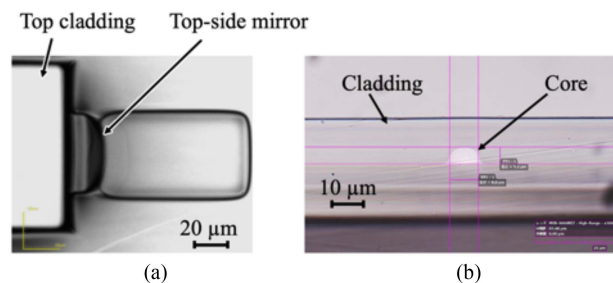


Fig. 6. (a) A laser microscopic image of the fabricated top-side mirror and (b) a cross-sectional optical microscopic image of the polymer waveguide.

in Fig. 4(d). The die surface was 30 μm higher than that of the glass-epoxy substrate.

It is necessary to planarize the surface of the die-embedded glass-epoxy substrate to fabricate low-loss polymer waveguides. Fig. 5(a) shows a photograph of the planarization process. The surface profiles of the sample were measured before and after planarization, as shown in Fig. 5(b). The profiles were measured along the line shown in Fig. 5(a). The discontinuous surface profile before planarization was smoothed after planarization. Substrate warpage was observed before and after the planarization process. Therefore, planarization was not the origin of the warpage.

Fig. 6(a) and (b) show a laser microscopic image of the fabricated top-side mirror and a cross-sectional optical microscopic image of the polymer waveguide, respectively. The measured top-mirror angle was 43.5°, which was slightly gentler than the target value of 45°. This error also causes a coupling loss between the Si and polymer waveguides. The width and height of the polymer waveguide core were 9.0 and 5.4 μm , respectively. The height was slightly smaller than the design value of 9 μm . Therefore, a loss of approximately 1 dB was estimated for coupling with a standard single-mode fiber.

Photographs of the fabricated demonstration sample are shown in Fig. 7. As shown in this photograph, the polymer waveguides were fabricated on a Si-photonics embedded glass-epoxy substrate. The Si photonics I/O ports and edges of the glass-epoxy substrate were connected by polymer waveguides. Test I/O ports were prepared for subsequent evaluations and were not connected to the polymer waveguides.

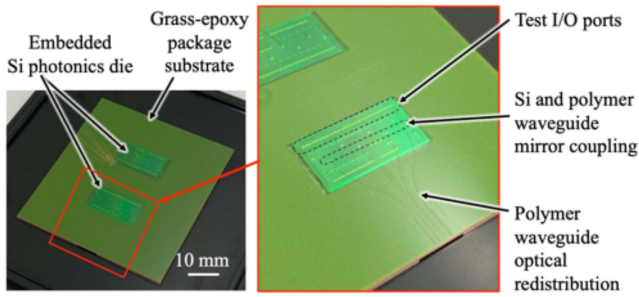


Fig. 7. Photographs of the fabricated demonstration sample.

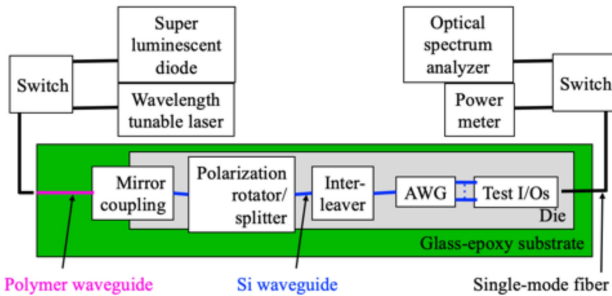


Fig. 8. Measurement setup for optical spectrum and insertion losses.

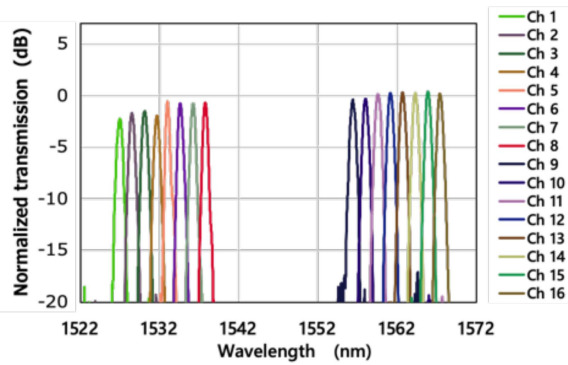


Fig. 9. Measured optical spectra.

IV. EVALUATIONS

A. Optical Spectrum and Insertion Loss

The optical spectral characteristics and insertion losses of the fabricated sample were measured, as shown in Fig. 8. A superluminescent diode (SLD) and an optical spectrum analyzer were used for spectrum measurements, and a wavelength-tunable laser and power meter were used for insertion loss measurements. Light was input to the polymer-waveguide optical redistribution and output from the test I/O ports through mirror coupling, a polarization splitter/rotator, an interleaver, and an AWG.

The measured optical spectra are shown in Fig. 9. All 16 channels are clearly observable. This means that the fabrication process of the hybrid substrate was compatible with Si photonics devices such as AWGs, interleavers, and polarization rotators/splitters.

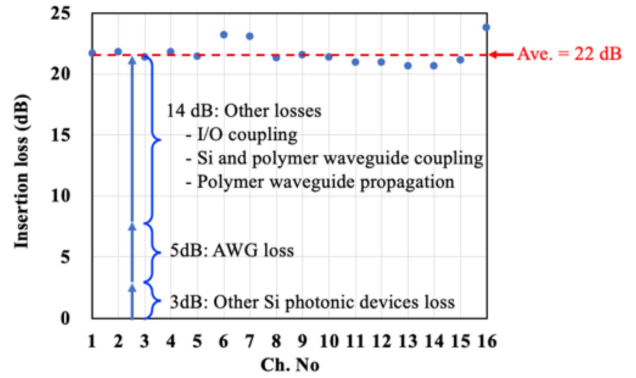


Fig. 10. Measured insertion losses.

Fig. 10 shows the insertion losses of the 16 channels. The average insertion loss was 22 dB. To break down the measured insertion loss, the loss of each Si photonics device was measured using the reference TEGs. As a result, the AWG loss was 5 dB, and the total loss due to other devices loss was 3 dB. Thus, Si photonics devices accounted for the 8 dB loss. The other 14 dB loss consists of coupling loss of SMF to polymer waveguide, propagation loss of the polymer waveguide, coupling loss of the polymer waveguide to Si waveguide via two micro mirrors, and coupling loss of the Si waveguide to SMF via test I/O port. As mentioned above, the coupling loss of SMF to polymer waveguide was estimated to be 1 dB. The propagation loss of polymer waveguide is approximately 0.8 dB/cm at 1.55- μ m wavelength [10]. The waveguide length of demonstration sample is 2.3 cm, therefore, the propagation loss is calculated to be 1.8 dB. The coupling loss of the polymer waveguide to Si waveguide via two micro mirrors was calculated by physical optical propagation method of Ansys Zemax OpticStudio. The measured dimensions of two micro mirrors, as described above, were used to construct the simulation model. Other dimensions such as the mirror position and polymer film thickness were also measured and used for the simulation. As a result, the coupling loss of 9.6 dB was obtained. The coupling loss of the Si waveguide to SMF via test I/O port was also calculated by the same simulation method. The calculated coupling loss was 3.8 dB. Thus, the total coupling loss of 16.2 dB was estimated. The estimated loss was slightly larger than the measured 14-dB loss, however, it was found that the dominant factors were the two coupling losses (between the Si and polymer waveguides and between the test I/O port and single-mode fiber) using mirror coupling. This is because the fabricated bottom- and top-side mirrors were not optimal structures, as mentioned above. However, in previous works, we have demonstrated efficient mirror coupling of 3.6 dB experimentally [11] and 0.5 dB in a simulation. Thus, by optimizing the mirrors, lower transmission losses can be achieved.

B. Signal Transmission Characteristics

To evaluate the optical signal transmission capability of the fabricated hybrid substrate, 112 Gbps pulse amplitude

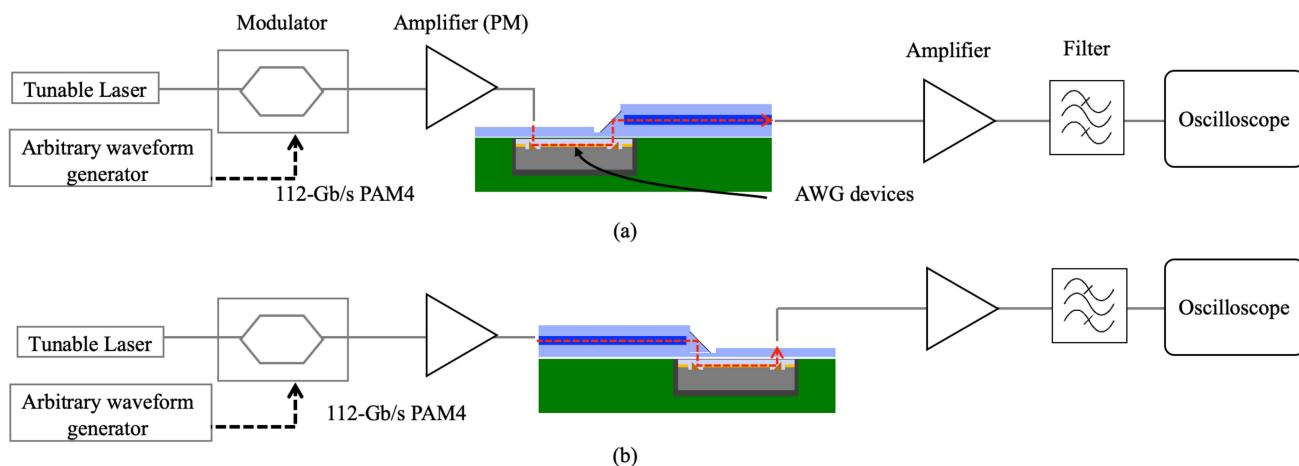


Fig. 11. Measurement setup of 112-Gbps PAM-4 signal transmission for (a) TX and (b) RX TEGs.

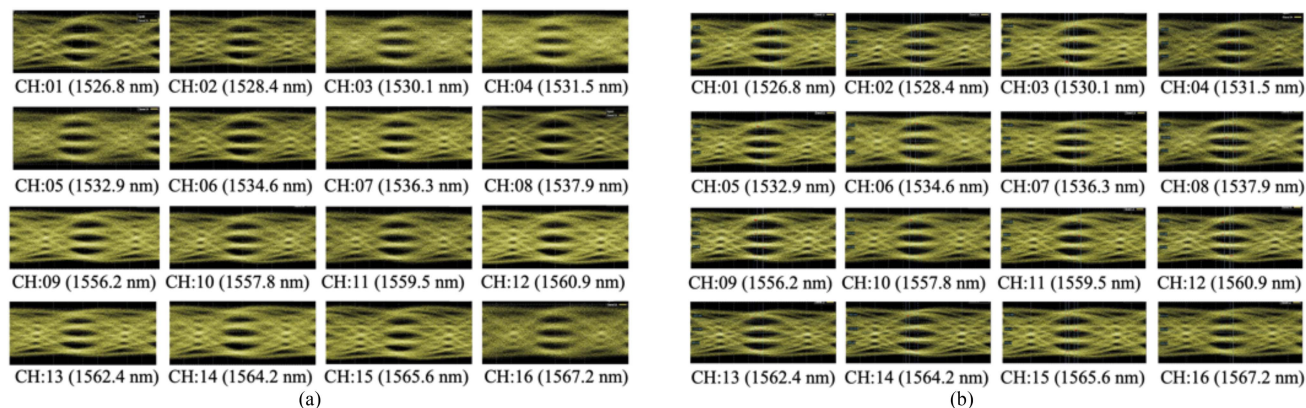


Fig. 12. Measured 16-ch eye diagrams for (a) TX and (b) RX TEGs.

modulation 4 (PAM-4) signals were transmitted, and the eye diagrams were obtained. The TDECQ values were also measured. The measurement setups for the TX and RX TEGs are shown in Fig. 11. For the evaluation, a 112 Gbps PAM-4 signal was generated using a tunable laser, an arbitrary waveform generator, and a lithium niobate (LiNbO₃) intensity modulator. The signal was amplified and TE polarized by an erbium-doped fiber amplifier (EDFA) and a polarization controller, respectively. The signal that passed through the sample was amplified using the EDFA. The amplified spontaneous emission (ASE) noise owing to the 2nd EDFA was removed using an optical filter. Finally, the signal is measured using an oscilloscope. In the TX-TEG evaluations, the signal was input from the test I/O port and passed through wavelength-multiplexing devices. Subsequently, the signal was output from the optical redistribution and measured using an oscilloscope. In the RX TEG evaluations, the signal was input from the optical redistribution and passed through the polarization diversity and wavelength demultiplexing devices. Subsequently, the signal was output from the test I/O port and measured using an oscilloscope.

Fig. 12 shows the measured 16-ch eye diagrams of the TX and RX TEGs. Sixteen channels were measured individually.

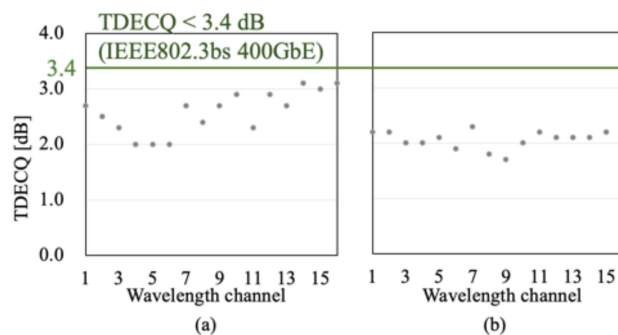


Fig. 13. Measured TDECQ values for (a) TX and (b) RX TEGs.

As shown, all 16 channels successfully transmitted a 112 Gbps PAM-4 signal for both TX and RX TEGs. Fig. 13 shows the measured TDECQ values. The IEEE 802.3bs 400G Base DR4 standard requires a TDECQ of less than 3.4 dB at a symbol rate of 53.125 Gbaud (106.25 Gbps) [12]. The measured results for all 16 channels of the TX and RX TEGs satisfied the IEEE standards. Thus, we successfully demonstrated that

the fabricated hybrid substrate is capable of 112 Gbps PAM-4 transmission with 16-ch WDM function. A reference TDECQ value was also measured by replacing the device with an optical attenuator of the same loss, and it was compared with that of the demonstration sample. As a result, the difference was less than 0.2 dB and was comparable to measurement fluctuation of ± 0.1 dB. Thus, the transmission penalty is enough low. However, the measured TDECQ values are relatively large. This may be due to the ASE noise of the EDFA used in the measurement setup. As mentioned above, the insertion losses were large because of the mirror coupling loss. Therefore, the noise tolerance is low, and the ASE noise affects the TDECQ values. In particular, the insertion losses of the TX TEGs were higher than those of RX; therefore, their TDECQ values were larger than those of RX. By optimizing mirror fabrication, a lower insertion loss can be achieved, and the TDECQ will become smaller.

V. CONCLUSION

To realize a Si-photonics hybrid glass-epoxy substrate as a novel package substrate for CPO, a demonstration sample designed for a total bandwidth of 10 Tbps was fabricated, and its wavelength MUX/DeMUX operation and signal transmission characteristics were evaluated. It was found that the hybrid substrate was capable of 112 Gbps PAM-4 transmission with a 16-ch WDM function because TDECQ values less than 3.4 dB were obtained for the TX and RX TEGs and a clear 16-ch DeMUX spectrum was obtained. Thus, passive hybrid substrates that can be used as WDM platforms for CPO using laser diodes and photodetector chips are demonstrated in this work. To the best of our knowledge, this is the first demonstration of such a hybrid substrate. This demonstration implies that the AOP substrate is feasible and the demonstrated technologies, such as silicon photonics embedding, micromirror fabrication, and single-mode polymer waveguide fabrication, are vital for its development. Electrical redistribution layer (RDL) was not included in this work, however, RDL technologies on Si dies which are embedded or molded in an organic substrate have been developed [13], [14]. These technologies can be applied for the RDL process of AOP substrate. In the future, hybrid substrates incorporating active optical devices, driver/TIA ICs and electrical RDL will be fabricated.

REFERENCES

- [1] C. Minkenbergh, R. Krishnaswamy, A. Zilkie, and D. Nelson, "Co-packaged datacenter optics: Opportunities and challenges," *Int. Eng. Technol. Optoelectron.*, vol. 15, pp. 77–91, 2021, doi: [10.1049/ote2.12020](https://doi.org/10.1049/ote2.12020).
- [2] A. Noriki et al., "Demonstration of optical re-distribution on silicon photonics die using polymer waveguide and micro mirrors," in *Proc. Eur. Conf. Opt. Commun.*, 2020, pp. 1–4, doi: [10.1109/ECOC48923.2020.9333180](https://doi.org/10.1109/ECOC48923.2020.9333180).
- [3] A. Noriki et al., "Mirror-based broadband silicon-photonics vertical I/O with coupling efficiency enhancement for standard single-mode fiber," *IEEE J. Lightw. Technol.*, vol. 38, no. 12, pp. 3147–3155, Jun. 2020, doi: [10.1109/JLT.2020.2995915](https://doi.org/10.1109/JLT.2020.2995915).
- [4] K. Takemura et al., "Silicon-photonics-embedded interposers as co-packaged optics platform," *Trans. Jpn. Inst. Electron. Packag.*, vol. 15, pp. E21–012, 2022, doi: [10.5104/jiepeng.15.E21-012-1](https://doi.org/10.5104/jiepeng.15.E21-012-1).
- [5] A. Noriki et al., "Demonstration of silicon-photonics hybrid glass-epoxy substrate for co-packaged optics," in *Proc. Eur. Conf. Opt. Commun.*, 2022, pp. 1–4.
- [6] S. Jeong et al., "Silicon photonics based 16C³-WDM demultiplexers for operating in C-band and O-band spectral regimes," in *Proc. 45th Eur. Conf. Opt. Commun.*, 2019, pp. 1–4, doi: [10.1049/cp.2019.0737](https://doi.org/10.1049/cp.2019.0737).
- [7] Y. Onawa, H. Okayama, D. Shimura, H. Takahashi, H. Yaegashi, and H. Sasaki, "Polarisation insensitive wavelength de-multiplexer using arrayed waveguide grating and polarisation rotator/splitter," *Electron. Lett.*, vol. 55, no. 8, pp. 475–476, Apr. 2019.
- [8] S. Suda et al., "Heat-tolerant 112-Gb/s PAM4 transmission using active optical package substrate for silicon photonics co-packaging," in *Proc. 26th Optoelectron. Commun. Conf.*, 2021, pp. 1–3.
- [9] F. Nakamura et al., "Analyzing thermal tolerance of mirror-based optical redistribution for co-packaged optics," in *Proc. Conf. Lasers Electro-Opt.*, 2022, pp. 1–2.
- [10] D. Hashimoto, T. Amano, T. Kubota, Y. Okano, and A. Noriki, "Low propagation loss of a single mode polymer optical waveguide on a glass epoxy substrate," in *Proc. IEEE Crit. Path Manage. Techn. Symp. Jpn.*, 2018, pp. 131–132, doi: [10.1109/icsj.2018.8602743](https://doi.org/10.1109/icsj.2018.8602743).
- [11] A. Noriki et al., "Characterization of optical redistribution loss developed for co-packaged optics," *IEEE Photon. Technol. Lett.*, vol. 34, no. 17, pp. 899–902, Sep. 2022, doi: [10.1109/LPT.2022.3191645](https://doi.org/10.1109/LPT.2022.3191645).
- [12] "IEEE P802.3bs 200 Gb/s and 400 Gb/s Ethernet Task Force," Accessed: Apr. 28, 2020. [Online]. Available: <https://www.ieee802.org/3/bs/>
- [13] R. Mahajan et al., "Embedded multi-die interconnect bridge (EMIB) – A high density, high bandwidth packaging interconnect," in *Proc. IEEE 66th Electron. Compon. Technol. Conf.*, 2016, pp. 557–565, doi: [10.1109/ectc.2016.201](https://doi.org/10.1109/ectc.2016.201).
- [14] C. C. Liu et al., "High-performance integrated fan-out wafer level packaging (InFO-WLP): Technology and system integration," in *Proc. Int. Electron. Devices Meeting*, 2012, pp. 14.1.1–14.1.4, doi: [10.1109/iedm.2012.6479039](https://doi.org/10.1109/iedm.2012.6479039).