224-Gbit/S 4-PAM Operation of Compact DC Block Circuit Integrated Hi-FIT AXEL Transmitter With Low Power Consumption

Shigeru Kanazawa, *Senior Member, IEEE*, Takahiko Shindo, *Member, IEEE*, Mingchen Chen, Yasuhiko Nakanishi, Shohei Kosuga, and Hirotaka Nakamura

***Abstract*—We previously developed a semiconductor optical amplifier (SOA) assisted extended reach electroabsorption modulator integrated distributed feedback (EADFB) laser (AXEL) to increase the optical modulation output power and a high-frequency integrated design based on the flip-chip interconnection technique (Hi-FIT) to obtain a high modulation bandwidth. We achieved a high-output power 224-Gbit/s 4-level pulse-amplitude-modulation (4-PAM) operation of a Hi-FIT AXEL module. In this paper, we developed a compact DC block circuit integrated into Hi-FIT AXEL module to decrease chip-power consumption without increasing the sub-assembly size and degrading the modulation bandwidth. We designed a Hi-FIT AXEL sub-assembly, that include a flip-chip interconnection board with a DC block circuit that affects the modulation bandwidth. We achieved a 3-dB bandwidth of up to 64 GHz for this designed sub-assembly. The fabricated Hi-FIT AXEL module has a 3-dB bandwidth of more than 62 GHz and a flat frequency response up to 50 GHz. For the 224-Gbit/s 4-PAM operation, the fabricated Hi-FIT AXEL module has a chip-out average output power of +10.0 dBm with a transmitter eye-closure quaternary (TECQ) of 1.9 dB. The integrated compact DC block circuit can reduce chip power consumption by up to 17%.**

***Index Terms*—Distributed-feedback (DFB) laser, EADFB laser, electroabsorption modulator (EAM), ethernet, flip-chip, semiconductor optical amplifier (SOA).**

I. Introduction

THANKS to the explosive growth of cloud applications, artificial intelligence (AI) services, and video-streaming services, data traffic is increasing rapidly. To cope with this trend, the Ethernet data rate has also been increasing. In 2021, 100-Gigabit Ethernet and 400-Gigabit Ethernet was standardized [1]. As specified in this standard, an interface with a 100-Gbit/s/λ signal (53.125-Gbaud 4-level pulse-amplitude-modulation (4-PAM)) was used. To meet this requirement, various high-speed optical transmitters have been reported, including directly modulated lasers (DMLs) [2], [3] and electroabsorption modulator integrated distributed-feedback (EADFB) lasers [4], [5], [6], [7]. With the demand for a further increase in network capacity, 800-Gbit/s and 1.6-Tb/s systems are now under discussion by the Ethernet Task Force [8]. If the number of channels decreases, the power consumption and size can decrease. Therefore, 4-channel × 200-Gbit/s/λ and 8-channel × 200-Gbit/s/λ schemes are promising candidates for compact and low power consumption 800-Gbit/s and 1.6-Tb/s systems, respectively. In the 200-Gbit/s/λ schemes, because the receiver sensitivity degrades compared with that for 100-Gbit/s/λ schemes, a higher output power is also required for a long-reach transmission system such as 10 km and beyond. Therefore, a 200-Gbit/s/λ operation optical transmitter with high output power is needed.

The 200-Gbit/s/λ operation of a DML using photon-photon resonance (PPR) has been reported [9], [10]. The DML is an attractive device because of its low power consumption. However, there are issues such as small output power and phase control difficulty. EADFB lasers [11], [12] are also attractive 200 Gbit/s/λ transmitter devices because of their simple controllability and high bandwidth. There are two issues to fabricate a high-speed and high-output power optical transmitter module using the EADFB laser. One is insufficient optical output power for a 200-Gbit/s/λ signal, beyond a 10-km transmission. The other is bandwidth degradation due to parasitic inductance, which is an issue when creating modules.

To solve these problems, we developed two key techniques. One is a semiconductor optical amplifier (SOA) assisted extended reach EADFB laser (AXEL) to increase the optical output power [13], [14]. The AXEL can increase the optical output power thanks to the SOA monolithically integrated into the AXEL chip. We will describe it in detail in Section II. The other is a high-frequency and integrated design based on the flip-chip interconnection technique (Hi-FIT) to solve the bandwidth degradation [15]. The Hi-FIT can increase the modulation bandwidth because of the wire-free interconnection technique and achieves a 214-Gbit/s/λ 4-PAM operation. We will describe it in detail in Section III. The fabricated Hi-FIT AXEL module achieved a 224-Gbit/s/λ 4-PAM operation with a chip-output optical modulation amplitude of +7.0 dBm thanks to these key techniques [16]. The termination circuit in this Hi-FIT AXEL module does not include the DC block capacitance. Therefore, the DC current flows in the termination circuit and the power consumption increases.

Manuscript received 9 November 2022; revised 19 January 2023; accepted 2 February 2023. Date of publication 6 February 2023; date of current version 16 May 2023. *(Corresponding authors: Shigeru Kanazawa; Takahiko Shindo; Mingchen Chen; Yasuhiko Nakanishi; Shohei Kosuga; Hirotaka Nakamura.)*

The authors are with the NTT Device Innovation Center, NTT Corporation, Atsugi 243-0198, Japan (e-mail: shigeru.kanazawa.vn@hco.ntt.co.jp; takahiko.shindo.xu@hco.ntt.co.jp; mingchen.chen.gn@hco.ntt.co.jp; yasuhiko.nakanishi.wy@hco.ntt.co.jp; shouhei.kosuga.er@hco.ntt.co.jp; hirotaka.nakamura.by@hco.ntt.co.jp).

Color versions of one or more figures in this article are available at https://doi.org/10.1109/JLT.2023.3242371.

Digital Object Identifier 10.1109/JLT.2023.3242371

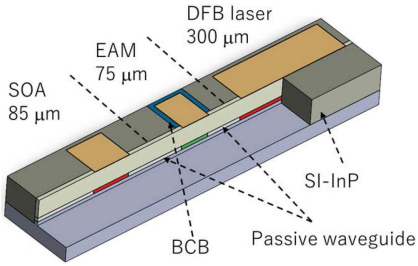

Fig. 1. Schematic structure of AXEL chip.

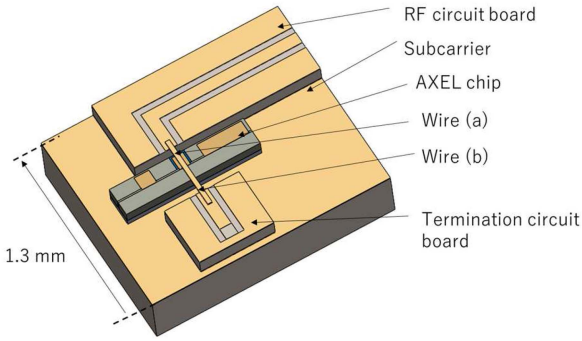

Fig. 2. Schematic structure of wire-interconnection AXEL sub-assembly.

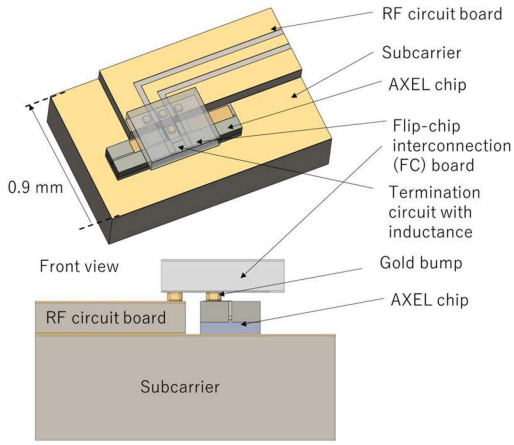

Fig. 3. Schematic structure of Hi-FIT AXEL sub-assembly.

In this paper, we developed a compact DC block circuit integrated into the Hi-FIT AXEL module [17]. In general, the DC block capacitor can block the DC current and reduce the chip's power consumption. However, the size of the DC block capacitor is large, and the DC block integrated into the sub-assembly becomes large. By mounting the DC block capacitor in three dimensions and designing a flip-chip interconnection board, we fabricated a compact DC block circuit integrated into the Hi-FIT AXEL module with a 3-dB bandwidth of 62 GHz. We successfully demonstrated a 224-Gbit/s 4-PAM operation with an average output power of +10.0 dBm and low power consumption.

II. AXEL Chip Design

Fig. 1 shows the schematic structure of an AXEL chip [13], [14]. In a conventional EADFB laser, only a DFB laser and an electroabsorption modulator (EAM) are monolithically integrated. In contrast, in an AXEL, a DFB laser, an EAM, and an SOA are monolithically integrated as shown in Fig. 1. The SOA can increase the optical modulation output power because it works as an optical post amplifier. The active regions of the SOA and DFB laser have the same structure because of the simplification of the fabrication process. When the SOA length increases, the optical modulation output power also increases, but the optical signal waveform degrades due to the increase of the amplified spontaneous emission (ASE) noise of the SOA. Based on the results of SOA length dependence of optical output power [13], we decide the length of the SOA for achieving a chip out average output power of +10 dBm. Therefore, the SOA length was set to 85 μm. To achieve a 224-Gbit/s/λ 4-PAM operation, the EAM length needs to decrease because of the decrease in the EAM's parasitic capacitance. However, when the EAM length decreases, the extinction ratio also decreases. Therefore, the EAM length was set to 75 μm for achieving a module's 3-dB bandwidth of more than 60 GHz. Benzocyclobutene (BCB) was used to fill under the EAM's electrode as it can decrease the parasitic capacitance of the EAM's electrode because it is a low dielectric material.

Passive waveguides were placed between the DFB laser and EAM section and the EAM and SOA sections by using the butt-joint process. The mesa structure was formed by the dry etching process, and a buried-heterostructure with semi-insulating indium phosphide (SI-InP) for current blocking layers was formed by using the regrowth process. An antireflection (AR) coating was deposited on the front facet and a high reflection (HR) coating was deposited on the rear facet.

III. Compact DC Block Integrated Hi-FIT AXEL Module Design

Fig. 2 shows the schematic structure of a conventional wire interconnection AXEL sub-assembly. A radio frequency (RF) circuit board, AXEL chip, and termination circuit board were mounted on a subcarrier. The width of the sub-assembly is about 1.3 mm. Wire (a) is connected between a signal line on the RF circuit board and an EAM electrode on the AXEL chip. Wire (b) is connected between the EAM electrode and termination circuit board. The parasitic inductance of Wire (a) degrades the modulation bandwidth. Therefore, the wire-free interconnection technique is needed to connect the signal line and EAM electrode. The parasitic inductance of Wire (b) causes the peaking in the frequency response. If inductance is too small or too large, the modulation bandwidth will be degraded. In addition, if inductance is too large, the peak level becomes too large, and the frequency response characteristic does not become flat. Therefore, it should be precisely designed to the length of Wire (b), which provides proper peaking in the frequency response.

To obtain a wire-free interconnection between the signal line and EAM electrode and a high-precision inductance for proper peaking, we developed Hi-FIT as shown in Fig. 3 [15], [16].

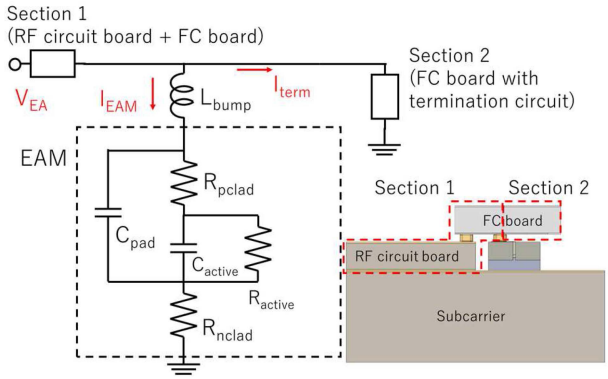

Fig. 4. Equivalent circuit of Hi-FIT AXEL sub-assembly.

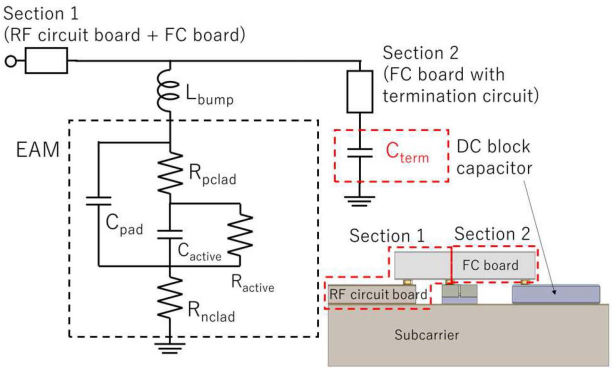

Fig. 5. Equivalent circuit of Hi-FIT AXEL sub-assembly with DC block capacitor.

As with the wire interconnection sub-assembly, the RF circuit board and AXEL chip were mounted on the subcarrier. Gold bumps were placed on the RF circuit board and EAM electrode. A flip-chip interconnection (FC) board was mounted on the gold bumps by using the flip-chip mounting technique. The FC board was integrated into a termination circuit with photolithographically controlled precision inductance corresponding to Wire (b). The width of the sub-assembly is only about 0.9 mm. The Hi-FIT does not require the wire interconnection between the signal line and EAM pad and had precise inductance that operates as a peaking controller. Therefore, the Hi-FIT provides a high modulation bandwidth and flat frequency response characteristic.

However, for the conventional Hi-FIT, there was an issue of high-power consumption. Fig. 4 shows an equivalent circuit of the Hi-FIT AXEL sub-assembly. The EAM needs to apply DC bias voltage (V_{EA}). When V_{EA} is applied, the photocurrent of the EAM (I_{EAM}) and the DC bias current (I_{term}) in a termination circuit flow. I_{EAM} needs to flow, but I_{term} does not need to flow because the termination circuit works as the RF terminator. If I_{term} does not flow, the power consumption will decrease. In general, the method of connecting a DC block capacitor in series with the termination circuit is known as a method of passing only RF signals without the DC bias current as shown in Fig. 5. Fig. 6 shows the schematic structure of a Hi-FIT AXEL sub-assembly with a DC block capacitor. The RF circuit board, AXEL chip, and DC block capacitor were mounted on the subcarrier. Gold

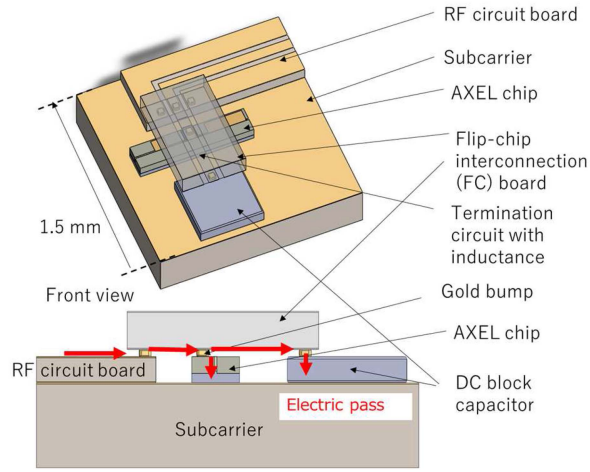

Fig. 6. Schematic structure of Hi-FIT AXEL sub-assembly with DC block capacitor.

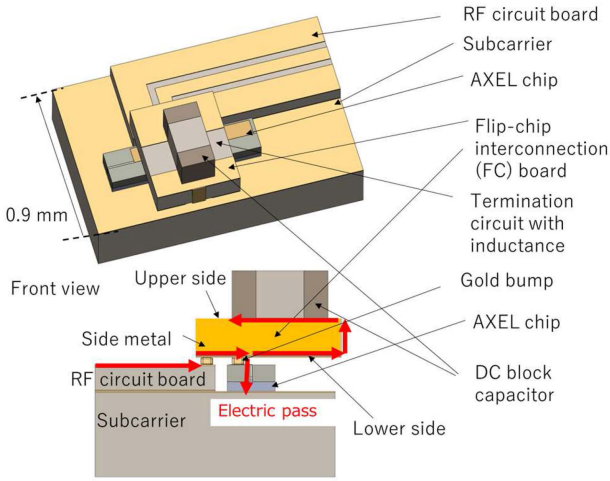

Fig. 7. Schematic structure of Hi-FIT AXEL sub-assembly with compact DC block circuit.

bumps were placed on the RF circuit board, EAM electrode, and DC block capacitor. The FC board was mounted on these gold bumps by using the flip-chip mounting technique. However, the DC block capacitor size is large because its capacitance needs to be sufficiently large to not affect the RF signal. Therefore, this sub-assembly size is large as shown in Fig. 6 and the width of this is about 1.5 mm. In addition, it is difficult to fabricate this sub-assembly because the RF circuit board, AXEL chip, and DC block capacitor are connected by only one FC board.

To solve these problems, we proposed a Hi-FIT AXEL sub-assembly with a compact DC block circuit as shown in Fig. 7 [17]. As with the wire interconnection and conventional Hi-FIT sub-assembly, the RF circuit board and AXEL chip were mounted on the subcarrier. Gold bumps were placed on the RF circuit board and EAM electrode. The FC board was mounted on the gold bumps by using the flip-chip mounting technique. The signal line width of the FC board and the gold bump diameter are 80 and 60 μm, respectively. Therefore, the mounting position accuracy of about 10 μm is required. After

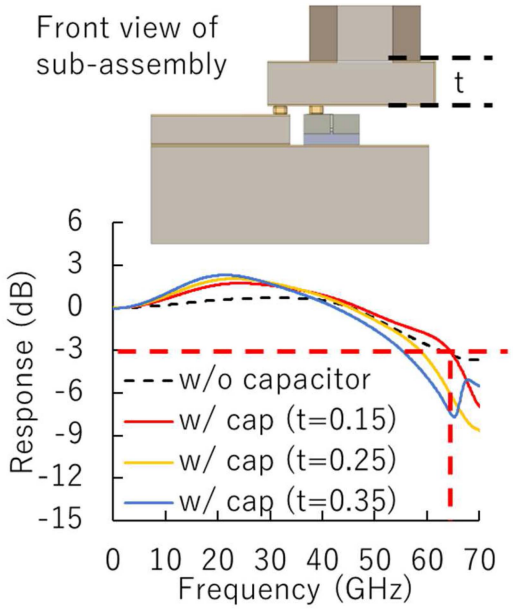

Fig. 8. Frequency responses of Hi-FIT AXEL sub-assemblies w/ and w/o DC block capacitor.

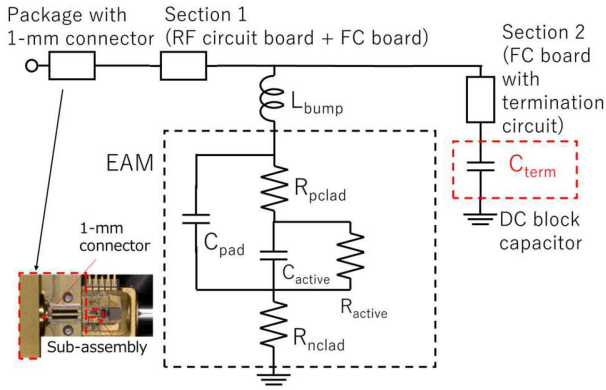

Fig. 9. Photograph and equivalent circuit of fabricated Hi-FIT AXEL module.

mounting the FC board, a surface mount type DC block capacitor was mounted on the upper side of the FC board. An upper ground (GND) pad of the FC board was connected to a lower GND one through a side metal as shown in Fig. 7. Therefore, the size of this sub-assembly can be as small as that of the conventional Hi-FIT sub-assembly without a DC block capacitor thanks to the three-dimensional arrangement of the DC block capacitor. And the width of this sub-assembly is only about 0.9 mm. The fabrication process for this sub-assembly can be as simple as that of the conventional Hi-FIT sub-assembly without a DC block capacitor. In this configuration, the heat dissipation path from the active region of the chip to the subcarrier connected to the thermo-electric cooler is the same as that of the conventional wire interconnection sub-assembly [18].

When we designed this proposed Hi-FIT AXEL sub-assembly, the thickness of the FC board is one of the key points to obtain a high modulation bandwidth. The electrical signal that entered the FC board in Fig. 7 transmitted from the lower side in the FC board to the upper side via the side. After that, the signal was transmitted to the GND pad on the FC board's upper side through the DC block capacitor. Therefore, when the thickness of the FC board increases, the length of the signal line to the DC block capacitor, corresponding to Wire (b) in Fig. 2, becomes longer and the peak level increases. If the FC board thickness becomes too thin, the electromagnetic fields from the signal line on the lower side of the FC board will be strongly coupled to the GND of the upper side, the characteristic impedance will decrease, and the frequency response will degrade. Therefore, to achieve a sufficient modulation bandwidth for a 200-Gbit/s/λ operation, we calculate the frequency responses of the Hi-FIT AXEL sub-assembly with the compact DC block circuit using the equivalent circuit as shown in Fig. 5. Fig. 8 shows the FC board thickness dependence of the calculated frequency responses of the sub-assemblies. The C_{active}, C_{pad}, C_{term}, R_{active}, R_{pclad}, R_{nclad}, and L_{bump} were 0.09, 0.05 pF, 100 nF, 110, 20, 2 ohm, and 0.03 nH, respectively. The S-parameters of the Sections I and II were calculated by using the 3-dimensional electromagnetic field simulator. The width of the signal line on the FC board and the gap between the signal line and ground were set to be 80 and 40 μm, respectively. Therefore, to avoid affecting the characteristic impedance, the thickness was set to 0.15 mm or more. The FC board contains a high-impedance transmission line with characteristic impedance of more than 50 ohm as a peaking controller. The length of this line is about 0.35 mm. For comparison, we also calculated the frequency response of the Hi-FIT AXEL sub-assembly without the DC block capacitor (cap) using the equivalent circuit as shown in Fig. 4. The 3-dB bandwidths of the sub-assemblies with thicknesses of 0.15, 0.25, and 0.35 mm are 64, 58, and 55 GHz, respectively. Dips in the frequency response of the sub-assembly with a thickness of 0.35 mm occur due to the resonance in the FC board substrate. Therefore, the substrate thickness was set to be 0.15 mm. The designed sub-assembly has a good frequency response characteristic compared with that of the sub-assembly without a DC block capacitor.

We fabricated the designed Hi-FIT AXEL module as shown in Fig. 9. The capacitance of the DC block (C_{term}) was set to 100 nF in order not to affect the PRBS signal. The capacitance is made of ceramic and is 0.2 mm $\times$ 0.4 mm in size. The designed Hi-FIT AXEL sub-assembly was mounted in this module and a 1-mm connector was used as an RF interface. We calculated the frequency response of the compact DC block circuit integrated Hi-FIT AXEL module using an equivalent circuit as shown in Fig. 9 and measured the E/O response of the fabricated module. Fig. 10 shows the measured and simulated E/O responses of the Hi-FIT AXEL module. The laser diode (LD) and SOA currents were 80 and 30 mA, respectively, and the EA bias voltage was -1.43 V. The chip temperature was 45°C. The measured 3-dB bandwidth exceeded 62 GHz and the measured E/O response was sufficiently flat up to 50 GHz. The peaking level of the measurement result is slightly smaller than that of the simulation one due to distributed micro parasitic components, such as capacitance, inductance, and resistance, not considered in the simulation model.

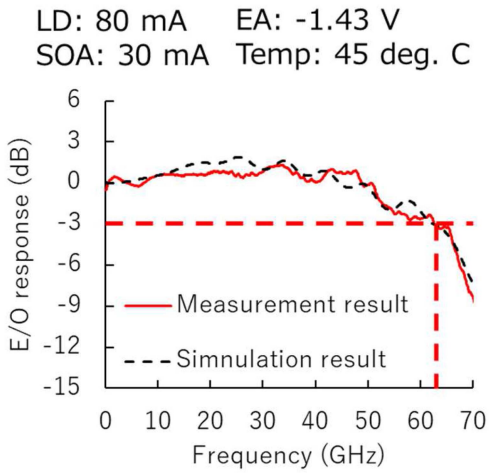

Fig. 10. Measured and simulated E/O responses of Hi-FIT AXEL module.

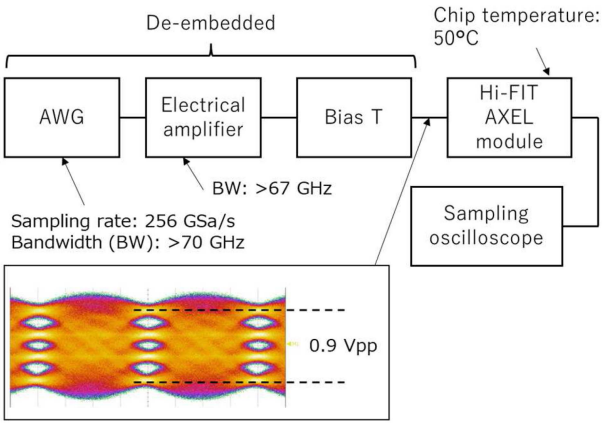

Fig. 11. Measurement setup for 224-Gbit/s 4-PAM operation.

IV. 224 GBIT/S OPERATION OF DESIGNED HI-FIT AXEL MODULE

We measured the optical modulation amplitudes (OMAs), eye diagrams, and transmitter eye-closure quaternaries (TECQs) using the fabricated compact DC block circuit integrated Hi-FIT AXEL module under a 224-Gbit/s 4-PAM operation. Fig. 11 shows the measurement setup for the 224-Gbit/s 4-PAM operation. The electrical signal was generated from an arbitrary waveform generator (AWG) with a sampling rate of 256 GSa/s and a bandwidth of over 70 GHz. The AWG generates a 224-Gbit/s 4-PAM signal with a pattern of short stress pattern random quaternary (SSPRQ). The electrical signal was amplified by an electrical amplifier (SHF M827) with a bandwidth of over 67 GHz. The amplitude voltage of the amplified electrical signal was 0.9 Vpp after de-embedding the frequency response characteristic of the AWG, the electrical amplifier and a bias T as shown in Fig. 11. After passing through the bias T, the amplified electrical signal was converted to an optical signal by using the fabricated Hi-FIT AXEL module. The chip temperature was set to 50°C. The optical eye diagrams and TECQs were measured by using a sampling oscilloscope with a 5-tap finite impulse response filter. When we measured the TECQs, the target symbol rate was set to 7.8E-3, which corresponds to the forward error correction (FEC) limit using a 7%-overhead hard-decision FEC code [19].

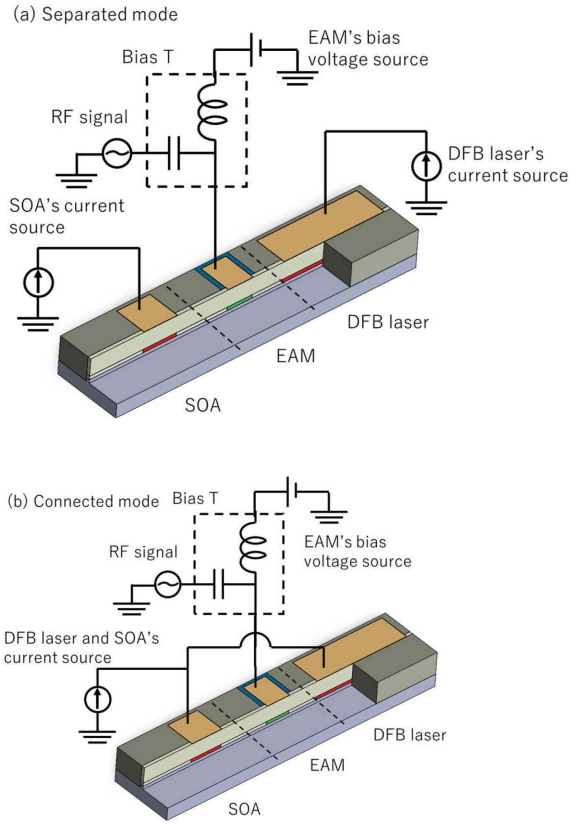

Fig. 12. (a) Driving circuits for AXEL in separetaed mode. (b) Driving circuits for AXEL in connected mode.

In these measurements, the LD and SOA were driven in two operating states, separated mode and connected mode, as shown in Fig. 12. In the separated mode, as shown in Fig. 12(a), the DFB laser and SOA are electrically separated and driven by independent current sources, enabling their values to be set independently, however, the electrical terminals are increased compared with the conventional EADFB laser. In the connected mode as shown in Fig. 12(b) [20], the DFB laser and SOA are electrically connected in parallel, enabling the number of the electrical terminals to be the same as that of the conventional EADFB laser, however, the current ratio between the DFB laser and SOA cannot be changed.

Fig. 13 shows the 224-Gbit/s 4-PAM eye diagrams, average output powers at chip output (P_{avg}), extinction ratios (ERs), and TECQs for a back-to-back configuration (BtoB). In the separated mode, the SOA current was changed from 10 to 50 mA at 10 mA interval, and the sum of the SOA and LD currents was 100 mA uniformly. In the connected mode, the sum of the SOA and LD currents was set at 100 mA. The EA bias voltage was adjusted to maintain an extinction ratio of about 4.0 dB. The chip-output average output power was calculated by subtracting the measured coupling loss of 2.2 dB from the measured module output power. For all eye diagrams, we obtained clear eye openings. Fig. 14 shows the SOA current dependence of the average output power from chip out and TECQ. With SOA and

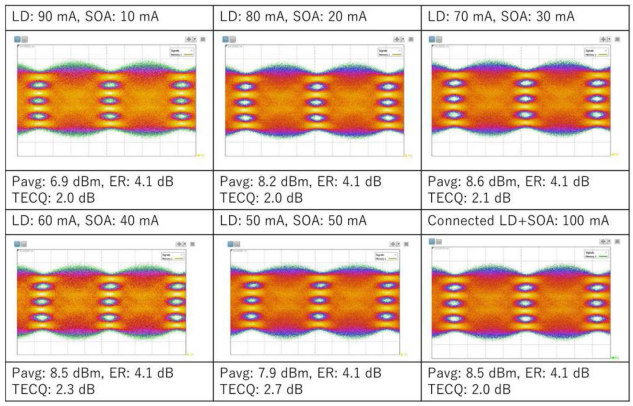

Fig. 13. 224-Gbit/s 4-PAM eye diagrams for BtoB configuration.

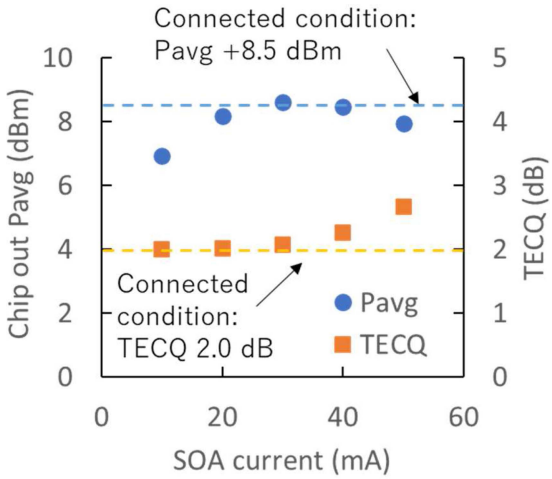

Fig. 14. SOA current dependence of average output power and TECQ.

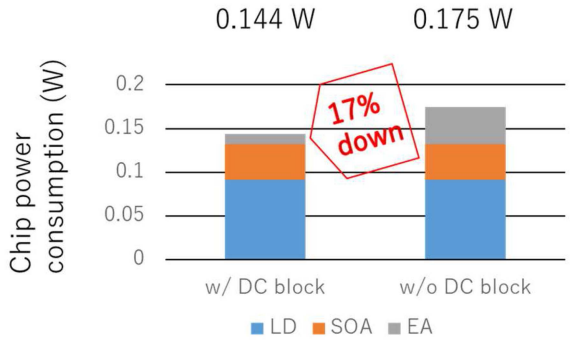

Fig. 15. Chip power consumption comparison of Hi-FIT AXEL module w/ and w/o DC block circuit.

DFB laser currents of 30 and 70 mA, respectively, the chip out average output power was +8.6 dBm and the TECQ was 2.1 dB. The average output power in the connected mode was similar to the maximum average output power in the separated mode, and the TECQ was similar. Fig. 15 shows a comparison of chip power consumption of the Hi-FIT AXEL module with and without the DC block circuit. The SOA and DFB laser currents, which were the conditions for maximum average output power, were set to 30 and 70 mA, respectively. The chip power consumptions of the module with and without the DC block circuit were 0.144 and

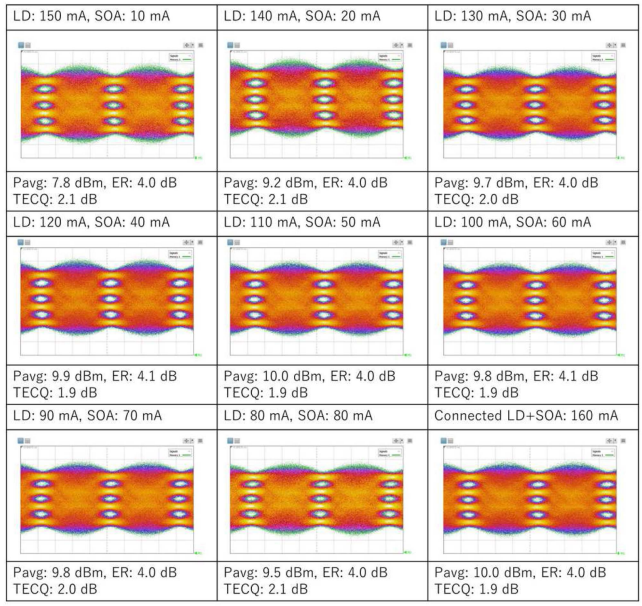

Fig. 16. 224-Gbit/s 4-PAM eye diagrams for BtoB configuration.

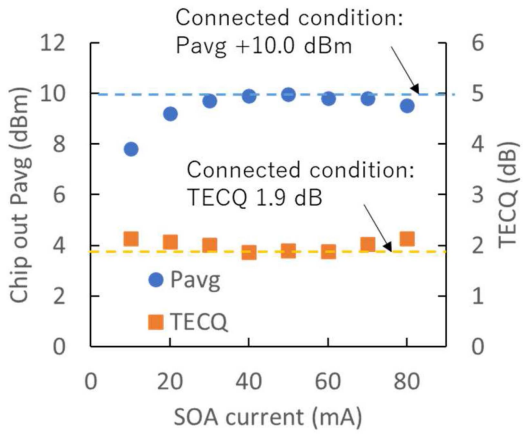

Fig. 17. SOA current dependence of average output power and TECQ.

0.175 W, respectively. As a result, the DC block circuit could reduce the chip power consumption by up to 17%.

Fig. 16 shows 224-Gbit/s 4-PAM eye diagrams, average output powers at chip output, ERs, and TECQs for a BtoB. In the separated mode, the SOA current was changed from 10 to 80 mA at 10 mA intervals, and the sum of the SOA and LD currents was 160 mA uniformly to achieve the average output power of more than +10.0 dBm. In the connected mode, the current value of the DFB laser and SOA was set to 160 mA. The EA bias voltage was adjusted to maintain an extinction ratio of about 4.0 dB. For all eye diagrams, we also obtained clear eye openings. Fig. 17 shows the SOA current dependence of average output power and TECQ. With SOA and DFB laser currents of 50 and 110 mA, respectively, the average output power was +10.0 dBm and the TECQ was 1.9 dB. The average output power in connected mode was similar to the maximum average output power in separated mode, and the TECQ was similar. Fig. 18 shows a comparison of the chip power consumption of the Hi-FIT AXEL module

Fig. 18. Chip power consumption comparison of Hi-FIT AXEL module w/ and w/o DC block circuit.

with and without a DC block, which were 0.257 and 0.294 W, respectively. As a result, the DC block circuit could reduce the chip power consumption by up to 12%.

V. Conclusion

We designed and fabricated a Hi-FIT AXEL module with a compact DC block circuit. The Hi-FIT can increase the modulation bandwidth thanks to the wire-free interconnection technique and precise peaking control technique. The AXEL can increase the modulation output power thanks to the SOA monolithically integrated in the AXEL chip. The compact DC block circuit can decrease the chip power consumption without increasing the size of the sub-assembly. The fabricated Hi-FIT AXEL module achieved a 3-dB bandwidth of more than 62 GHz. For a 224-Gbit/s 4-PAM operation, the clear eye opening was obtained and a chip out average output power of +10 dBm was obtained with a TECQ of 1.9 dB. The compact DC block circuit can reduce chip power consumption by up to 17%. The fabricated Hi-FIT AXEL module with the compact DC block circuit is a promising low power consumption and high-output power 200-Gbit/s/λ optical transmitter for long-reach applications.

References

[1] *IEEE Standard for Ethernet - Amendment 11: Physical Layers and Management Parameters for 100 Gb/s and 400 Gb/s Operation over Single-Mode Fiber at 100 Gb/s per Wavelength*, IEEE 802.3cu-2021, 2021.
[2] Y. Matsui et al., "55-GHz bandwidth short-cavity distributed reflector laser and its application to 112-Gb/s PAM-4," in *Proc. Opt. Fiber Commun. Conf.*, 2016, Paper Th5B–4.
[3] N. Sasada et al., "Wide-temperature-range ((25°C to 80°C) 53-Gbaud PAM4 (106-Gb/s) operation of 1.3-μm directly modulated DFB lasers for 10-km transmission," *J. Lightw. Technol.*, vol. 37, no. 7, pp. 1686–1689, 2019.
[4] S. Kanazawa et al., "Flip-chip interconnection lumped-electrode EADFB laser for 100-Gb/s/λ transmitter," *IEEE Photon. Technol. Lett.*, vol. 27, no. 16, pp. 1699–1701, Aug. 2015.
[5] E. E. Fiky et al., "First demonstration of a 400 Gb/s 4λ CWDM TOSA for datacenter optical interconnects," *Opt. Exp..*, vol. 26, no. 16, pp. 19742–19749, 2018.
[6] Y. Nakai et al., "Uncooled operation of 53-GBd PAM4 (106-Gb/s) EA/DFB lasers with extremely low drive voltage with 0.9 Vpp," *J. Lightw. Technol.*, vol. 37, no. 7, pp. 1658–1662, 2019.
[7] R. Fujihara, M. Shirao, S. Nakamura, S. Nakano, and K. Hasegawa, "A cost effective hermetically sealed 106 Gbit/s PAM4 EML TO-CAN for beyond-5G mobile fronthaul," in *Proc. Eur. Conf. Opt. Commun.*, 2020, pp. 1–4.
[8] IEEE P802.3df 200 Gb/s, 400 Gb/s, 800 Gb/s, and 1.6 Tb/s Ethernet Task Force, 2022. [Online]. Available: https://www.ieee802.org/3/df/
[9] S. Yamaoka et al., "Directly modulated membrane lasers with 108 GHz bandwidth on a high-thermal-conductivity silicon carbide substrate," *Nature Photon..*, vol. 15, pp. 18–35, 2021.
[10] Y. Matsui, R. Schatz, D. Che, F. Khan, M. Kwakernaak, and T. Sudo, "Low-chirp isolator-free 65-GHz-bandwidth directly modulated lasers," *Nature Photon.*, vol. 15, pp. 59–63, 2021.
[11] H. Mardoyan et al., "204-GBaud on-off keying transmitter for inter-data center communications," in *Proc. Opt. Fiber Commun. Conf. Expo.*, 2018, pp. 1–3.
[12] S. Yamauchi et al., "224-Gb/s PAM4 uncooled operation of lumped-electrode EA-DFB lasers with 2-km transmission for 800GbE application," in *Proc. Opt. Fiber Commun. Conf. Exhib.*, 2021, pp. 1–3.
[13] W. Kobayashi et al., "Novel approach for chirp and output power compensation applied to a 40-Gbit/s EADFB laser integrated with a short SOA," *Opt. Exp.*, vol. 23, no. 7, pp. 9533–9542, 2015.
[14] T. Shindo et al., "High power and high speed SOA assisted extended reach EADFB laser (AXEL) for 53-Gbaud PAM4 fiber-amplifier-less 60-km optical link," *J. Lightw. Technol.*, vol. 38, no. 11, pp. 2984–2991, Jun. 2020.
[15] S. Kanazawa et al., "214-Gb/s 4-PAM operation of flip-chip interconnection EADFB laser module," *J. Lightw. Technol.*, vol. 35, no. 3, pp. 418–422, 2017.
[16] S. Kanazawa, T. Shindo, M. Chen, Y. Nakanishi, H. Nakamura, and H. Matsuzaki, "224-Gbit/s 4-PAM operation of a high-modulation-bandwidth high-output-power Hi-FIT AXEL transmitter," *Opt. Lett.*, vol. 47, no. 12, pp. 3019–3022, 2022.
[17] S. Kanazawa, T. Shindo, M. Chen, Y. Nakanishi, and H. Nakamura, "Low-power-consumption Hi-FIT AXEL transmitter integrated with compact DC block circuit for 200Gbit/s/application," in *Proc. 27th OptoElectron. Commun. Conf.*, 2022, pp. 1–3.
[18] S. Kanazawa et al., "Compact flip-chip interconnection 112-Gbit/s EADFB laser array module with high eye-mask margin," *J. Lightw. Technol.*, vol. 32, no. 1, pp. 115–121, 2014.
[19] Forward error correction for high bitrate DWDM submarine systems, ITU-T G.975.1, 2004. [Online]. Available: https://www.itu.int/rec/T-REC-G.975-200010-I/en
[20] W. Kobayashi et al., "Low-power consumption 28-Gb/s 80-km transmission with 1.3-μm SOA-assisted extended-reach EADFB laser," *J. Lightw. Technol.*, vol. 35, no. 19, pp. 4297–4303, Oct. 2017.

Shigeru Kanazawa (Senior Member, IEEE) received the B.E., M.E., and Ph.D. degrees in electronic engineering from the Tokyo Institute of Technology, Tokyo, Japan, in 2005, 2007 and 2016, respectively. In April 2007, he joined Nippon Telegraph and Telephone (NTT) Photonics Laboratories (now NTT Device Innovation Center), Atsugi, Japan. He is engaged in research and development of optical semiconductor devices and integrated devices for optical communications systems. Dr. Kanazawa is a Senior Member of the Photonics Society and Institute of Electronics, Information and Communication Engineers of Japan, and a Member of the Japan Society of Applied Physics and Japan Institute of Electronics Packaging.

Takahiko Shindo (Member, IEEE) received the B.E., M.E., and Ph.D. degrees in electrical and electronic engineering from the Tokyo Institute of Technology, Tokyo, Japan, in 2008, 2010, and 2012, respectively. After the Ph.D. degree, he was a Research Fellow with the Japan Society for the Promotion of Science. In April 2013, he joined Nippon Telegraph and Telephone (NTT) Photonics Laboratories (now NTT Device Innovation Center), NTT Corporation, Kanagawa, Japan, where he is currently engaged in research on optical semiconductor devices. Dr. Shindo is a Member of the IEEE Photonics Society, Japan Society of Applied Physics, and the Institute of Electronics, Information and Communication Engineers. From 2010 to 2012, he received a research fellowship for young scientists from the Japan Society for the Promotion of Science.

Mingchen Chen received the B.E. and M.E. degrees in electronic engineering from the University of Electro-Communications, Chofu, Japan, in 2010 and 2012, respectively, and the Ph.D. degree in engineering from the University of Electro-Communications, Chofu, Japan, in 2015, and joined NTT Device Technology Labs, NTT Corporation the same year. He is currently engaged in research and development of semiconductor optical devices.

Yasuhiko Nakanishi received the B.E. and M.E degrees from Hokkaido University, Sapporo, Japan, in 2000 and 2002, respectively. In 2002, he joined the NTT Access Network Service Systems Laboratories, Chiba, Japan, where he was involved in research and development of optical communication systems and devices. He is currently with NTT Device Innovation Center, Kanagawa, Japan. He is a Member of the Photonics Society, Institute of Electronics, Information and Communication Engineers, Japan.

Shohei Kosuga received the B.E., M.E., and Ph.D. degrees in electronic engineering from Aoyama Gakuin University, Tokyo, Japan, in 2016, 2018, and 2021, respectively. He received the Japan Society for the Promotion of Science research fellowships for young scientists in 2019 and 2020. He joined the Nippon Telegraph and Telephone Device Innovation Center, Japan. He is currently engaged in the research and development of ultrafast opt-electronic devices. He is a Member of the Japan Society of Applied Physics and Institute of Electronics, Information and Communication Engineers of Japan.

Hirotaka Nakamura received the B.E. degree in applied physics from the University of Tokyo, Tokyo, Japan, in 1999, and the Ph.D. degree from Hokkaido University, Hokkaido, Japan, in 2011. In 1999, he joined NTT Access Network Service Systems Laboratories, Japan, where he was engaged in research on optical technologies of high-speed passive optical networks. Since 2020, he has been with NTT Device Innovation Center, where he is engaged in the research and development of laser diodes, photo diodes, and analog ICs for optical metro and access networks. He is a Member of the Institute of Electronics, Information and Communication Engineers of Japan. Since 2009, he has been participating in ITU-T and FSAN.