Path-Independent Insertion Loss 8 × 8 Silicon Photonics Switch With Nanosecond-Order Switching Time

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***Abstract*—Silicon photonic switches with integrated p-i-n junctions can exhibit fast switching on the order of nanoseconds, enabling prospective optical networks with very fast reconfiguration times. However, carriers injected through the p-i-n junction cause extra loss, which can increase insertion loss, degrade uniformity and cause crosstalk. In this paper, we show that a path-independent insertion loss (PILOSS) switch with integrated p-i-n junctions can achieve uniform and very low on-chip insertion loss (3.8 ± 0.19 dB) with strictly non-blocking characteristics. The switching time of our switch is <12.5 ns and <6.1 ns for 10%–90% and 10%–80% rise/fall times, respectively, and the optical crosstalk can be suppressed by more than 20 dB for a bandwidth of >31 nm for the worst case.**

***Index Terms*—Optical networks, optical switch, silicon photonics.**

I. Introduction

THE rapid growth of cloud computing workloads including machine learning (ML) applications is creating a constant demand for more powerful and efficient cloud datacenters (DCs). One of the ultimate ways to realize efficient DCs with high resource utilization is *full disaggregation* of the DCs, in which hardware resources such as CPUs and memory are disaggregated and allocated dynamically to fit to the workload [1]. Realizing such fully disaggregated DCs requires broad-bandwidth optical interconnections (e.g. >400 Gb/s) with extremely small latency (e.g. <100 ns) between CPUs and memory, which is not technologically possible at this point [1]. Fast and large-scale optical switches would be key components in such networks. Considering that a receiver's phase-locking time will range from 2.6 to 18.5 ns [2], [3], such optical switches should have a reconfiguration time on the order of nanoseconds. Furthermore, scalability to a large number of optical ports is very important. In particular, the formation of a Clos network [4] of multiple *strictly non-blocking* switches would be a straightforward way to construct a large-scale optical switching network as this approach is already used in modern DC networks.

Silicon (Si) photonics-based optical switches are promising candidates for realizing such high-radix, broadband and fast optical networks, because they offer an ultra-small footprint, high reliability and very high productivity by utilizing complementary metal-oxide-semiconductor (CMOS) process lines [5].

To obtain a nanosecond-order switching time, the electro-optic (EO) effect should be used, in which the free-carrier density in the Si waveguide is modulated using p-i-n junctions [5], [6], [7], [8], [9], [10]. The EO effect is useful for obtaining a fast reconfiguration time, in contrast to the thermo-optic (TO) effect and MEMS-based optical switches which have switching times on the order of microseconds [11], [12]. EO-based switches generally have large losses of approximately 1 dB per Mach–Zehnder interferometer (MZI) element switch, in contrast to TO-based switches which have an approximately 0.1 dB loss per MZI [12].

The loss in an EO-based switch originates from carrier plasma absorption (CPA), which arises when we inject carriers into EO-based phase shifters, i.e., when the phase shifter (and the MZI) is 'on' [9]. CPA not only causes large accumulated loss, but also inter-port crosstalk due to unbalanced optical power at the couplers in an MZI. Therefore, it is beneficial for EO-based optical switches if the number of 'on' MZIs is as small as possible.

Previous demonstrations of Si EO switches have used a Beneš or double-layer network (DLN) topology [6], [7], [8], [10], [13]. The Beneš topology is not strictly non-blocking and therefore is not suited for large-scale implementations with a Clos network structure. Although a DLN is strictly non-blocking, the topology potentially has a considerable number of 'on' MZIs on a path, as shown in Fig. 1(a), leading to a large path-dependent loss.

Here, we investigate the use of a path-independent insertion loss (PILOSS) topology [14] in EO-based silicon photonic switches [15]. The PILOSS topology, in contrast to the DLN topology, has exactly one 'on' MZI on any path, as shown in Fig. 1(b). Therefore, when used with EO-based phase shifters, it has low and uniform loss for any path setting. Moreover, the leaked portion of light at the 'on' MZI (illustrated by

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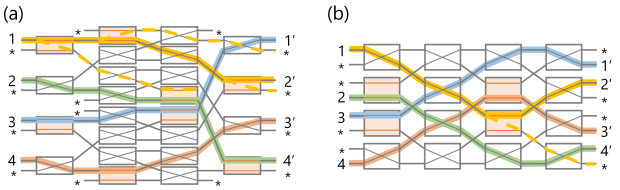

Fig. 1. Schematic illustrations of (a) a 4 × 4 DLN topology and (b) a 4 × 4 path-independent insertion loss (PILOSS) topology. Idle ports are indicated by asterisks.

TABLE I
COMPARISON BETWEEN DLN AND PILOSS TOPOLOGY

Item	DLN-based EO	PILOSS-based EO
Number of 'on' MZIs on a path	0 to $2\log_2 N - 1$	1
Inter-port crosstalk	Low	Low
Power consumption	$\propto N \times \log_2 N$	$\propto N$
Number of MZIs on a path	$2\log_2 N$	N

yellow dashed lines in Fig. 1(b)) can be directed to the *idle* ports, which are terminated on chip, suppressing inter-port crosstalk.

Table I compares several characteristics between the DLN and PILOSS topologies. The number of 'on' MZIs on a path varies in the DLN topology, while it is constant in the PILOSS topology. Inter-port crosstalk can be suppressed in both schemes because they can be guided to *idle* ports as shown in Fig. 1. The PILOSS topology has a lower power consumption than the DLN topology. Although the total number of MZIs on a path is larger in PILOSS, we consider that this has a small impact on the overall characteristics, because the 'off' MZIs, when appropriately designed, have a much smaller insertion loss than 'on' MZIs. Thus, we consider that the PILOSS topology is suited for use with EO-based phase shifters.

In this paper, we detail the fabrication and demonstrate the operation of an 8 × 8 Si photonic EO-based optical switch with a nanosecond-order switching time [15]. We then show the results of dynamic switching measurements of 60 MZIs on the chip and discuss plans to expand the device.

In Section II, we show the detailed design and fabrication methods for the EO-based phase shifters and the switch. We then describe the results of static and dynamic performance measurements in Section III. Section IV discusses future improvements in device performance. Finally, Section V concludes this paper.

II. Device Design and Fabrication

Fig. 2(a) shows a schematic of the 8 × 8 silicon photonic switch based on PILOSS topology. We integrated both EO and TO phase shifters on each arm of the MZI. The details of the EO phase shifter are given in the next paragraph. For the TO phase shifter, we used TiN-film heaters patterned on the clad of the Si waveguide. We used output-port-exchanged MZIs to expand the crosstalk bandwidth in the PILOSS topology [16].

The structure of the EO phase shifter is shown in Fig. 2(b), and is based on a rib-type Si waveguide integrated with a lateral p-i-n junction. This structure is basically an injection-type phase shifter. Although depletion-type phase shifters generally have faster responses than injection-type phase shifters, they typically have smaller modulation depths with moderate (1 ∼ 2 V) operating voltages, which can lead to longer devices. Especially for the switches the compactness of the phase shifter is important because we need to put many phase shifters on the chip. Moreover, the intrinsic loss of the injection-type phase shifters can be very small because the waveguide core is not doped. With these reasons, we used injection-type phase shifter for our switch device. The waveguide height was 220 nm, while the slab height was 50 nm. The *p*++ and *n*++ regions were formed by doped impurities with densities of approximately $10^{20}\mathrm{cm}^{-3}$. The intrinsic (i) region was extended from the edge of the waveguide by an amount d_{pn} in order to reduce the loss without carrier injection. Fig. 2(c) shows the calculated electric-field (E_x) distribution for the phase shifter. As shown in this figure, the electric field does not overlap the *p*++ and *n*++ regions, which ensures low loss. Fig. 2(d) shows the calculated intrinsic insertion loss for the doped regions, where losses corresponding to the accumulation of 1, 4 and 10 phase shifters were considered. As shown in this figure, when we set d_{pn} to be 0.55 μm, the loss due to the doped regions can be negligible, thus enabling low insertion loss for the switch. The length of the EO phase shifter was 250 μm. We note that this length is determined to be as small as possible to reduce the loss and the device size. However, it should also be large enough to obtain π-phase shift with moderate operation voltages (1 ∼ 2 V).

The waveguide crossings of Fig. 2(a) were realized by using fully-etched, adiabatically widened multimode waveguides proposed in [17].

We then fabricated the Si chip using a CMOS process line equipped with ArF immersion lithography on a 300-mm SOI wafer. After dicing the Si chip, we bonded it on the 304-pin PGA package, as shown in Fig. 2(e). The chip size was 13 mm × 13 mm. All the EO and TO phase shifters were electrically connected to the package pins using wire bonds. Finally, we attached 20 arrays of high-Δ fibers to the edge of the Si chip, where we designed tapered spot-size converters (SSCs) on the Si waveguide.

III. Device Characterization

In this section, we describe the results of static and dynamic measurements of the fabricated device.

A. Static Loss Measurement

Here, we show the static characteristics of the fabricated 8 × 8 switch. Fig. 3(a) shows the measurement setup. We used a wavelength-tunable laser diode (LD), a 1 × 8 selector, eight fiber polarization controllers (FPCs) and eight-channel photodetectors (PDs). FPCs were required because the device was designed only for the transverse-electric (TE)-like polarization component. All 128 TO phase shifters (heaters) on the chip were electrically connected to a 128 channel heater driver through a fan-out printed circuit board (PCB). We used either eight-channel digital-to-analog converters (DACs) or two-channel pulse sources to measure the static or dynamic characteristics of the device, respectively.

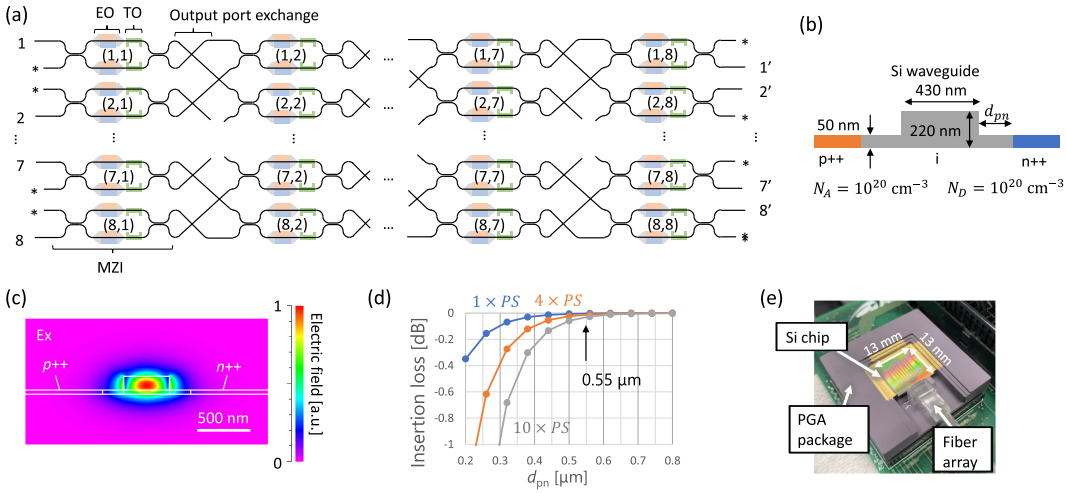

Fig. 2. (a) Schematic of 8 × 8 EO-based PILOSS optical switch. The *idle* ports are indicated by asterisks. (b) Illustration of cross-section of EO-based phase shifter. (c) Calculated electric-field distribution for EO-based phase shifter. (d) Calculated loss through the phase shifters, where accumulation of 1, 4, and 10 phase shifters (PSs) are considered by changing the distance between the waveguide edge and the *p, n* region (d_{pn}). (e) Photograph of fabricated Si photonic chip, mounted on a 304-pin PGA package together with an edge-attached fiber array.

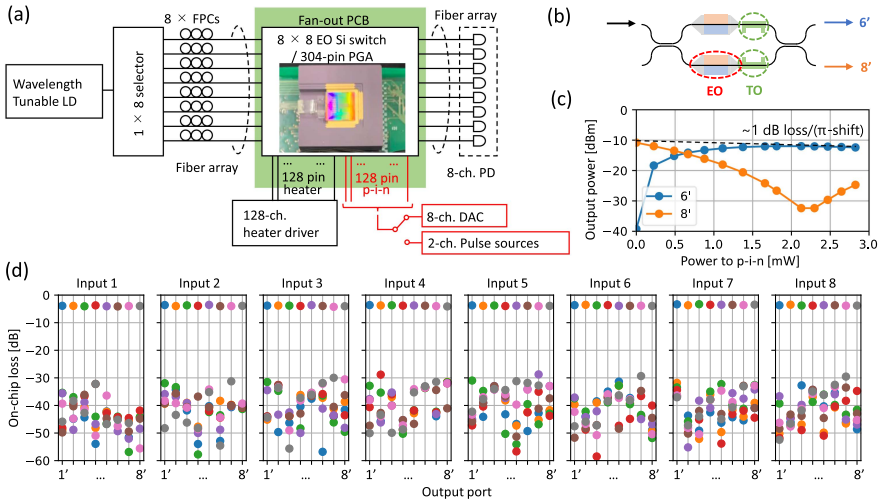

Fig. 3. (a) Schematic of measurement setup. LD = laser diode, FPC = fiber polarization controller, PCB = printed circuit board, DAC = digital-to-analog converter, PD = photodetector. (b) Illustration of setup used to measure single-MZI switching by EO phase shifter. (c) Results of single-MZI switching experiment. (d) Results of an all-path-setting transmittance measurement showing uniform insertion loss and suppression of leakage. The y-axis shows the on-chip loss.

Before starting the measurement, we trimmed initial phase errors caused by fabrication errors by manually tuning the heating amount to each TO phaser shifter. The average electrical power required for the phase trimming was 11.0 mW per an MZI, corresponding to ∼1.5 V. This trimming power (voltage) was larger than our previous demonstrations of the TO-based silicon photonics switch (1.27 mW) [12]. We consider the reason as follows. The amount of initial phase error highly depends on the lithography technique. In our previous result, we used ArF immersion lithography which had high precision [12]. In this work we also used the ArF immersion lithography to form Si channel-type waveguides, but only the EO phase shifters were fabricated using KrF lithography, which have relatively degraded precision. Therefore, the initial error we had was larger, resulting in larger trimming power. This issue could be solved by using ArF immersion lithography to form the EO phase shifters.

We then input continuous-wave (CW) light at input port 1 of Fig. 2(a) and guided it to the (7,7)-th MZI, which is illustrated in Fig. 3(b). We first configured the MZI so that the light is guided to output 8' without injection of carriers to the EO phase shifter. We then injected various currents into the EO phase shifter to change the switching state. Fig. 3(c) shows the observed output power to outputs 6' and 8' of the chip as functions of the input power to the p-i-n junction. Here, the π shift was observed with a power of 2.3 mW. This power consumption is much smaller than that for TO phase shifters (approximately 20 mW). Therefore, the EO-based switch is considered to have better scalability. Also, an approximately 1 dB loss increase was observed for the EO-based MZI element at the π-shift or 'on' state, as expected from earlier works [8], [9].

We then configured all $64(= 8 \times 8)$ path settings and measured the on-chip transmittance to the eight output ports while

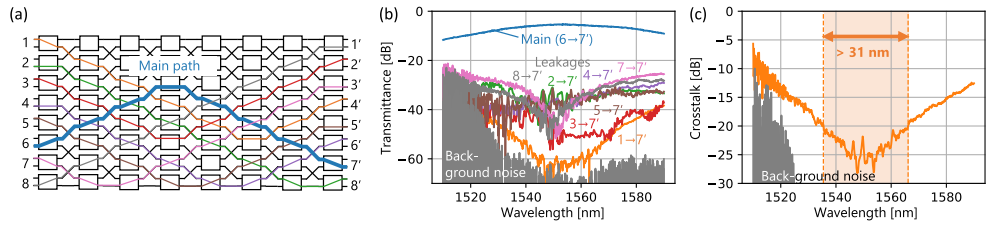

Fig. 4. (a) Schematic illustration of one of the worst-crosstalk path settings, where the blue lines show the main path. (b) Measured results of the main path transmission, plotted together with leakages from the other ports to the main path. (c) Calculated worst-case crosstalk of the switch, where a $>$ 31 nm bandwidth was observed with $>$ 20 dB crosstalk suppression.

injecting currents to the corresponding *p-i-n* junctions. The results are shown in Fig. 3(d), where each panel corresponds to an input port, the x-axis shows the measured output port, and the colors of the points correspond to different path settings. The points around -4 dB in the figure correspond to target-port outputs. From these points, we can see that all the EO phase shifters worked well and the on-chip insertion loss to all path settings was 3.80 dB $\pm$ 0.19 dB, which was small and very uniform. The minimum loss was 3.30 dB. Moreover, leakage of light to unintended ports was suppressed, as shown in the figure, leading to low crosstalk.

The breakdown of the insertion loss is shown below. The fiber-to-chip coupling loss was approximately 3 dB per facet, which was excluded from the results above. We note that this value can be improved to 1.4 dB per facet by using high-Δ PLC connectors [12]. On-chip waveguides, with a loss of approximately 1.5 dB, were used to connect the SSCs at the chip edge and the switch matrix. There was only one 'on'-state MZI, which had a loss of approximately 1 dB. The remaining seven 'off'-state MZIs had a loss of 0.1 dB each. Summarizing, the on-chip loss was 3.3 dB at minimum. The fluctuations of the on-chip loss are considered to originate from errors in the initial phase trimming and from fluctuations in the coupling loss.

B. Crosstalk Measurement

Here, we measure the crosstalk characteristics of the switch. Fig. 4(a) shows a schematic of one of the worst crosstalk settings on the switch. The blue lines show the main path (6–7'), where the leakages from the other paths (1–4,' 2–8,' 3–2,' 4–6,' 5–5,' 7–3,' 8–1') accumulate. We configured the switch to have these path settings and measured the spectra of the main path and the leakages from the other paths to the main path. The results are shown in Fig. 4(b), where the background noise associated with the spectrum analyzer is also plotted. We consider that the difference in spectra in each leakages, which are denoted by 2–7,' 3–7,' and so on, in the Fig. 4(b), is originated from imperfect phase trimming and fabrication errors at the 3-dB couplers of the MZIs.

We integrated all the leakages from the other paths to the main path, and subtracted the result from the main path transmittance to obtain the accumulated worst-case crosstalk, plotted in Fig. 4(c). The figure shows that the crosstalk bandwidth was more than 31 nm with a crosstalk suppression ratio of $>$20 dB.

C. Dynamic Performance Measurement

Finally, we measured the dynamic characteristics of the 8×8 optical switch. Here, we configured the switch to have an optical connection from 1 to 8,' as shown in Fig. 5(a). We then input a positive edge to the (7,7)-th MZI and a negative edge to the (8,8)-th MZI to switch the optical path from 1–8' to 1–6'. We used two-channel pulse generators to produce these two pulses, which are plotted in Figs. 5(b) and (c). We used a negative bias of approximately 0.4 V to quickly remove the remaining free carriers in the EO-based phase shifters. Figs. 5(d) and (e) show the optical responses of the dynamic switching experiments (d) from 1–8' to 1–6' and (e) from 1–6' to 1–8,' respectively. The optical responses were measured using 12.5-GHz bandwidth optical receivers and an oscilloscope. The 10%–90% rise and fall-time were measured to be 6.3 and 7.3 ns, respectively, for this particular case.

We then measured the optical responses of 60 MZIs on the chip. The remaining four MZIs were temporarily not able to be measured because the wire bonds were accidentally broken. Figs. 5(f) and (g) respectively show the rise and fall optical responses of the 60 MZIs, where the 10%–80% and 10%–90% rise times were 2.5 $\pm$ 0.8 ns and 10.4 $\pm$ 1.5 ns on average, and 6.1 ns and 12.5 ns at maximum. The 80%–10% and 90%–10% fall times were 1.8 $\pm$ 0.1 ns and 2.0 $\pm$ 0.2 ns on average, and 2.2 ns and 2.4 ns at maximum, respectively.

The reason for the longer rise time for 10%–90% was the small dip in the rise-edge response, shown in Fig. 5(f). We consider that this was caused by electrical overshoot, which rotated the phase by more than π and decreased the optical transmittance, originating from an impedance mismatch of the device in RF.

A promising approach to improve the dynamic performance is to integrate on-chip terminators to terminate the transmission line with a 50 Ω impedance. The fabricated switching device did not have any termination structure. Here, we report preliminary measurements of the effect of termination using a test sample fabricated on a silicon platform.

The inset of Fig. 6(a) shows the fabricated sample, in which a TiN film with dimensions of 9 μm $\times$ 300 μm was used as the 50 Ω terminator of the transmission line. We connected this structure with a three-port (GSG) RF probe and measured the temporal response of the system shown in Fig. 6(a) with and without the terminator. Fig. 6(b) shows the measured results without (blue) and with (orange) the on-chip terminator. As can be seen, the terminator can effectively reduce the overshoot

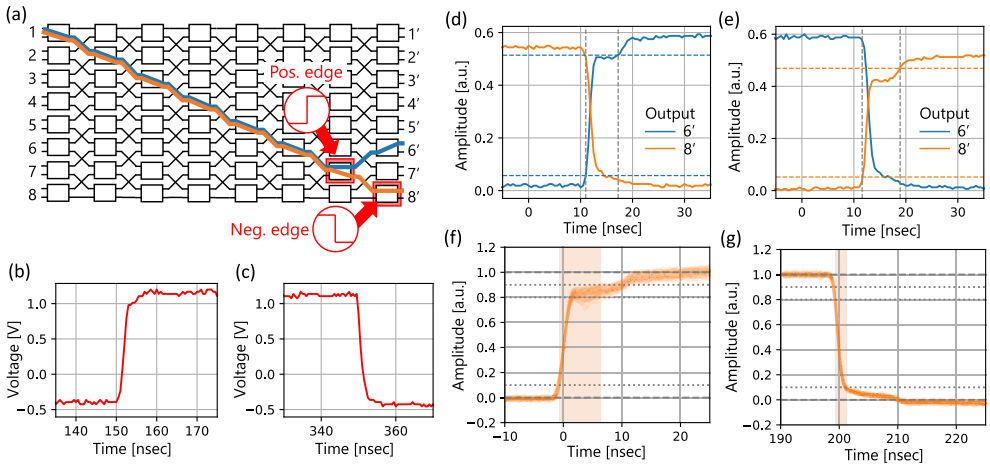

Fig. 5. (a) Schematic of dynamic measurement setup. We input a positive edge to the (7,7)-th MZI and a negative edge to the (8,8)-th MZI. (b) and (c) show the applied pulse shape for the positive and negative edges. A negative bias was applied to remove carriers rapidly. Switching experiments: (d) from 1–8' to 1–6' and (e) from 1–6' to 1–8'. (f) Rising and (g) falling edges of the optical response of 60 MZIs on the chip.

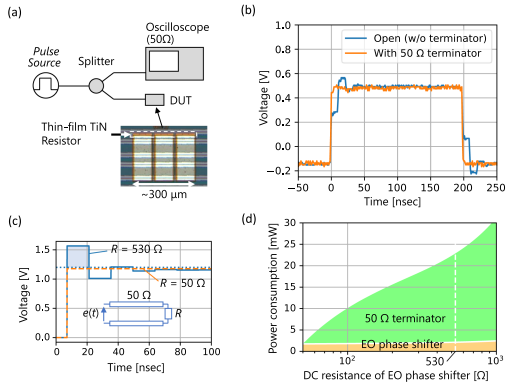

Fig. 6. (a) Illustration of measurement setup for on-chip 50 Ω terminator. (b) Measured electrical wave shapes of pulses with and without the terminator. (c) Calculated voltage response for the case of simple resister-load model in which the resistance is varied. (d) Calculated result of total power consumption of an MZI as a function of DC resistance of the EO phase shifter, where the power fraction of both 50 Ω terminator (green) and the EO phase shifter (orange) were plotted.

and ringing observed in the results in Fig. 5(f). The on-chip terminator demonstrated here can be easily integrated with the switching device because a TiN layer was also used for the TO phase shifters.

For a qualitative analysis, we calculated the voltage responses of EO phase shifter for the cases with and without the terminator, in which the phase shifter is simply regarded as a resister with the resistance of 530 Ω. The calculated results are shown in Fig. 6(c), where the inset shows the circuitry of the calculation. The length of the transmission line and the internal resistance of the voltage source were estimated to be 1.5 meters and 20 Ω, respectively. Because the EO phase shifter is a diode with the forward voltage of ∼1 V, the voltage overshoot (indicated by blue shaded region) would result in large injection current. We consider that this is related to the slow optical rise time observed in Fig. 5(f). As shown in the orange dashed line in Fig. 6(c), impedance-matching technique could reduce the amount of the overshoot.

We should also note that adding the resistive 50 Ω terminator to the device would increase the power consumption. Fig. 6(d) shows a calculated result of power consumption of a single MZI as a function of the DC resistance of EO phase shifter. The upper green-shaded (lower orange-shaded) region in this graph shows the power fraction of the terminator (EO phase shifter). From this figure, the terminator consumes much power than the EO phaser shifter. This high power consumption could be alleviated by reducing the DC resistance of the EO phase shifter by reducing the contact resistance and the series resistance, both of which could be achieved by adjusting the impurity density. Another way to reduce the power consumption would be to use the inductive or capacitive loads to obtain 50 Ω impedance. However, this method can work only for a specific (designed) RF frequency, having smaller effect at DC. In this end, further works would be required to optimize both the response time and the power consumption. As shown here, there seems to be a trade-off between the speed an the complexity (or the power consumption) of the device. If the obtained speed of this paper is already sufficient for the applications, the proposed structure without any termination would be a good solution. Furthermore, modulation on the driving voltages could also be a solution to obtain faster responses without terminations.

IV. Discussion

As discussed in Section I and Section III-A, the PILOSS topology is effective because it has only one 'on' MZI on any path, leading to low and uniform loss. The 'on' MZI had a loss of approximately 1 dB. The remaining $N-1$ 'off' MZIs had a loss of approximately 0.1 dB, which had a relatively small effect on the on-chip insertion loss. We can therefore expect further scaling of the port counts. For example, for a 32 × 32 switch, we can expect that the on-chip loss can be less than 6 dB.

Regarding the crosstalk of the switch, we can also use a double-gated MZI configuration as shown in [18]. In this configuration, although the number of MZIs on the chip is doubled, there is only one additional MZI on the path. Therefore, this

configuration is beneficial when we further increase the port count by reducing the crosstalk of the switch.

We finally discuss about the phase delay between paths which is relevant to large-scale optical circuits. The PILOSS topology actually have exactly the same path lengths between any path settings if we designed to have the same the waveguide lengths between adjacent MZIs. Therefore, the phase delay between paths could be theoretically zero. Although fabrication errors can add phase delays, we consider that they could be trimmed out by using additional TO phase shifters if the range of this error is less than $\sim 2\pi$.

V. Conclusion

In this paper, we proposed and demonstrated the use of PI-LOSS topology for an EO-based Si optical switch. We fabricated an 8×8 EO-based PILOSS switch and characterized all the path settings, observing a uniform loss of 3.8 ± 0.19 dB thanks to the topology. A crosstalk suppression of $>$20 dB for $>$31 nm bandwidth was also observed. We also conducted dynamic switching experiments and found that the 10%–80% and 10%–90% rise/fall-times were less than 6.1 ns and 12.5 ns, respectively. We performed a preliminary demonstration of on-chip terminators to investigate a potential approach to further reduce the response time in future devices. We finally discussed increasing the port count in terms of the loss and crosstalk and presented a possible configuration for the switch topology.

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