INVITED PAPER

Heterogeneous Integration on Silicon Photonics

This paper focuses on other material combinations (a.o. PZT, BTO, and graphene) as well as hetero–epitaxial growth of III–V semiconductors.

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ABSTRACT | To enhance the functionality of the standard silicon photonics platform and to overcome its limitations, in particular for light emission, ultrafast modulation, and nonlinear applications, integration with novel materials is being investigated by several groups. In this paper, we will discuss, among others, the integration of silicon waveguides with ferroelectric materials such as lead zirconate titanate (PZT) and barium titanate (BTO), with electro–optically active polymers, with 2-D materials such as graphene and with III–V semiconductors through epitaxy. We discuss both the technology and design aspects.

KEYWORDS | Electro–optic modulation; hybrid integration; integrated optics; laser; silicon photonics; III–V on silicon epitaxy

I. INTRODUCTION

The main driver for silicon photonics is the fact that standard processes and standard materials from the complementary metal–oxide–semiconductor (CMOS) industry can be reused for realizing complex photonic integrated circuits (ICs) with high yield and high volume. As extensively described in other articles of this issue, this has allowed the field to make tremendous progress over the last decade. However, in some cases, the standard processes and standard materials of the CMOS industry do not suffice. The most prominent example is the laser source. Despite considerable research efforts, thus far there has been no viable path to realizing an efficient on-chip laser relying only on materials commonly used in the electronics industry. Also, continued improvement of "standard" modulators and switches relying on the carrier dispersion effect are increasingly hampered by fundamental tradeoffs between modulation efficiency and losses (see the article by Witzens in this issue). Furthermore, it is not possible to decouple phase and amplitude modulation in these devices, while in many applications pure phase modulation or pure amplitude modulation is desired. Finally, while silicon exhibits a relatively large third-order nonlinearity, nonlinear losses inhibit real breakthroughs in fields such as on-chip supercontinuum generation and frequency combs. Hence there is a growing need to integrate new materials into the silicon photonics platform. This includes direct bandgap III–V semiconductors, which can provide the gain needed for realizing integrated lasers and optical amplifiers. It also includes materials exhibiting a large electro–optic (EO) effect that can be used for realizing more efficient modulators, and interestingly often also exhibit a large second- or third-order nonlinearity, such as electro–optic polymers, ferro–electric materials, graphene and other 2-D materials.

As extensively described in the article by Bowers *et al.* in this issue, a first approach to integrate new materials with silicon waveguides relies on wafer bonding techniques. This approach is maturing rapidly and is extremely versatile in the sense that it can be extended to a wide range of different materials. It also preserves the high quality of the source material without introducing defects, which is particularly relevant for crystalline materials such as III–V semiconductors or lithium niobate. Nevertheless,

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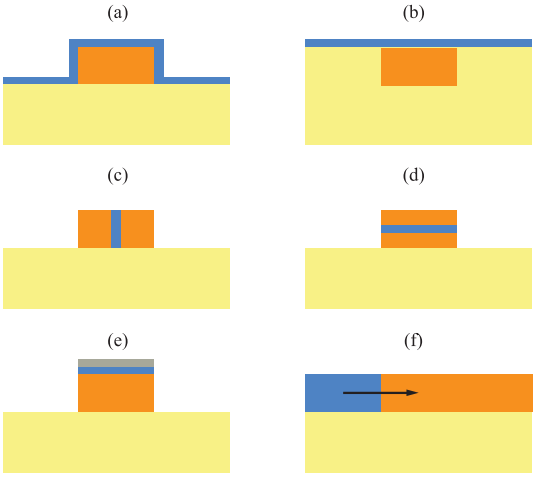

Fig. 1. *Possible schemes for hybrid integration of an active material (blue) with a silicon waveguide (orange): on top of (a) a nonplanarized or (b) planarized waveguide; embedded within (c) a vertical or (d) horizontal slot waveguide; integrated in (e) a hybrid silicon-plasmonic waveguide; (f) butt coupling.*

in some cases, there is the desire to use true wafer scale compatible processes such as physical vapor deposition, spin coating, chemical vapor deposition, or epitaxy. These integration methods allow for a degree of integration not achievable with wafer bonding techniques, such as for the vertical and horizontal slot waveguides discussed below. In most cases, however, cost is the main driver, as these wafer scale processes can, in principle, be cheaper, especially for high volume applications. With each of these approaches, an important hurdle that must be overcome is the high development cost associated with introducing new materials and new processes into a silicon fab. This hurdle could be lower if the material is also already being investigated for new applications in the electronics industry. For example, this is the case for III–V semiconductors and for various 2-D materials, which are being considered for introduction in next-generation electronic nodes.

Fig. 1 schematically illustrates how the new materials can be integrated on the silicon photonics platform. The most straightforward approach is to simply deposit the material on top of the waveguide [Fig. 1(a) and (b)]. Planarizing the waveguide [Fig. 1(b)] by chemical mechanical polishing (CMP) is in certain cases essential for reaching high yield, e.g., for 2-D materials (see Section IV). In other cases, in particular for lower index materials, this option leads to a very low confinement of the optical field in the optically active material, reducing the efficiency of the device. One option is, therefore, to embed the active material in the center of the waveguide core, as shown in Fig. 1(c) and (d). In the case of a low index active material, embedded in a higher index waveguide, the boundary conditions for the surface normal electric field can further enhance the optical confinement. This is the so-called slot effect [30] and has been exploited both for EO polymers, as discussed in Section II and for barium titanate, as discussed in Section III. The drawback of this embedding approach is that waveguide manufacturing is typically somewhat more involved. Even greater field enhancement can be obtained through the use of plasmonic waveguides, and several different approaches have been proposed. The common disadvantage shared by these metallic waveguides are their high optical losses. The hybrid silicon-plasmonic waveguide shown in Fig. 1(e) exploits both plasmonic confinement and dielectric confinement, offering an interesting compromise between losses and field enhancement [1]. Finally, the active material can be deposited in a separate region. One example of this is the butt coupling scheme as shown schematically in Fig. 1(f). When integrating silicon waveguides with III–V epitaxy, this might be the preferred method (see Section V). For a particular application, the choice of the most appropriate integration scheme may also depend upon other factors, such as the temperature budget of the processes involved and compatibility of a material with the fab.

In this paper, we will review recent progress in the field of hybrid integration of novel materials with silicon photonics, using wafer scale processes. Specifically, we will discuss the integration with ferro–electric materials (Section II), with electro–optical polymers (Section III), with 2-D materials (Section IV) and with III–V semiconductors (Section V). For each material, we discuss the integration approaches being investigated, current state of the art and an outlook to the future maturation of the related platform.

II. INTEGRATION WITH FERRO–ELECTRIC MATERIALS

Lithium niobate ($LiNbO_3$ or LN) has long been the preferred material for building the high-performance modulators used in telecom systems. They are also widely used in sensing applications and, for example, gyroscopes. They are very attractive because through the large Pockels effect in LN they can provide pure phase modulation, without spurious amplitude modulation, contrary to silicon modulators relying on the carrier dispersion effect or III–V modulators relying on the quantum confined Stark effect. The recent development of techniques for realizing thin film LN allows now for the integration of crystalline LN layers with silicon waveguides using wafer bonding approaches [2]. Using such an approach, Zhang [3] demonstrated Mach–Zhender modulators exhibiting a bandwidth beyond 100 GHz, and a $V_\pi L = 2.2$ V.cm (in a push–pull configuration). While this waferbonding-based approach is very promising, thus far no practical method for integrating LN monolithically on silicon has been shown. Furthermore, the EO coefficient of LN is relatively low. An interesting alternative is barium titanate ($BaTiO_3$ or BTO), which exhibits a very large EO coefficient ($r > 1000$ pm/V, for bulk films). McKee *et al.* [4]

showed that BTO can be grown on Si using a thin BaO buffer layer. In later work, it was shown that $SrTiO_3$ (STO) can be an efficient buffer layer for growing BTO on Si [5]. The STO buffer layer overcomes the chemical incompatibility between Si and STO and drives the desired 45° orientation between the lattices of both materials, which reduces the original mismatch in lattice constant between silicon and STO/BTO (>25%) to less than 2%. More recently, Abel *et al.* optimized the STO buffer layer to monolithically integrate BTO on Si for optical applications [6]. An effective EO constant $r_{\text{eff}} = 148$ pm/V was extracted, establishing the potential of this approach for optical applications. However, BTO has a relatively low refractive index ($n_{\text{BTO}} = 2.38$) compared to silicon, and therefore simply depositing it on top of a silicon waveguide [Fig. 1(a) and (b)] would lead to a low optical confinement. Xiong *et al.* [7] therefore proposed to use a slot waveguide, fabricated by first growing an STO/BTO stack on an SOI substrate using molecular beam epitaxy, followed by an amorphous silicon layer. Only the top silicon layer was patterned, avoiding the need for etching the BTO layer. Several functional devices (grating couplers, ring resonator, MZI) were demonstrated, including modulators with $V_\pi L = 1.5$ V.cm (with an applied bias $V_{\text{bias}} = 20$ V), equivalent with an effective Pockels coefficient $r_{\text{eff}} \sim 210$ pm/V. The largest modulation bandwidth obtained was 4.9 GHz, limited by electrical parasitics. Unfortunately, the waveguide losses were relatively high (∼ 44 dB/cm). More recently, Abel *et al.* [8] used wafer bonding with a thin Al_2O_3 interlayer to form the desired horizontal slot waveguide structure, circumventing the need for amorphous silicon deposition. Again, a range of different passive devices with good performance were reported and tuning of a ring resonator resonance with very low power consumption (<4 μW/nm) was also demonstrated. The measured $V_\pi L$ product was 1.35 V.cm ($r_{\text{eff}} \sim 300$ pm/V). However, waveguide losses were once again very high, varying from ∼ 50 dB/cm up to ∼ 600 dB/cm depending on the process conditions. An in-depth study of the origin of these losses was subsequently carried out and revealed hydrogenation of the STO buffer to be the primary culprit [9]. This study also showed that annealing at relatively low temperature (300 °C–400 °C) can reduce these losses to 6 dB/cm, a very promising number for future applications. More recently, a device working at high data rates was reported in the form of a BTO-plasmonic modulator, integrated on a silicon platform [10]. The plasmon waveguide ensures a very strong overlap between the optical and electrical field, resulting in a very compact device (10 μm). NRZ modulation at data rates up to 72 Gb/s was demonstrated. Also integration in the back end of line of a full silicon photonics platform was shown [11], with excellent performance (25-Gb/s operation, $V_\pi L = 0.3$ V.cm, loss 5.8 dB/cm). It is important to note that in order to optimize the EO response of the integrated device, the relative orientation of the BTO domains, the applied electric field, and the polarization of the optical field are crucial [12]. In most cases, the BTO layer is a-axis oriented (long tetragonal a-axis of the crystallographic unit cell parallel to the silicon surface), but it has been shown that through strain engineering c-axis orientation can also be obtained [13]. Recently, advanced in-plane piezoforce microscopy (PFM) was used to investigate in-plane domain dynamics during modulator operation [14].

Given the high cost of molecular beam epitaxy (MBE), Kormondy *et al.* [15] also investigated alternative deposition techniques such as pulsed laser deposition (PLD), RF sputtering, and chemical vapor deposition (CVD). However, in each case, the Pockels coefficient of the resulting film was strongly degraded. An alternative approach was proposed in [16], relying on the use of a thin spin-coated lanthanide buffer layer on which the BTO layer is deposited using a sol-gel method. The transparent buffer layer can induce a preferential orientation in the BTO layer. Later this method was extended to other ferro–electric materials such as PZT, and an effective Pockels coefficient $r_{\text{eff}} \sim 150$ pm/V was demonstrated. In [17], these layers were integrated on SiN ring resonators, demonstrating a $V_\pi L \approx 3.2$ V . cm, low propagation losses ($\alpha \approx 1$ dB/cm), bandwidths beyond 33 GHz, and data rates of 40 Gb/s.

The above results show that the monolithic integration of BTO on silicon using MBE is very promising: an effective Pockels coefficient considerably higher than that of bulk LN was demonstrated by several groups and the large waveguide losses originally observed seem now to be understood and resolvable. In addition, this approach is compatible with standard fabrication methods used in CMOS foundries. That said, several important issues remain to be resolved. The best values for the effective Pockels coefficient were obtained under a large electrical bias. Furthermore, in some cases, other effects (such as charge accumulation) that might affect practical use were observed. Finally, the effectiveness and stability of poling the domains in the BTO layer is not yet well studied. Consequently, thus far no practical device has been demonstrated, leaving considerable room for further research.

III. INTEGRATION WITH ORGANIC EO MATERIALS

Integration of organic materials with silicon waveguides allows one to combine the tremendous processing advantages of silicon photonics with the wealth of optical properties that can be obtained by molecular engineering of organic materials [18]–[20]. Silicon-organic hybrid (SOH) devices have been demonstrated to provide both second-order [21]–[25] and third-order [26]–[28] optical nonlinearities, as well as optical gain [29]. For efficient devices, it is imperative to maximize the interaction of the optical silicon waveguide mode with the organic cladding materials, for example by exploiting discontinuous field enhancement in slot-waveguide structures [30],

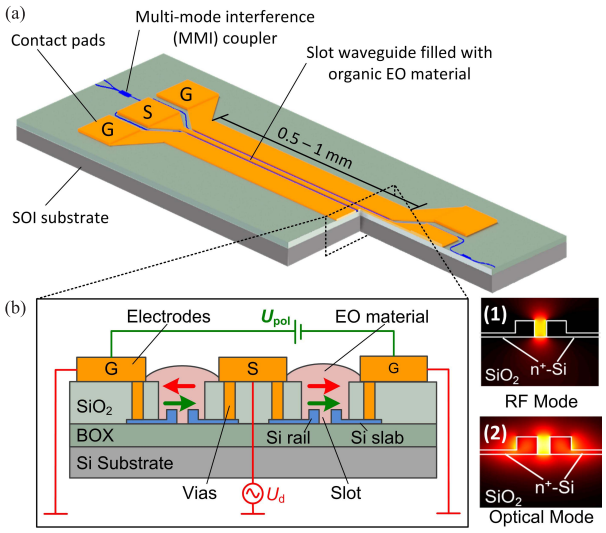

Fig. 2. ***Device concept of a SOH MZM. (a) Device layout: The device relies on silicon photonic slot waveguides embedded into a highly efficient organic EO cladding material. The light is split by a multimode-interference coupler (MMI) into the two arms of the MZM. (b) Device cross section: Each slot waveguide consists of a pair of silicon photonic rails (typical width 200–240 nm, typical height 220 nm), separated by a narrow slot (typical width 80–160 nm). The EO cladding material homogeneously fills the slot. The signal is applied via a GSG coplanar transmission line, which is connected to the rails of the slot waveguide by thin conductive n-doped silicon slabs (typical height 70 nm) and aluminum vias. For poling of the EO materials, a dc voltage U_{pol} (green circuit) is applied at an elevated temperature and removed after cooling. A modulating drive voltage U_d applied to the signal electrode induces an electric field in the slots (red arrows) that is anti-parallel (parallel) in the left (right) arm of the MZM, thus leading to efficient push–pull operation. Insets (1) and (2): Field distributions of the modulating electrical RF mode and the optical quasi-TE mode, respectively. The strong overlap of the RF mode and the optical mode leads to highly efficient modulation. Figure adapted from [32].***

also shown in Fig. 1c. The remainder of this section will focus on SOH EO modulators, since those devices feature the largest application potential.

SOH EO modulators have been shown to outperform conventional all-silicon depletion-type *pn*-modulators both in terms of speed [31]–[33] and energy efficiency [25], [34], [35], [36]. The concept of an SOH Mach–Zehnder modulator (MZM) is sketched in Fig. 2(a) and (b). Each arm of the modulator consists of a silicon photonic slot waveguide, comprising a pair of silicon rails. The doped rails are separated by a narrow slot with typical widths between 80 and 160 nm, depending on the resolution of the underlying fabrication technology. The electrical RF drive signal is applied via a ground–signal–ground (GSG) transmission line and copropagates with the optical signal along the device. The transmission line is connected to the silicon rails of the slot waveguide by metal vias and conductive n-doped silicon slabs (typical thickness $h \approx$ 70 nm). The electrical RF voltage drops mainly across the narrow slot, to which the light is highly confined, thus leading to a strong overlap of the optical mode and the modulating RF field [see insets of Fig. 2(b)]. This represents a key advantage in comparison to conventional organic EO modulators [37], [38]. The device is functionalized by filling and coating the slot waveguide with an EO organic cladding material. To activate the macroscopic $\chi^{(2)}$-nonlinearity, the microscopic molecular dipoles in the organic material need to be aligned in a dedicated one-time poling process. To this end, a poling voltage U_{pol} is applied across the (floating) ground electrodes at an elevated temperature. After cooling down to ambient temperature, the poling voltage can be removed, and the molecule orientation remains in the aligned state [indicated by green arrows in Fig. 2(b)]. The modulating field (red arrows) induced by the RF drive voltage U_{d} is oriented parallel to the chromophore alignment in one phase modulator and antiparallel in the other phase modulator, thereby resulting in efficient chirp-free push–pull operation of the MZM. While fabrication of SOH modulators for research experiments has relied on high-resolution electron-beam lithography [39]–[41], more recent demonstrations were based on deep-UV (DUV) lithography processes on a commercial platform, which offers the full portfolio of silicon photonic devices and SiGe detectors [31], [32], [42].

Over the last few years, the remarkable performance of SOH EO modulators has been demonstrated in a series of experiments, exhibiting efficiencies with voltage-length products down to $U_\pi L = 0.3$ V.mm and energy consumptions of only a few fJ per bit [34]–[36]. Losses are typically in the order of 2 dB/mm, currently dominated by scattering losses in the slot waveguide. Improved lithography processes might reduce these such that the doping in the silicon rails will become relevant as still some light is guided by the latter. The response of the EO cladding materials is ultrafast and enables small-signal modulation at frequencies beyond 100 GHz [42]. The viability of SOH devices has been demonstrated both for data transmission using intensity modulation and direct detection (IM/DD) and for coherent communications. Regarding IM/DD transmission, generation of 100-Gb/s ON–OFF keying (OOK) data signals and 120-Gb/s pulse amplitude modulation-4 was shown [32], [33]. For coherent communications, generation of advanced modulation formats such as 16quadrature amplitude modulation (QAM) was demonstrated at record-low energy consumptions and with symbol rates of up to 100 GBd transmitted on a single polarization [40], [41], [33], [43]. The extraordinarily low drive voltage of SOH modulators allows operation of these devices directly from standard output ports of field-programmable gate arrays (FPGAs), without external amplifiers or digital-to-analog converters [42]. Such schemes can be used even if higher order modulation formats such as 16QAM are to be generated [42]. SOH EO modulators have also proven useful for frequency comb generation [44] or as ultracompact phase shifters for optical metrology applications [45].

Besides boosting the performance of SOH devices, research efforts have also concentrated on improved organic EO materials. Currently, in most material systems, less than 15% of the EO activity inherent in the chromophores is translated to macroscopic EO effects by poling. Improved theoretical methods [18]–[20] have led to new classes of organic EO materials and allowed systematic improvements of the poling efficiency. This resulted in macroscopic EO coefficients r_{33} in excess of 500 pm/V in thin films [46], [48]–[51] and of up to 390 pm/V in SOH devices [36]. Theoretical calculations also suggest that new chromophores with significantly improved molecular first-order hyperpolarizability are possible [46], which would enable SOH modulators with π-voltages of less than 100 mV.

Alongside the improvement of EO coefficients, the thermal and photochemical stabilities of EO cladding materials are also the subject of ongoing investigation and optimization [47]. Thermal stability is defined by lattice hardness and usually quantified by the glass transition temperature T_g of the material [48]. A glass transition temperature of $T_g = 150$ °C is adequate to satisfy Telcordia standards, and such temperatures may be achieved by cross-linking chemistry, for which values of $T_g = 200$ °C are routinely obtained [48]. A specific advantage of organic EO materials is that a variety of parameters such as EO activity, optical loss, dielectric permittivity, lattice hardness, material compatibility, and ease of material processing can be simultaneously optimized by systematic chemical modification of the material. SOH devices will hence immediately benefit from future advances in design and synthesis of functional organic optical materials.

IV. INTEGRATION WITH 2-D MATERIALS

Graphene and other 2-D materials, such as transition metal dichalcogenides, have attracted a lot of attention in the electronics industry in recent years. One reason for this interest is the fact that these 2-D allotropes and compounds can possess electrical, mechanical, and optical properties which differ significantly from their 3-D relatives [52], [53]. Furthermore, they can be stacked in van der Waals heterostructures to extend their functionality [54]. Consequently, 2-D materials represent an exciting new platform that may be key to unlocking applications which are challenging (if not impossible) with conventional technologies and traditional materials [55]. While the library of available 2-D materials continues to grow [53], graphene is, at present, the most mature in terms of production, processing, and integration with existing Si technology. Graphene's appeal stems from its unique combination of properties, including high carrier mobility (room temperature $\mu > 100\,000$ cm^2/Vs at low carrier densities [56]) and the possibility of opening a bandgap in this intrinsically zero-gap material [57], paving the way for high-performance graphene-based FETs. However, for photonics applications, including integrated Si-based devices, it is graphene's optical absorption that is the most fascinating. This single atomic monolayer of carbon, in the absence of significant doping, absorbs 2.3% of normally incident light from the visible to mid-infrared (mid-IR), a value which is solely determined by fundamental constants ($= \pi\alpha$, where $\alpha = e^2/\hbar c \approx 1/137$ is the fine structure constant) [59]. What is more, by increasing the carrier concentration, for example by electrostatic gating, this absorption can be suppressed [60], making graphene highly appealing for use in both optical modulators and detectors. Graphene also lends itself naturally to Si waveguide integration, where the transferred graphene sheet lies in the plane of the waveguiding components (parallel to light propagation). If the waveguide mode has an electric field component parallel to the graphene surface, then optical absorption can occur, with a magnitude which is then dependent upon the interaction length.

In 2011, Liu *et al.* reported the first integration of single-layer graphene (SLG) with a Si waveguide to produce a broadband (1.35–1.6 μm) electroabsorption modulator (EAM) [61]. Electrostatic gating was achieved with an electrical bias applied between the graphene and the underlying doped Si waveguide (separated by a thin dielectric spacer), leading to a modulation depth of up to 0.1 dB/μm (for quasi-TM polarized light, which has a higher interaction with the graphene layer than quasi-TE polarized light; for a detailed discussion, see [63]). The same group went on to quickly demonstrate a double-layer graphene (DLG) modulator [62], where two graphene layers (again, separated by a dielectric spacer) were placed over the Si waveguide. In this case, the gate bias was applied between the graphene layers, each sheet thereby gating the other, to achieve a modulation depth of over 0.16 dB/μm. The larger modulation depth per unit length in DLG modulators allows for smaller devices—crucial when electrical bandwidth is limited by the inverse of the device resistance–capacitance (RC) product. It is worth noting that DLG modulators do not require a doped waveguide, simplifying one aspect of fabrication and removing another potential RC contribution, while also making them compatible with other waveguide materials such as silicon nitride [63], [64].

Since their first demonstration, the performances of SLG-Si and DLG-Si modulators have continued to improve. Large modulation depths (>12 dB) have been achieved in SLG-Si microring resonators [65], albeit sacrificing the optically broadband aspect of nonresonant designs. On the other hand, SLG-Si modulators employing straight waveguides have been demonstrated with low driving bias (2.5 V), bit rates of 10 Gb/s, static power consumption $< 1 \times 10^{-4}$ mW and dynamic energy consumption as low as 350 fJ/b [66]. Dalir *et al.* used DLG beneath an amorphous Si waveguide to achieve broadband (1500–1640 nm) athermal (25 °C–145 °C) modulation at speeds of 35 GHz [67] (see Fig. 3), although with a

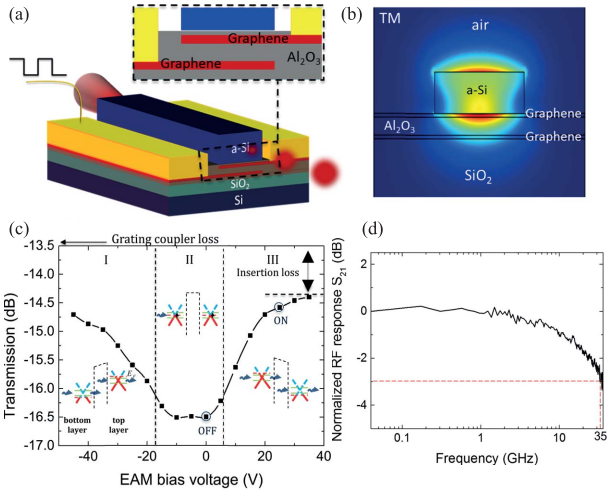

Fig. 3. ***Double-layer graphene modulator results. (a) and (b) Device schematic and calculated quasi-TM optical mode profile. (b) Transmission versus applied bias between graphene layers. Insets: Band profiles of graphene (blue and red for unoccupied and occupied states, respectively). (d) High-frequency response showing 3-dB frequency of 35 GHz. Figure adapted from [67].***

relatively low modulation efficiency of ∼0.1 dB/V (note that in all graphene–Si modulators, a tradeoff typically exists between modulation bias and speed; thinner gate dielectrics reduce the required gate bias but increase device capacitance). Many of the reported graphene–Si EAM performance figures approach or surpass those of state-of-the-art SiGe EAMs [66], although further work is still required to combine them in a single device.

To date, graphene–Si EAMs have been the most intensively studied. However, for some complex modulation formats, phase modulators are necessary. These too can be achieved with graphene as its electrostatically controlled absorption can produce a large change in the effective refractive index of a SLG-Si waveguide (on the order of 10^{-3}) [68]. Recently, this effect was utilized in SLG-Si phase modulators to achieve modulation depths and efficiencies of 35 dB and 0.28 dB/cm, respectively [69].

As mentioned above, graphene is also a promising material for ultrafast integrated graphene–Si photodetectors (GPDs). Its broadband absorption, extremely short photo-generated carrier lifetimes and high mobility (enabling fast carrier extraction) make it ideal for ultrafast operation. Pulsed laser-based measurement of GPD response times indicate bandwidths of over 260 GHz [70]. A number of GPD structures have already been demonstrated, relying on a variety of photodetection mechanisms such as the bolometric, photovoltaic, photothermoelectric, and photogating effects [71]–[76]. It must be noted that multiple effects may occur simultaneously in devices or become dominant under varying operating conditions [77]. The underlying physics behind each of these effects is discussed in depth in a recent comprehensive GPD review [77]. In terms of device performance, the last few years have seen huge advances. Responsivity values of tens of mA/W at zero bias and up to hundreds of mA/W under applied bias have been reported [74], along with a steady increase in operating speeds, now reaching >76 GHz [76]. One common drawback of the lateral metal–graphene–metal architecture employed in many GPD structures is a high dark current under biased operation (necessary for high responsivity). An alternative architecture which avoids this issue is a metal–graphene–Si plasmonic Schottky photodetector [78]. Goykhman *et al.* showed that integration of graphene greatly enhanced Schottky photodetector performance, giving an internal quantum efficiency of 7% and good responsivity (85 mA/W at 1 V reverse bias) with minimal dark current. Under higher bias avalanche multiplication gives even higher responsivities (∼0.4 A/W at 3 V reverse bias).

The performance of graphene–Si modulators and photodetectors is expected to improve as 2-D material processing techniques continue to mature. Many of the results to date have relied upon small graphene flakes produced by mechanical exfoliation from graphite crystals, manually transferred to devices. Pristine (high μ) graphene is produced in this way, but submillimeter flake dimensions—and the time-consuming nature of the process—limit the scalability of this approach. The most promising alternative is CVD-grown wafer scale monolayer graphene (typically grown on metal substrates and transferred to the target substrate using a polymer support [55]). Although this graphene is of lower quality than exfoliated material, recent high-speed GPD devices have been processed in a 6-inch semiconductor pilot line using large area CVD-grown graphene [76] (see Fig. 4). Single-crystal

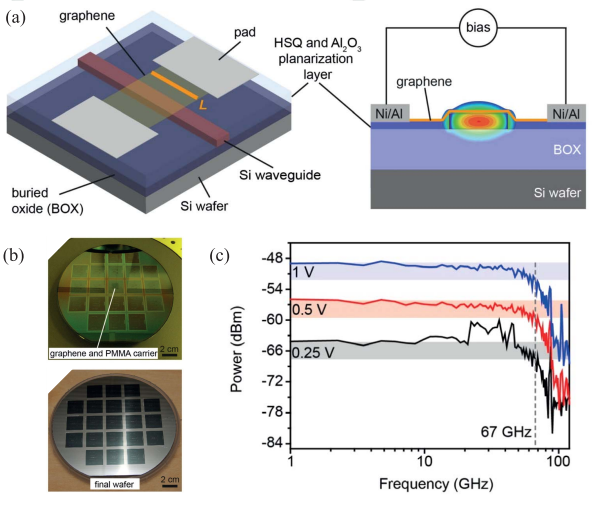

Fig. 4. ***Example of a typical lateral metal–graphene–metal photodetector on a Si waveguide. (a) Device schematics. (b) Devices were processed using wafer scale CVD-grown graphene, a significant technological milestone. (c) GPD frequency response of a typical GPD at various bias voltages. Figure adapted from [76].***

CVD-grown graphene [79], possibly in combination with graphene transfer printing techniques [80], may lead to even higher μ and therefore device performance (for example, higher modulation efficiency and lower insertion loss in graphene–Si EAMs [63]). High contact resistances between graphene and metal, which limited early device operating speeds [61], can be overcome by using 1-D edge contacts with CMOS compatible metals such as Ni ($<$ 100 $\Omega.\mu$m [81]). Finally, encapsulation of graphene between thin layers of exfoliated hexagonal boron nitride (hBN) is known to dramatically improve graphene quality (giving flatter, higher mobility material, which is also protected from ambient moisture; a source of unintentional graphene doping). Ongoing advances in wafer scale CVD hBN growth are, therefore, expected to be hugely beneficial to graphene device performance. This nicely reinforces an important point when looking ahead to the future of heterogeneous integration of 2-D materials: Although the use of individual 2-D materials (such as graphene) can and will lead to novel, high-performance devices, even greater accomplishments may be achieved when 2-D materials are combined to reveal their full potential.

V. III–V EPITAXY

Thus far, the use of III–V semiconductors provides the only viable path toward realizing practical laser sources for applications in integrated photonics. Wafer bonding techniques for integrating direct bandgap III–V semiconductors on silicon substrates have matured considerably over the last decade and now provide a viable route toward large scale integration of efficient lasers on a silicon photonics platform. On the other hand, monolithic integration of III–V semiconductors on silicon using epitaxial techniques remains a very attractive approach to be pursued, as it would provide the ultimate integration density and the advantages of wafer scale integration. However, the large lattice constant mismatch between silicon and relevant III–V materials such as GaAs (4% mismatch) and InP (8%), and the formation of antiphase domains (APDs) at the polar/nonpolar III–V/silicon interface form a big hurdle to achieving this goal. Nevertheless, very substantial progress has been made in the last decade, making commercial deployment of such technology in the coming years a distinct possibility.

Two main approaches can be discerned. In the first of these, the III–V is grown over the full wafer, typically using a few-micrometer-thick metamorphic buffer layer optimized to suppress threading dislocations inside the device layer. Until now it is this technology which has been investigated most intensively and several groups have demonstrated electrically injected lasers operating at room temperature. However, at present, this approach does not offer a straightforward path toward integration with standard silicon photonics devices. The second main approach focuses on the selective area growth of III–V materials on prepatterned silicon substrates. This provides a clearer path toward integration with waveguides, but thus far only optically injected laser devices have been reported. Below we will discuss the main results obtained using these two approaches.

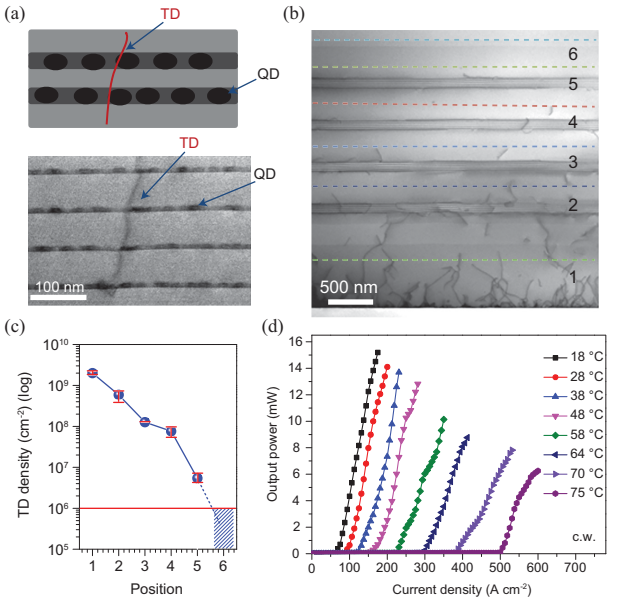

Fig. 5. *InAs/GaAs QD laser on silicon. (a) Schematic and brightfield TEM image describing interaction between QDs and threading dislocations. (b) Brightfield scanning TEM image of defect filtering layers. (c) Dislocation density measured at positions indicated in (b). (d) Light output power versus current at various heatsink temperatures. Figure adapted from [85].*

For realizing lasers operating at a wavelength of 1.3 μm, self-assembled InAs quantum dot (QD) layers show particular promise. III–V QD lasers have been shown to be less sensitive to nonradiative defects due to carrier localization within the individual dots. Fig. 5(a) shows a schematic and an SEM picture of a threading dislocation passing through a QD-based device layer (from [85]). Following the first demonstration of lasing at 1.3 μm under pulsed electrical injection [82] most efforts have focused on optimizing the buffer layer, aiming to suppress threading dislocations and APD-formation [83]–[85]. Using a Ge/Si substrate, Liu *et al.* [84] demonstrated lasing with a low threshold current (16 mA), high output power (176 mW), and high continuous-wave (CW) operating temperature (119 °C). Chen *et al.* [85] used a strained-layer superlattice (SLS) based on periodic $In_{0.18}Ga_{0.82}As/GaAs$ layers as a defect filter to reduce the defect density to values below 10^6 cm^{-2} [see Fig. 5(b) and (c)]. This allowed the demonstration of a laser operating with a threshold as low as 62 A/cm^2 (12.5 A/cm^2 per QD layer) up to temperatures of 75 °C [Fig. 5(d)]. The lasers were also operated (in CW) for up to 3100 h.

While very impressive, all of the above results were obtained with off-cut Si substrates (4°–6° toward

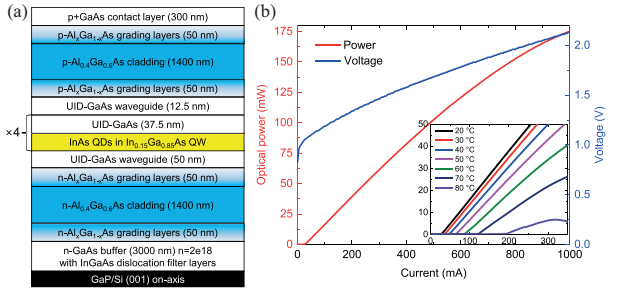

Fig. 6. *InAs QD laser structure grown on a GaP/Si substrate. (a) Cross-sectional schematic. (b) Single-side CW LIV curves at 20 °C from a 2600 μm × 8 μm laser with as-cleaved facets. The inset shows temperature-dependent single-side CW LI curves from 20 °C–80 °C. Figure adapted from [90].*

the [110] plane) in order to avoid the formation of antiphase domains. Unfortunately, such substrates are not compatible with standard CMOS processing. Recent research has therefore focused on exact (001) silicon substrates. In one approach, KOH is used to define v-shaped grooves along the [110] direction in the Si substrate, exposing the {111} surfaces that allow the growth of APD-free III–V layers. This allowed the demonstration optically pumped and later electrically pumped microdisk lasers [87]. In [86], a high-temperature Si substrate preparation step was used to promote the growth of an APD-free GaAs layer. However, the most successful approach to date relies on the use of a GaP/Si buffer layer [89], [90]. The GaP layer is almost lattice matched to silicon and terminates APDs within ∼40 nm of the interface. Using GaP/Si (commercially obtained from NAsP$_{III/V}$ GmbH and grown by MOCVD), Jung *et al.* [90] developed an optimized GaAs-buffer layer (grown by MBE) containing strained InGaAs dislocation filter layers to reduce the defect density to a few 10^6 cm^{-2}. A QD-based laser stack containing four QD layers was grown on top of this buffer [full stack shown in Fig. 6(a)]. A record low threshold current for a III–V-on-silicon laser of 6.7 mA (J_{th} = 132 A/cm^2 or 36 A/cm^2 per QD layer), a wall plug efficiency of 38%, operation up to 80 °C and output powers above 100 mW were obtained [see Fig. 6(b)]. Follow-up reliability tests at 35 °C for 1500 h showed an extrapolated mean-time-to-failure of more than one million hours [91], a significant step forward, attributed to the low defect density.

Despite this enormous progress, reaching the important 1.55-μm wavelength is very challenging when relying on InAs-based QDs as the gain medium. A possible solution is to use Sb-based materials. It has been shown that using the correct growth conditions during MBE of III–Sb materials on silicon the high strain can be released through the formation of pure 90° misfit dislocations arranged in a 2-D network at the Si/III–Sb interface [92]. This leads to a very low threading-defect density without the need of a thick metamorphic buffer. Exploiting this effect, CW lasing at 1.55 μm was demonstrated [93].

As previously mentioned, the second approach to overcome the large lattice mismatch between III–V semiconductors and silicon relies on selective area growth in narrow trenches patterned on silicon (001) substrates. The trenches are defined using a shallow trench isolation (STI) process—a standard process in CMOS foundries—and then treated with a wet etch to expose the {111} faces of the silicon substrate. In initial work, bulk InP material was grown in 500-nm-wide trenches [94]. The InP growth conditions (MOCVD) were optimized such that the lattice mismatch toward Si was accommodated via partial dislocations in a highly twinned region parallel to the {111} facets. This section of microtwins is only a few tens of nanometers thick at the Si/InP interface. Following definition of a DFB grating in the top surface of the InP ridge, the silicon substrate was removed to avoid leakage of the optical field. Single-mode lasing at a wavelength of ∼900 nm was obtained under pulsed optical pumping. In later work, a 50-nm InGaAs gain layer was grown on top of the InP material (after planarization using CMP); see Fig. 7. This allowed shifting of the lasing wavelength to 1.3 μm and a reduction of the lasing threshold to ±8 mW.

In more recent work, GaAs nanoridges where grown, in this case starting from much narrower trenches (60–120 nm) [96]. Again, the v-shaped bottom of the trench suppresses APD formation, while the high aspect ratio of the trenches suppresses threading dislocations by trapping them at the sidewalls [see Fig. 8(a)]. This results in high crystalline quality of the material growing out of the trenches and no threading locations are observed in the region above the substrate. For more details on the epitaxy process, see [97]. Changing the growth conditions allows one to control the ratio of the vertical and horizontal growth speed, thereby controlling the shape of the resulting nanoridge. In this way, the nanoridge

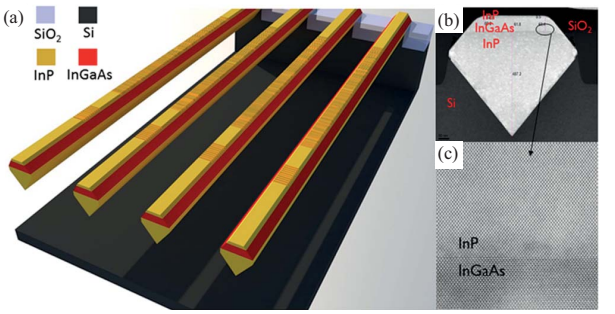

Fig. 7. *(a) Schematic plot of the monolithically integrated InGaAs/InP DFB lasers on silicon. The silicon pedestal (and the silicon oxide hard mask) under the near end has been removed for a better view of the III–IV waveguide. (b) STEM image of a typical cross section of the grown InGaAs/InP/Si waveguide. (c) Detail of the InGaAs/InP interface. Reproduced from [95].*

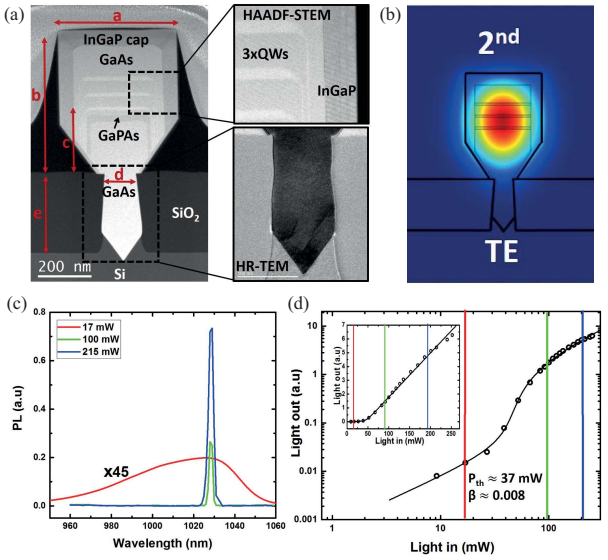

Fig. 8. *GaAs nanoridge laser. (a) HAADF–STEM images. The upper one shows zoomed-in QWs, barriers and the passivation layer while the lower high-resolution (HR) TEM shows that defects are trapped in the V-shaped trench. (b) The guided TE-like mode calculated by FDE simulation. (c) Room-temperature spectra of a DFB laser under different pump powers (100-nm trench width, 170-nm grating period, and 340-nm second-order grating coupler period). (d) L–L curve on logarithmic and linear (insert) scale of the measured DFB nanoridge laser. Black circles and solid line represent the experimental data the rate equations fit, respectively. Figure adapted from [96].*

waveguide can be designed such that leakage of the optical mode toward the substrate is avoided and high optical confinement in the InGaAs quantum well gain region is obtained [see Fig. 8(b)]. An InGaP capping layer was used to passivate the GaAs surface. Single-mode lasing under pulsed optical pumping with a threshold of 37 mW was obtained, showing the high quality of the material [see Fig. 8(c) and (d)].

In a rather different approach, the so-called template-assisted selective epitaxy (TASE) growth method, the III–V material is grown from a small silicon seed in a SiO_2 cavity. In the example shown in Fig. 9(a), the gain material is grown in 5 μm $\times$ 5 μm, hollow SiO_2 growth templates [98]. SEM images reveal GaAs microdisks with diameters of approximately 3.1 μm and heights of 390 nm. Fig. 9(b) shows lasing under room-temperature pulsed optical pumping of these devices.

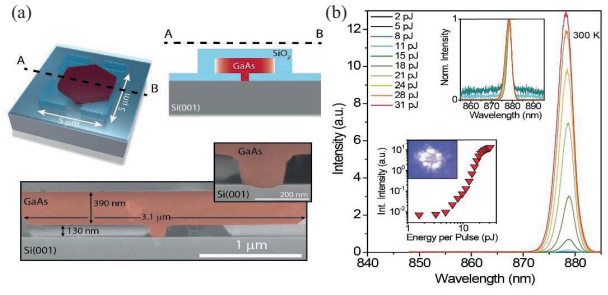

Fig. 9. *(a) Schematic and SEM images of monolithically integrated GaAs microdisks on Si. (b) Power-dependent PL spectra measured at room temperature. The insets show the normalized spectra, L–L curve, and optical image of an excited microdisk. The lasing threshold is approximately 15 pJ/pulse (reproduced from [98]).*

The approaches based on selective area growth have the distinct advantage that, in principle, they can be integrated in a standard CMOS process flow (actually, in several cases, they are derived from processes developed for future CMOS nodes). While integration with waveguides seems rather straightforward, the integration of the electrical contacts (required for electrical injection) without introducing excessive absorption losses is challenging. As such, at this point, it is not clear which approach will dominate the field in the future.

VI. CONCLUSION

In this paper, we reviewed the recent progress and status of the integration of novel materials, providing new or improved functionality, on the silicon photonics platform. Tremendous progress has been made in the field over the last few years. Quantum dot lasers, epitaxially grown on standard (001) wafers, now show extrapolated mean-time-to-failure of more than one million hours [91]. A bitrate of 72 Gb/s was demonstrated in hybrid plasmonic-BTO modulators which were only 10 μm long [10]. SOH modulators exploiting new electro–optically active polymers now outperform standard silicon modulators relying on the carrier dispersion effect on all performance parameters [25]. On the other hand, graphene offers modulation and ultrafast detectors in a single platform, possibly leading to considerable cost savings. Nevertheless, there is still need for concerted research and development efforts before these new materials are offered in a standard platform. Thus far no integration of III–V lasers epitaxially grown on silicon with actual silicon waveguides has been shown. While the hybrid BTO-plasmonic modulator is proof of the materials intrinsic properties, successful demonstration of ferroelectric materials used in a more standard Mach–Zehnder modulator configuration is essential for their broader uptake. Processing of 2-D materials on 200- and 300-mm scales is under development but still a lot of progress is needed, especially with respect to the transfer of graphene from its growth substrate to the device wafer. And also for the silicon-organic hybrids a viable way to integrate these modulators in an industrial platform needs to be demonstrated. All of this will still require considerable resources. Fortunately, we can rely on parallel efforts carried out by the electronics industry, pursuing integration of often identical or at least very similar materials into next-generation electronic chips. As a consequence, it is very likely that these efforts will be successful and that several of these materials will indeed be taken up by the photonics industry in a foreseeable timeframe. ■

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